NEC

MOS FIELD EFFECT POWER TRANSISTORS

2SJ495

SWITCHING P-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

This product is P-Channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Super Low On-State Resistance
  $R_{DS(on)1}$ = 30 mΩ MAX. (V_{GS} = –10 V, I_D = –15 A)
  $R_{DS(on)2}$ = 56 mΩ MAX. (V_{GS} = –4 V, I_D = –15 A)
- Low C_{iss} C_{iss} = 4120 pF TYP.
- Built-in Gate Protection Diode

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	V_{DSS}	–60	V
Gate to Source Voltage*	$V_{GSS(AC)}$	∓20	V
Gate to Source Voltage	$V_{GSS(DC)}$	–20, 0	V
Drain Current (DC)	$I_{D(DC)}$	∓30	A
Drain Current (pulse)**	$I_{D(pulse)}$	∓120	A
Total Power Dissipation (T_C = 25°C)	P_T	35	W
Total Power Dissipation (T_A = 25°C)	P_T	2.0	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

*f = 20 kHz, Duty Cycle ≤ 10% (+Side)

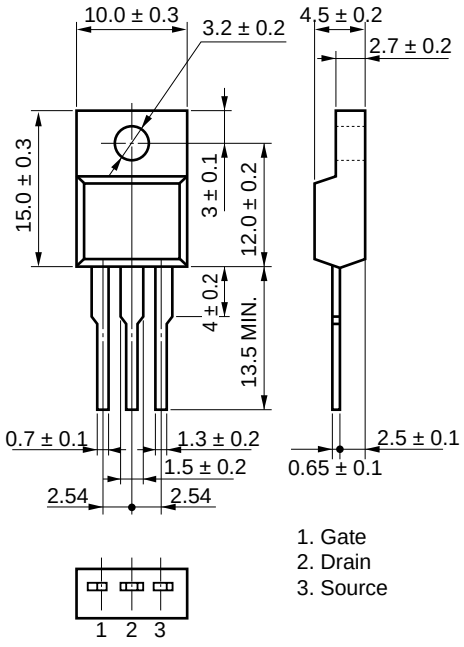
**PW ≤ 10 μs, Duty Cycle ≤ 1%

THERMAL RESISTANCE

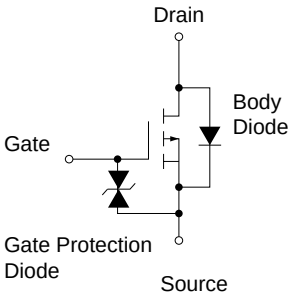
Channel to Case	$R_{th(ch-c)}$	3.57	°C/W
Channel to Ambient	$R_{th(ch-A)}$	62.5	°C/W

PACKAGE DIMENSIONS

(in millimeter)



MP-45F (ISOLATED TO-220)



The diode connected between the gate and source of the transistor serves as a protector against ESD. When this deveice acutally used, an addtional protection circiut is externally required if a voltage exceeding the rated voltage may be applied to this device.

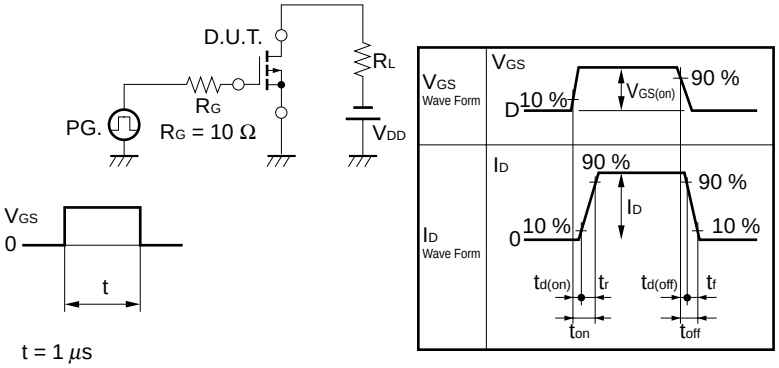
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Date Published November 1997 N
Printed in Japan

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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

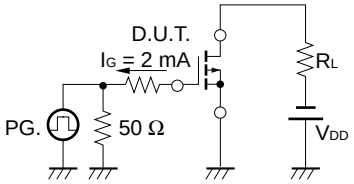
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On–state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –15 A		24	30	mΩ
	$R_{DS(on)2}$	V_{GS} = –4 V, I_D = –15 A		38	56	mΩ
Gate to Source Cutoff Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0	–1.5	–2.0	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –15 A	12	24		S
Drain Leakage Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0			–10	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ∓ 20 V, V_{DS} = 0			∓10	μA
Input Capacitance	C_{iss}	V_{DS} = –10 V		4120		pF
Output Capacitance	C_{OSS}	V_{GS} = 0		1750		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		580		pF
Turn-On Delay Time	$t_{d(on)}$	I_D = –15 A		40		ns
Rise Time	t_r	$V_{GS(on)}$ = –10 V		220		ns
Turn-Off Delay Time	$t_{d(off)}$	V_{DD} = –30 V		600		ns
Fall Time	t_f	R_G = 10 Ω		380		ns
Total Gate Charge	Q_G	I_D = –30 A		140		nC
Gate to Source Charge	Q_{GS}	V_{DD} = –48 V		12		nC
Gate to Drain Charge	Q_{GD}	V_{GS} = –10 V		46		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 30 A, V_{GS} = 0		0.8	1.5	V
Reverse Recovery Time	t_{rr}	I_F = 30 A, V_{GS} = 0		160		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		400		nC

Test Circuit 1 Switching Time

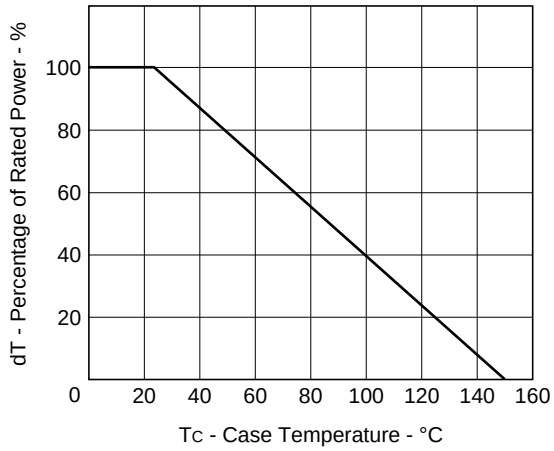


t = 1 μs
Duty Cycle ≤ 1%

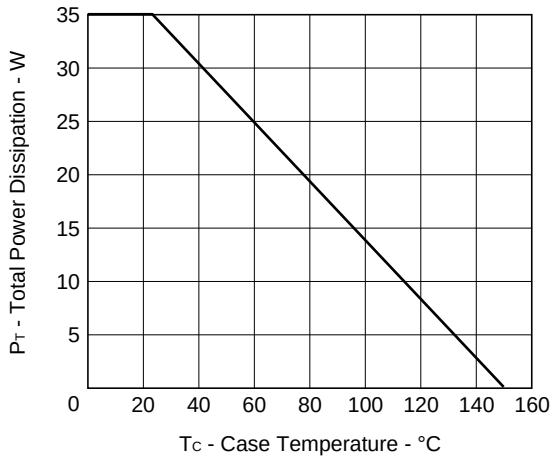
Test Circuit 2 Gate Charge



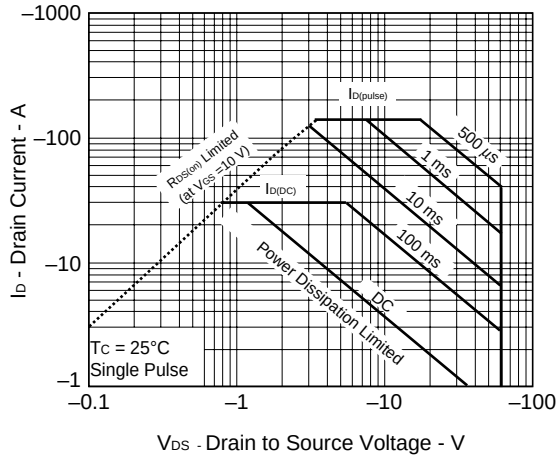
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



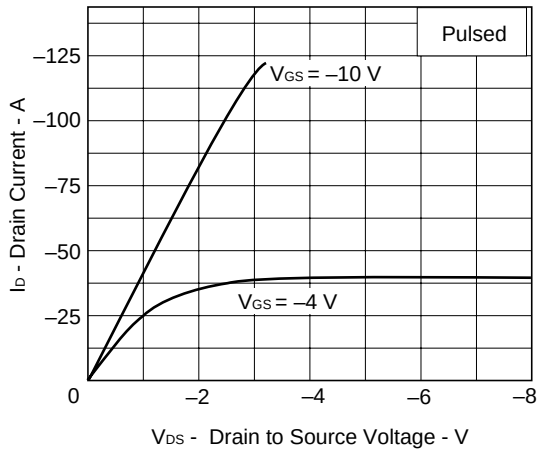
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



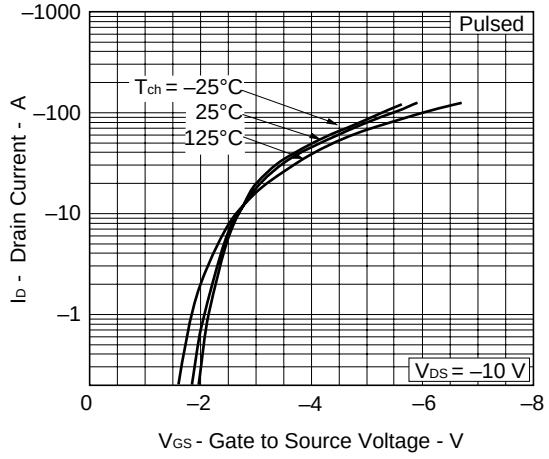
FORWARD BIAS SAFE OPERATING AREA



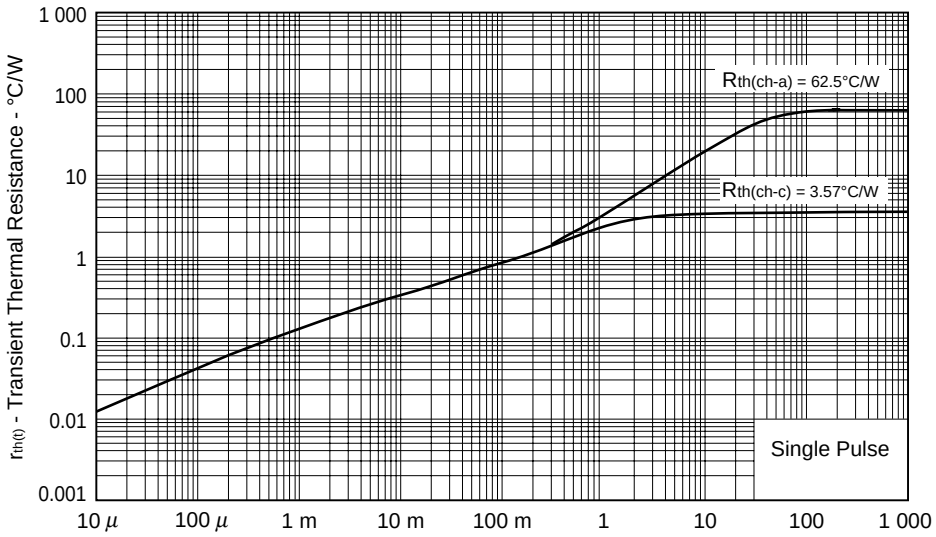
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



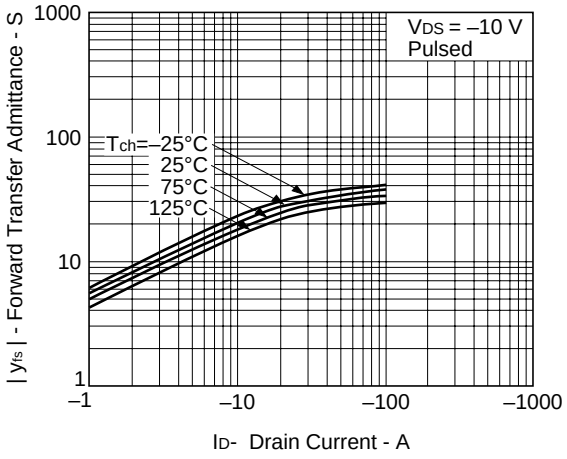
FORWARD TRANSFER CHARACTERISTICS



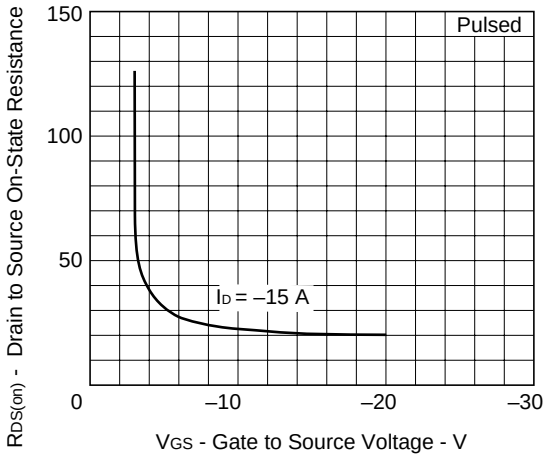
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



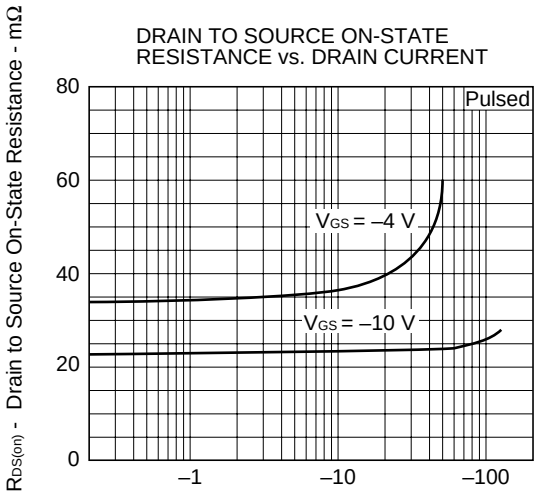
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



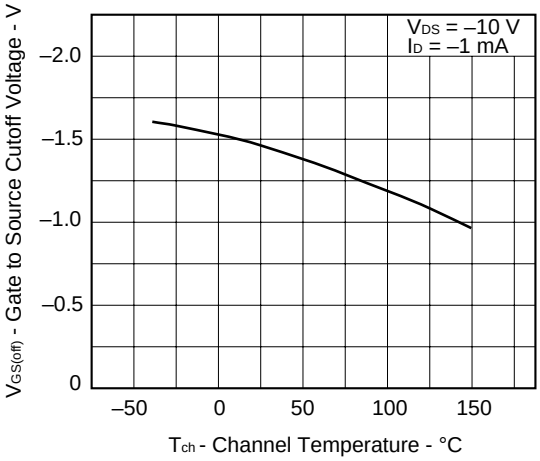
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



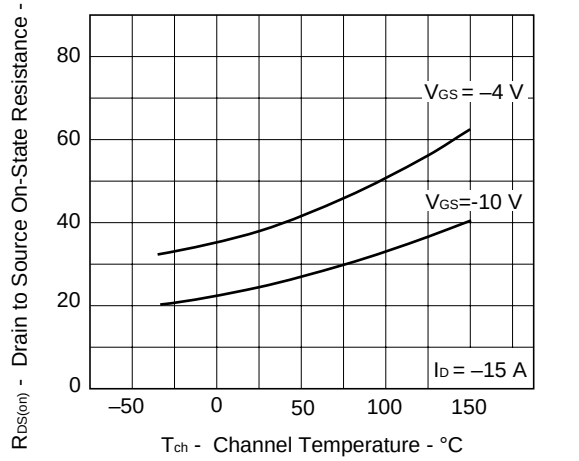
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



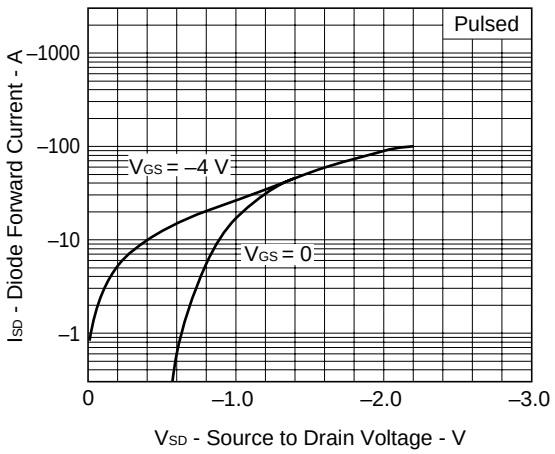
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



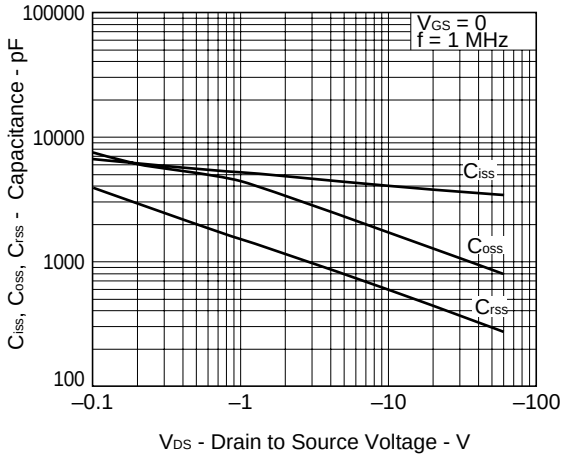
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



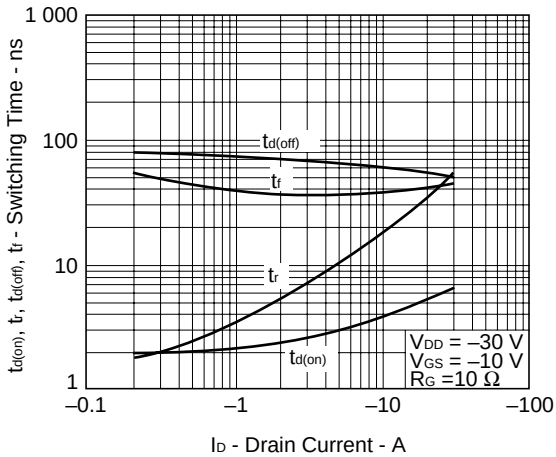
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



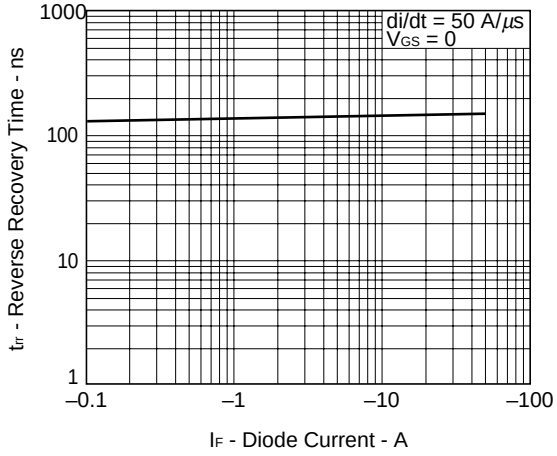
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



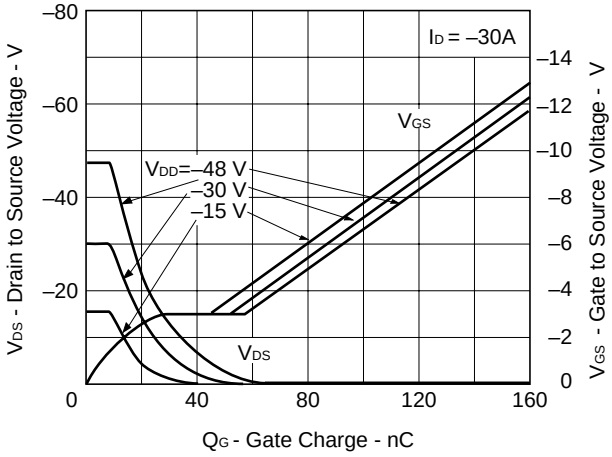
SWITCHING CHARACTERISTICS



REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



Document Name	Document No.
NEC semicondacter device reliabilty/quality control system	C11745E
Power MOS FET features and application to switching power supply	D12971E
Application circuits using Power MOS FET	TEA-1035
Safe operating area of Power MOS FET	TEA-1037
Guide to prevent damage for semiconductor devices by electrostatic discharge (EDS)	C11892E

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Anti-radioactive design is not implemented in this product.

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