# Dual-Input Power Manager/ 3.5A $LiFePO_4$ Battery Charger with $I^2C$ Control and USB OTG

## FEATURES

- **High Efficiency Charger Capable of 3.5A Charge Current**
- **Charge Control Algorithm Specifically Designed for $LiFePO_4$ Batteries (Lithium Iron Phosphate)**
- **Monolithic Switching Regulator Makes Optimal Use of Limited Power and Thermal Budget**
- **Dual Input Overvoltage Protection Controller**
- **Priority Multiplexing for Multiple Inputs**
- **$I^2C$/SMBus Control and Status Feedback**
- **NTC Thermistor ADC for Temperature Dependent Charge Algorithms (JEITA)**
- **Instant-On Operation with Low Battery**
- **Battery Ideal Diode Controller for Power Management**
- **USB On-The-Go Power Delivery to the USB Port**
- Four Float Voltage Settings (3.45V, 3.55V, 3.6V, 3.8V)
- 28-Lead 4mm × 5mm QFN Package

## APPLICATIONS

- Portable Medical Devices
- Portable Industrial Devices
- Backup Devices

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## DESCRIPTION

The LTC®4156 is a 15 watt $I^2C$ controlled power manager with PowerPath™ instant-on operation, high efficiency switching battery charging and USB compatibility. The LTC4156 seamlessly manages power distribution from two 5V sources, such as a USB port and a wall adapter, to a single-cell rechargeable lithium iron phosphate battery and a system load.

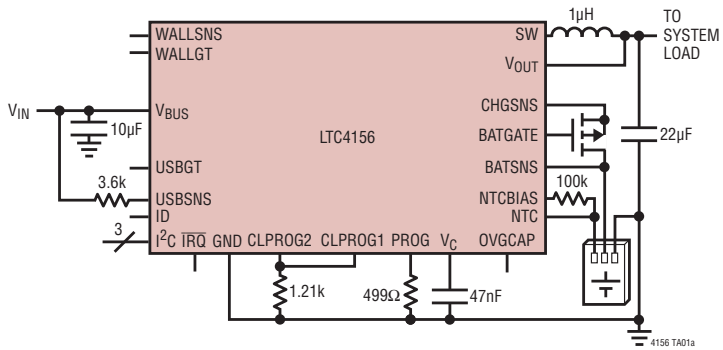
The LTC4156's switching battery charger automatically limits its input current for USB compatibility, or may draw up to 3A from a high power wall adapter. The high efficiency step-down switching charger is designed to provide maximum power to the application and reduced heat in high power density applications.

$I^2C$ adjustability of input current, charge current, battery float voltage, charge termination, and many other parameters allows maximum flexibility. $I^2C$ status reporting of key system and charge parameters facilitates intelligent control decisions. USB On-The-Go support provides 5V power back to the USB port without any additional components. A dual-input, priority multiplexing, overvoltage protection circuit guards the LTC4156 from high voltage damage on the $V_{BUS}$ pin.

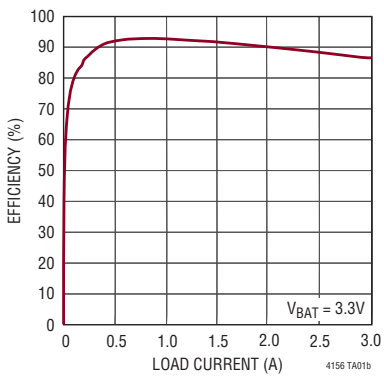
The LTC4156 is available in the low profile (0.75mm) 28-lead 4mm × 5mm QFN surface mount package.

## TYPICAL APPLICATION

**$I^2C$ Controlled High Power Battery Charger/USB Power Manager**




**Switching Regulator Efficiency**



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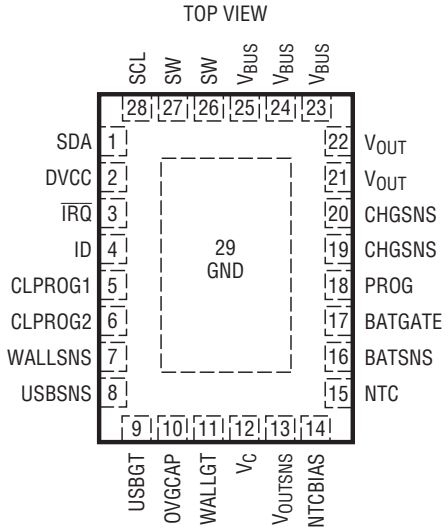
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## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2)**

$V_{BUS}$ (Transient) t < 1ms, Duty Cycle < 1% ... –0.3V to 7V
$V_{BUS}$ (Steady State), BATSNS, $\overline{IRQ}$, NTC..... –0.3V to 6V
DVCC, SDA, SCL (Note 3) .....–0.3V to $V_{MAX}$
$I_{WALLSNS}$, $I_{USBSNS}$..... ±20mA
$I_{NTCBIAS}$, $I_{\overline{IRQ}}$.....10mA
$I_{SW}$, $I_{VOUT}$, $I_{CHGSNS}$ (Both Pins in Each Case).....4A
Operating Junction Temperature Range... –40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

## PIN CONFIGURATION




UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC4156EUFD#PBF | LTC4156EUFD#TRPBF | 4156 | 28-Lead (4mm × 5mm × 0.75mm) Plastic QFN | –40°C to 125°C |
| LTC4156IUFD#PBF | LTC4156IUFD#TRPBF | 4156 | 28-Lead (4mm × 5mm × 0.75mm) Plastic QFN | –40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A \approx T_J$ = 25°C (Note 2). $V_{BUS}$ = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1} = R_{CLPROG2}$ = 1.21k, $R_{PROG}$ = 499Ω, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Switching Battery Charger** | | | | | | | |
| $V_{BUS}$ | Input Supply Voltage | | ● | 4.35 | | 5.5 | V |
| $V_{BUSREG}$ | Undervoltage Current Reduction | Input Undervoltage Current Limit Enabled | | | 4.30 | | V |
| $I_{VBUSQ}$ | Input Quiescent Current | USB Suspend Mode | | | 0.060 | | mA |
| | | 100mA $I_{VBUS}$ Mode, $I_{VOUT}$ = 0µA, Charger Off | | | 0.560 | | mA |
| | | 500mA – 3A $I_{VBUS}$ Modes, $I_{VOUT}$ = 0µA, Charger Off | | | 17 | | mA |
| | | CLPROG1 Mode, $I_{VOUT}$ = 0µA, Charger Off | | | 17 | | mA |
| $I_{BATQ}$ | Battery Drain Current | $V_{BUS} > V_{UVLO}$, Battery Charger Off, $I_{VOUT}$ = 0µA | | | 7.0 | | µA |
| | | $V_{BUS}$ = 0V, $I_{VOUT}$ = 0µA | | | 2.0 | 3.0 | µA |
| | | Storage and Shipment Mode, DVCC = 0V | | | 0.6 | 1.25 | µA |
| $I_{VBUSLIM}$ | Total Input Current When Load Exceeds Power Limit | 100mA $I_{VBUS}$ Mode (USB Lo Power) (Default) | ● | 65 | 80 | 100 | mA |
| | | 500mA $I_{VBUS}$ Mode (USB Hi Power) | ● | 460 | 480 | 500 | mA |
| | | 600mA $I_{VBUS}$ Mode | | 550 | 570 | 600 | mA |
| | | 700mA $I_{VBUS}$ Mode | | 650 | 670 | 700 | mA |
| | | 800mA $I_{VBUS}$ Mode | | 745 | 770 | 800 | mA |
| | | 900mA $I_{VBUS}$ Mode (USB 3.0) | ● | 800 | 850 | 900 | mA |
| | | 1.00A $I_{VBUS}$ Mode | | 950 | 1000 | 1025 | mA |
| | | 1.25A $I_{VBUS}$ Mode | | 1150 | 1230 | 1300 | mA |
| | | 1.50A $I_{VBUS}$ Mode | | 1425 | 1500 | 1575 | mA |
| | | 1.75A $I_{VBUS}$ Mode | | 1650 | 1750 | 1875 | mA |
| | | 2.00A $I_{VBUS}$ Mode | | 1900 | 2000 | 2125 | mA |
| | | 2.25A $I_{VBUS}$ Mode | | 2050 | 2175 | 2300 | mA |
| | | 2.50A $I_{VBUS}$ Mode | | 2350 | 2475 | 2600 | mA |
| | | 2.75A $I_{VBUS}$ Mode | | 2550 | 2725 | 2900 | mA |
| | | 3.00A $I_{VBUS}$ Mode (Default) | | 2800 | 2950 | 3100 | mA |
| | | 2.5mA $I_{VBUS}$ Mode (USB Suspend) | | | 1.8 | 2.5 | mA |
| $V_{FLOAT}$ | BATSNS Regulated Output Voltage Selected by I²C Control. Switching Modes | 3.45V Setting (Default) | ● | 3.42 | 3.45 | 3.48 | V |
| | | 3.55V Setting | ● | 3.52 | 3.55 | 3.58 | V |
| | | 3.60V Setting | ● | 3.57 | 3.60 | 3.63 | V |
| | | 3.80V Setting | ● | 3.77 | 3.80 | 3.83 | V |
| $I_{CHARGE}$ | Regulated Battery Charge Current Selected by I²C Control | 12.50% Charge Current Mode | | 290 | 315 | 340 | mA |
| | | 18.75% Charge Current Mode | | 430 | 465 | 500 | mA |
| | | 25.00% Charge Current Mode | | 590 | 620 | 650 | mA |
| | | 31.25% Charge Current Mode | | 730 | 770 | 810 | mA |
| | | 37.50% Charge Current Mode | | 880 | 925 | 970 | mA |
| | | 43.75% Charge Current Mode | | 1025 | 1075 | 1125 | mA |
| | | 50.00% Charge Current Mode | | 1180 | 1230 | 1280 | mA |
| | | 56.25% Charge Current Mode | | 1330 | 1385 | 1440 | mA |
| | | 62.50% Charge Current Mode | | 1485 | 1535 | 1585 | mA |
| | | 68.75% Charge Current Mode | | 1635 | 1685 | 1735 | mA |
| | | 75.00% Charge Current Mode | | 1780 | 1835 | 1890 | mA |
| | | 81.25% Charge Current Mode | | 1915 | 1980 | 2045 | mA |
| | | 87.50% Charge Current Mode | | 2065 | 2130 | 2195 | mA |
| | | 93.75% Charge Current Mode | | 2210 | 2280 | 2350 | mA |
| | | 100.0% Charge Current Mode (Default) | | 2350 | 2430 | 2500 | mA |
| $I_{CHARGE(MAX)}$ | Regulated Battery Charge Current | 100.0% Charge Current Mode, $R_{PROG}$ = 340Ω | | 3.44 | 3.57 | 3.70 | A |
| $V_{OUT}$ | PowerPath Regulated Output Voltage ($V_{BUS}$ Power Available) | Suspend Mode, $I_{VOUT}$ = 1mA | | | 4.35 | 4.5 | V |
| | | Battery Charger Enabled, Charging, BATSNS ≥ 3.19V | | | BATSNS | | V |
| | | Battery Charger Terminated or Battery Charger Disabled | | | 4.35 | 4.5 | V |
| $V_{OUT(MIN)}$ | Low Battery Instant-On Output Voltage ($V_{BUS}$ Power Available) | Battery Charger Enabled, Charging, BATSNS ≤ 3.0V | | 3.10 | 3.19 | | V |

## ELECTRICAL CHARACTERISTICS

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| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $I_{VOUT}$ | $V_{OUT}$ Current Available Before Loading Battery | 2.5mA $I_{VBUS}$ Mode (USB Suspend) | | 1 | 1.3 | | mA |
| | | 100mA $I_{VBUS}$ Mode, BAT = 3.3V | | | 76 | | mA |
| | | 500mA $I_{VBUS}$ Mode, BAT = 3.3V | | | 673 | | mA |
| | | 600mA $I_{VBUS}$ Mode, BAT = 3.3V | | | 810 | | mA |
| | | 700mA $I_{VBUS}$ Mode, BAT = 3.3V | | | 944 | | mA |
| | | 800mA $I_{VBUS}$ Mode, BAT = 3.3V | | | 1093 | | mA |
| | | 900mA $I_{VBUS}$ Mode, BAT = 3.3V | | | 1200 | | mA |
| | | 1.00A $I_{VBUS}$ Mode, BAT = 3.3V | | | 1397 | | mA |
| | | 1.25A $I_{VBUS}$ Mode, BAT = 3.3V | | | 1728 | | mA |
| | | 1.50A $I_{VBUS}$ Mode, BAT = 3.3V | | | 2072 | | mA |
| | | 1.75A $I_{VBUS}$ Mode, BAT = 3.3V | | | 2411 | | mA |
| | | 2.00A $I_{VBUS}$ Mode, BAT = 3.3V | | | 2700 | | mA |
| | | 2.25A $I_{VBUS}$ Mode, BAT = 3.3V | | | 2846 | | mA |
| | | 2.50A $I_{VBUS}$ Mode, BAT = 3.3V | | | 3154 | | mA |
| | | 2.75A $I_{VBUS}$ Mode, BAT = 3.3V | | | 3408 | | mA |
| | | 3.00A $I_{VBUS}$ Mode, BAT = 3.3V | | | 3657 | | mA |
| $V_{PROG}$ | PROG Pin Servo Voltage | 12.50% Charge Current Mode | | | 150 | | mV |
| | | 18.75% Charge Current Mode | | | 225 | | mV |
| | | 25.00% Charge Current Mode | | | 300 | | mV |
| | | 31.25% Charge Current Mode | | | 375 | | mV |
| | | 37.50% Charge Current Mode | | | 450 | | mV |
| | | 43.75% Charge Current Mode | | | 525 | | mV |
| | | 50.00% Charge Current Mode | | | 600 | | mV |
| | | 56.25% Charge Current Mode | | | 675 | | mV |
| | | 62.50% Charge Current Mode | | | 750 | | mV |
| | | 68.75% Charge Current Mode | | | 825 | | mV |
| | | 75.00% Charge Current Mode | | | 900 | | mV |
| | | 81.25% Charge Current Mode | | | 975 | | mV |
| | | 87.50% Charge Current Mode | | | 1050 | | mV |
| | | 93.75% Charge Current Mode | | | 1125 | | mV |
| | | 100.0% Charge Current Mode (Default) | | | 1200 | | mV |
| $V_{RECHRG}$ | Recharge Battery Threshold Voltage | Threshold Voltage Relative to $V_{FLOAT}$ | | 96.6 | 97.6 | 98.4 | % |
| $t_{TERMINATE}$ | Safety Timer Termination Period Selected by $I^2C$ Control. Timer Starts When BATSNS ≥ $V_{FLOAT}$ | 0.25-Hour Mode | | 0.23 | 0.27 | 0.30 | Hours |
| | | 0.5-Hour Mode | | 0.47 | 0.53 | 0.59 | Hours |
| | | 1-Hour Mode (Default) | | 0.95 | 1.06 | 1.17 | Hours |
| | | 4-Hour Mode | | 3.81 | 4.24 | 4.66 | Hours |
| $V_{LOWBAT}$ | Threshold Voltage | Rising Threshold | | 2.65 | 2.8 | 2.95 | V |
| | | Hysteresis | | | 130 | | mV |
| $t_{BADBAT}$ | Bad Battery Termination Time | BATSNS < ($V_{LOWBAT} - \Delta V_{LOWBAT}$) | | 0.47 | 0.53 | 0.59 | Hours |
| $V_{C/x}$ | Full Capacity Charge Indication PROG Voltage Selected by $I^2C$ Control | C/10 Mode ($I_{CHARGE}$ = 10%FS) (Default) | | 110 | 120 | 130 | mV |
| | | C/5 Mode ($I_{CHARGE}$ = 20%FS) | | 230 | 240 | 250 | mV |
| | | C/20 Mode ($I_{CHARGE}$ = 5%FS) | | 15 | 24 | 33 | mV |
| | | C/50 Mode ($I_{CHARGE}$ = 2%FS) | | 50 | 60 | 70 | mV |
| $h_{PROG}$ | Ratio of $I_{CHGSNS}$ to PROG Pin Current | | | | 1000 | | mA/mA |
| $h_{CLPROG1}$ (Note 4) | Ratio of Measured $V_{BUS}$ Current to CLPROG1 Sense Current | CLPROG1 $I_{VBUS}$ Mode | | | 990 | | mA/mA |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A \approx T_J$ = 25°C (Note 2). $V_{BUS}$ = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1} = R_{CLPROG2}$ = 1.21k, $R_{PROG}$ = 499Ω, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $h_{CLPROG2}$ (Note 4) | Ratio of Measured $V_{BUS}$ Current to CLPROG2 Sense Current | 2.5mA $I_{VBUS}$ Mode (USB Suspend)<br>100mA $I_{VBUS}$ Mode<br>500mA $I_{VBUS}$ Mode<br>600mA $I_{VBUS}$ Mode<br>700mA $I_{VBUS}$ Mode<br>800mA $I_{VBUS}$ Mode<br>900mA $I_{VBUS}$ Mode<br>1.00A $I_{VBUS}$ Mode<br>1.25A $I_{VBUS}$ Mode<br>1.50A $I_{VBUS}$ Mode<br>1.75A $I_{VBUS}$ Mode<br>2.00A $I_{VBUS}$ Mode<br>2.25A $I_{VBUS}$ Mode<br>2.50A $I_{VBUS}$ Mode<br>2.75A $I_{VBUS}$ Mode<br>3.00A $I_{VBUS}$ Mode | | | 19<br>79<br>466<br>557<br>657<br>758<br>839<br>990<br>1222<br>1494<br>1746<br>1999<br>2175<br>2477<br>2730<br>2956 | | mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA<br>mA/mA |
| $V_{CLPROG1}$ | CLPROG1 Servo Voltage in Current Limit | CLPROG1 $I_{VBUS}$ Mode | | | 1.2 | | V |
| $V_{CLPROG2}$ | CLPROG2 Servo Voltage in Current Limit | 2.5mA $I_{VBUS}$ Mode (USB Suspend)<br>100mA – 3A $I_{VBUS}$ Modes | | | 103<br>1.2 | | mV<br>V |
| $f_{OSC}$ | Switching Frequency | | | 2.05 | 2.25 | 2.50 | MHz |
| $R_{PMOS}$ | High Side Switch On Resistance | | | | 0.090 | | Ω |
| $R_{NMOS}$ | Low Side Switch On Resistance | | | | 0.080 | | Ω |
| $R_{CHG}$ | Battery Charger Current Sense Resistance | | | | 0.040 | | Ω |
| $I_{PEAK}$ | Peak Inductor Current Clamp | 500mA – 3A $I_{VBUS}$ Modes | | | 6.7 | | A |
| **Step-Up Mode PowerPath Switching Regulator (USB On-The-Go)** | | | | | | | |
| $V_{BUS}$ | Output Voltage | 0mA ≤ $I_{VBUS}$ ≤ 500mA | | 4.75 | | 5.25 | V |
| $V_{OUT}$ | Input Voltage | | | 2.9 | | | V |
| $I_{VBUSOTG}$ | Output Current Limit | | | | 1.4 | | A |
| $I_{VOUTOTGQ}$ | $V_{OUT}$ Quiescent Current | $I_{VBUS}$ = 0mA | | | 1.96 | | mA |
| $V_{CLPROG2}$ | Output Current Limit Servo Voltage | | | | 1.2 | | V |
| $V_{BATSNSUVLO}$ | $V_{BATSNS}$ Undervoltage Lockout | $V_{BATSNS}$ Falling<br>Hysteresis | | 2.65 | 2.8<br>130 | 2.95 | V<br>mV |
| $t_{SCFAULT}$ | Short-Circuit Fault Delay | $V_{BUS}$ < 4V | | | 7.2 | | ms |
| **Overvoltage Protection, Priority Multiplexer and Undervoltage Lockout; USB Input Connected to USBSNS Through 3.6k Resistor; WALL Input Connected to WALLSNS Through 3.6k Resistor** | | | | | | | |
| $V_{UVLO}$ | USB Input, Wall Input Undervoltage Lockout | Rising Threshold<br>Falling Threshold<br>Hysteresis | | 4.05<br>3.90 | <br><br>100 | 4.45<br>4.25 | V<br>V<br>mV |
| $V_{DUVLO}$ | USB Input, Wall Input to BATSNS Differential Undervoltage Lockout | Rising Threshold<br>Falling Threshold<br>Hysteresis | | 100<br>50 | <br><br>70 | 425<br>375 | mV<br>mV<br>mV |
| $V_{OVLO}$ | USB Input, Wall Input Overvoltage Protection Threshold | Rising Threshold | | 5.75 | 6.0 | 6.3 | V |
| $V_{USBGTACTV}$ | USBGT Output Voltage Active | USBSNS < $V_{USBOVLO}$ | | | 2 • $V_{USBSNS}$ | | V |
| $V_{WALLGTACTV}$ | WALLGT Output Voltage Active | WALLSNS < $V_{WALLOVLO}$ | | | 2 • $V_{WALLSNS}$ | | V |

## ELECTRICAL CHARACTERISTICS

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| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{USBGTPROT}$ | USBGT Output Voltage Protected | USBSNS > $V_{USBOVLO}$ | | | 0 | | V |
| $V_{WALLGTPROT}$ | WALLGT Output Voltage Protected | WALLSNS > $V_{WALLOVLO}$ | | | 0 | | V |
| $V_{USBGTLOAD}$, $V_{WALLGTLOAD}$ | USBGT, WALLGT Voltage Under Load | 5V Through 3.6k into WALLSNS, USBSNS, $I_{USBGT}$, $I_{WALLGT}$ = 1µA | | 8.4 | 8.9 | | V |
| $I_{USBSNSQ}$ | USBSNS Quiescent Current | $V_{USBSNS}$ = 5V, $V_{USBSNS}$ > $V_{WALLSNS}$<br>$V_{USBSNS}$ = 5V, $V_{WALLSNS}$ > $V_{USBSNS}$ | | | 27<br>54 | | µA<br>µA |
| $I_{WALLSNSQ}$ | WALLSNS Quiescent Current | $V_{WALLSNS}$ = 5V, $V_{WALLSNS}$ > $V_{USBSNS}$<br>$V_{WALLSNS}$ = 5V, $V_{USBSNS}$ > $V_{WALLSNS}$ | | | 27<br>54 | | µA<br>µA |
| $t_{RISE}$ | OVGCAP Time to Reach Regulation | $C_{OVGCAP}$ = 1nF | | | 1.2 | | ms |
| **$\overline{IRQ}$ Pin Characteristics** | | | | | | | |
| $I_{\overline{IRQ}}$ | $\overline{IRQ}$ Pin Leakage Current | $V_{\overline{IRQ}}$ = 5V | | | | 1 | µA |
| $V_{\overline{IRQ}}$ | $\overline{IRQ}$ Pin Output Low Voltage | $I_{\overline{IRQ}}$ = 5mA | | | 75 | 100 | mV |
| **ID Pin Characteristics** | | | | | | | |
| $I_{ID}$ | ID Pin Pull-Up Current | $V_{ID}$ = 0V | | 35 | 55 | 85 | µA |
| $V_{ID_OTG}$ | ID Pin Threshold Voltage | ID Pin Falling<br>Hysteresis | | 0.5 | 0.86<br>0.2 | 0.95 | V<br>V |
| **Thermistor Measurement System** | | | | | | | |
| $\kappa_{OFFSET}$ | $V_{NTC}$ / $V_{NTCBIAS}$ A/D Lower Range End | $V_{NTC}$ / $V_{NTCBIAS}$ Ratio Below Which Only 0x00 Is Returned | | | 0.113 | | V/V |
| $\kappa_{HIGH}$ | $V_{NTC}$ / $V_{NTCBIAS}$ A/D Upper Range End | $V_{NTC}$ / $V_{NTCBIAS}$ Ratio Above Which Only 0x7F Is Returned | | | 0.895 | | V/V |
| $\kappa_{SPAN}$ | A/D Span Coefficient (Decimal Format) | | | 6.091 | 6.162 | 6.191 | mV/V/ LSB |
| $d_{TOO_COLD}$ | NTCVAL at NTC_TOO_COLD (Decimal Format) | Warning Threshold<br>Reset Threshold | | 102<br>98 | 102<br>98 | 102<br>98 | Count<br>Count |
| $d_{HOT_FAULT}$ | NTCVAL at HOT_FAULT (Decimal Format) | Fault Threshold<br>Reset Threshold | | 19<br>23 | 19<br>23 | 19<br>23 | Count<br>Count |
| $I_{NTC}$ | NTC Leakage Current | | | –100 | | 100 | nA |
| **Ideal Diode** | | | | | | | |
| $V_{FWD}$ | Forward Voltage Detection | Input Power Available, Battery Charger Off | | | 15 | | mV |
| **$I^2C$ Port** | | | | | | | |
| DVCC | $I^2C$ Logic Reference Level | (Note 3) | | 1.7 | | $V_{MAX}$ | V |
| $I_{DVCCQ}$ | DVCC Current | SCL/SDA = 0kHz | | | 0.25 | | µA |
| $V_{DVCC_UVLO}$ | DVCC UVLO | | | | 1.0 | | V |
| ADDRESS | $I^2C$ Address | | | | 0001_001[R/$\overline{W}$]b | | |
| $V_{IH,SDA,SCL}$ | Input High Threshold | | | 70 | | | % DVCC |
| $V_{IL,SDA,SCL}$ | Input Low Threshold | | | | | 30 | % DVCC |
| $I_{IH,SDA,SCL}$ | Input Leakage High | SDA, SCL = DVCC | | –1 | | 1 | µA |
| $I_{IL,SDA,SCL}$ | Input Leakage Low | SDA, SCL = 0V | | –1 | | 1 | µA |
| $V_{OL}$ | Digital Output Low (SDA) | $I_{SDA}$ = 3mA | | | | 0.4 | V |
| $f_{SCL}$ | Clock Operating Frequency | | | | | 400 | kHz |
| $t_{BUF}$ | Bus Free Time Between STOP and START Condition | | | 1.3 | | | µs |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A \approx T_J$ = 25°C (Note 2). $V_{BUS}$ = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1} = R_{CLPROG2}$ = 1.21k, $R_{PROG}$ = 499Ω, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{HD_SDA}$ | Hold Time After (Repeated) START Condition | | | 0.6 | | | µs |
| $t_{SU_SDA}$ | Repeated START Condition Set-Up Time | | | 0.6 | | | µs |
| $t_{SU_STO}$ | STOP Condition Time | | | 0.6 | | | µs |
| $t_{HD_DAT(OUT)}$ | Data Hold Time | | | 0 | | 900 | ns |
| $t_{HD_DAT(IN)}$ | Input Data Hold Time | | | 0 | | | ns |
| $t_{SU_DAT}$ | Data Set-Up Time | | | 100 | | | ns |
| $t_{LOW}$ | Clock LOW Period | | | 1.3 | | | µs |
| $t_{HIGH}$ | Clock HIGH Period | | | 0.6 | | | µs |
| $t_f$ | Clock Data Fall Time | | | 20 | | 300 | ns |
| $t_r$ | Clock Data Rise Time | | | 20 | | 300 | ns |
| $t_{SP}$ | Spike Suppression Time | | | | | 50 | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC4156E is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC4156E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC4156I is guaranteed over the full –40°C to 125°C operating junction temperature range. The junction temperature ($T_J$, in °C) is calculated from the ambient temperature ($T_A$, in °C) and power dissipation ($P_D$, in watts) according to the formula:

$T_J = T_A + (P_D \bullet \theta_{JA})$, where the package thermal impedance $\theta_{JA}$ = 43°C/W)

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

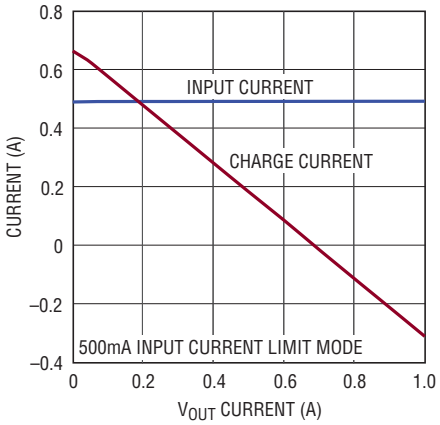
**Note 3.** $V_{MAX}$ is the maximum of $V_{BUS}$ or BATSNS

**Note 4.** Total input current is $I_{VBUSQ} + V_{CLPROG}/R_{CLPROG} \bullet (h_{CLPROG} + 1)$.

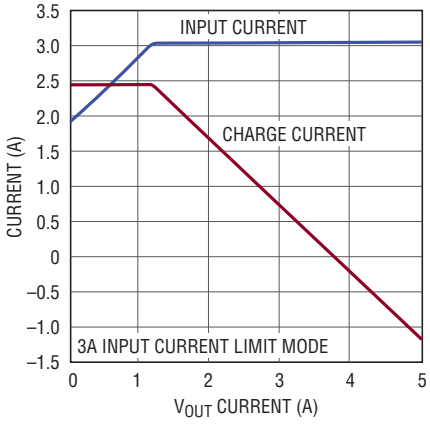
## TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C (Note 2). $V_{BUS}$ = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1}$ = $R_{CLPROG2}$ = 1.21k, $R_{PROG}$ = 499Ω, unless otherwise noted.**

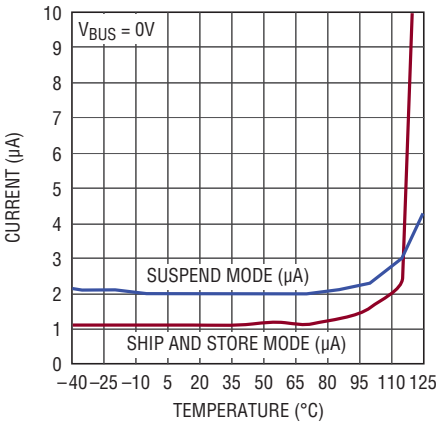
### Battery and $V_{BUS}$ Currents vs $V_{OUT}$ Current



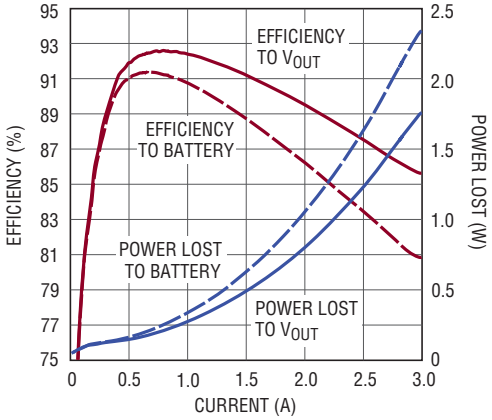

### Battery and $V_{BUS}$ Currents vs $V_{OUT}$ Current



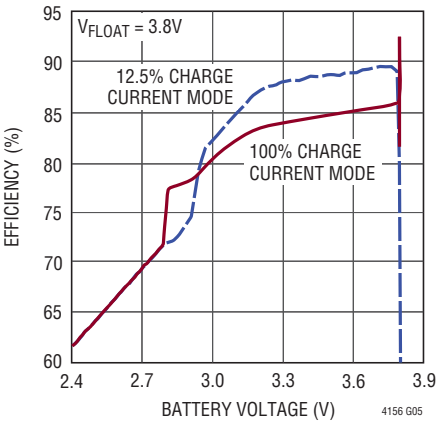

### Battery Drain Current vs Temperature




### Switching Regulator Efficiency

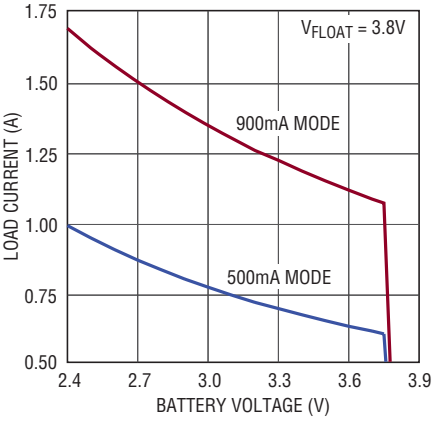



### Battery Charger Total Efficiency vs Battery Voltage

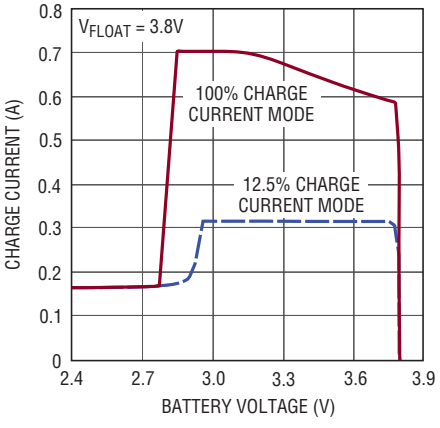



INCLUDES LOSSES FROM 2× Si7938DP OVP FETS
XFL4020-102ME INDUCTOR AND Si5481DU CHARGER FET

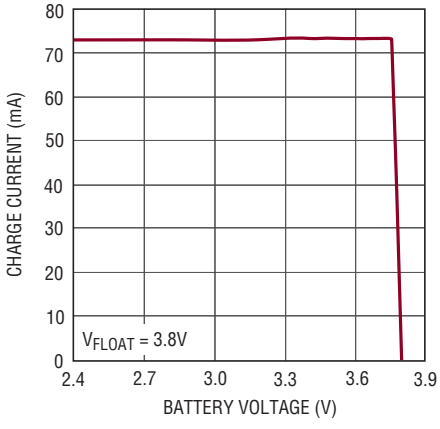
### USB Compliant Load Current Available Before Discharging Battery



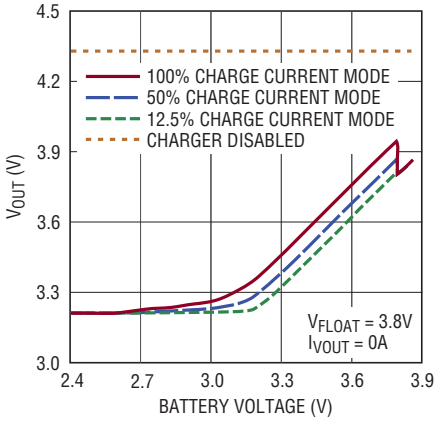

### 500mA USB Limited Battery Charge Current vs Battery Voltage




### 100mA USB Limited Battery Charge Current vs Battery Voltage



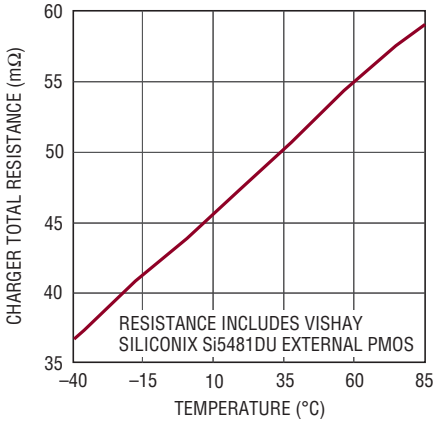

### $V_{OUT}$ Voltage vs Battery Voltage



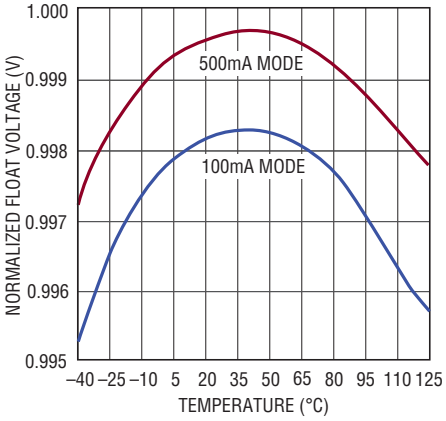
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C (Note 2). $V_{BUS}$ = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1}$ = $R_{CLPROG2}$ = 1.21k, $R_{PROG}$ = 499Ω, unless otherwise noted.

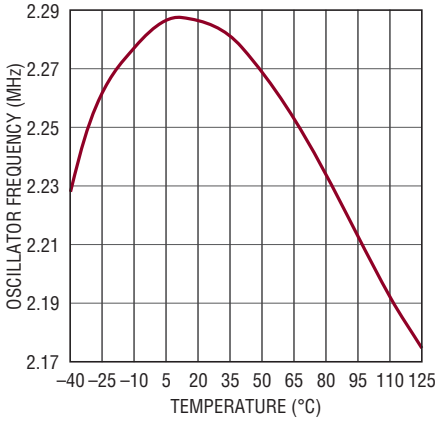
### Battery Charger Resistance vs Temperature



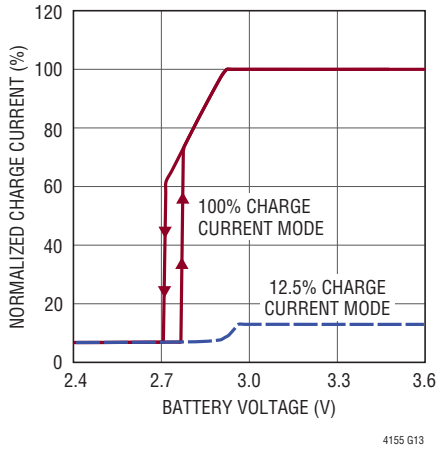

### Normalized Float Voltage vs Temperature



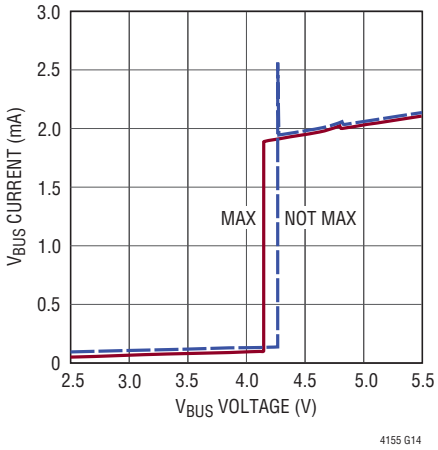

### Oscillator Frequency vs Temperature



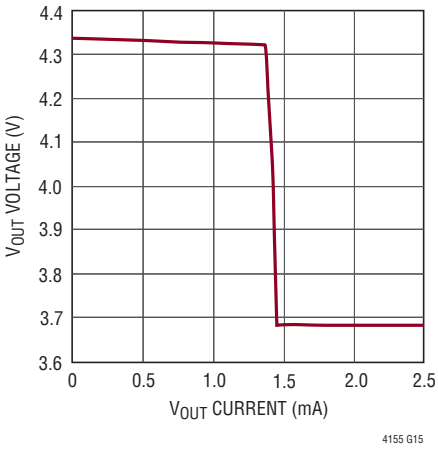

### Automatic Charge Current Reduction vs Battery Voltage



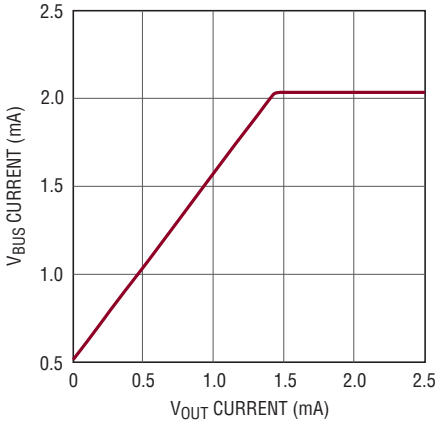

### $V_{BUS}$ Current vs $V_{BUS}$ Voltage in USB Suspend Mode



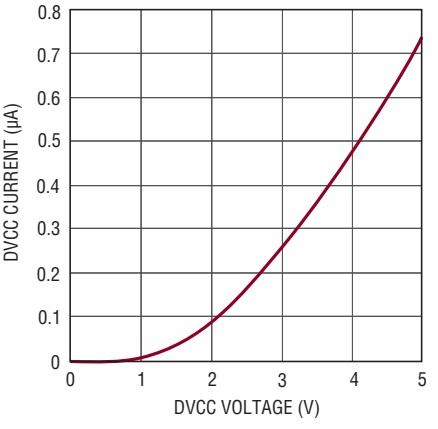

### $V_{OUT}$ Voltage vs $V_{OUT}$ Current in USB Suspend Mode



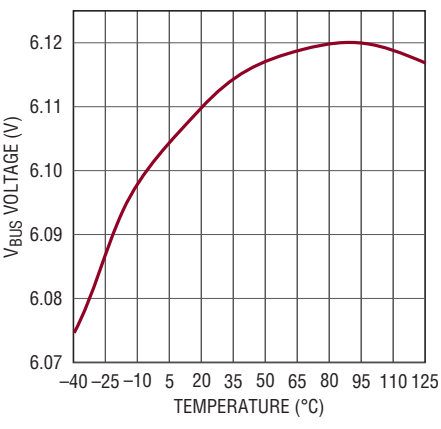

### $V_{BUS}$ Current vs $V_{OUT}$ Current in USB Suspend Mode




### Static DVCC Current vs DVCC Voltage



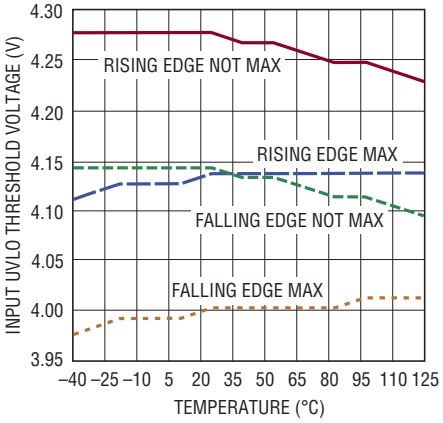

### Rising Overvoltage Lockout Threshold vs Temperature



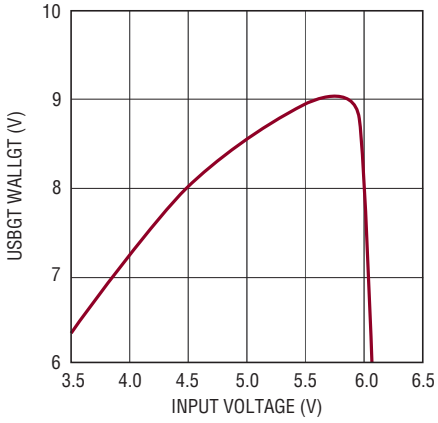
## TYPICAL PERFORMANCE CHARACTERISTICS

**$T_A$ = 25°C (Note 2). $V_{BUS}$ = 5V, BATSNS = 3.3V, DVCC = 3.3V, $R_{CLPROG1}$ = $R_{CLPROG2}$ = 1.21k, $R_{PROG}$ = 499Ω, unless otherwise noted.**

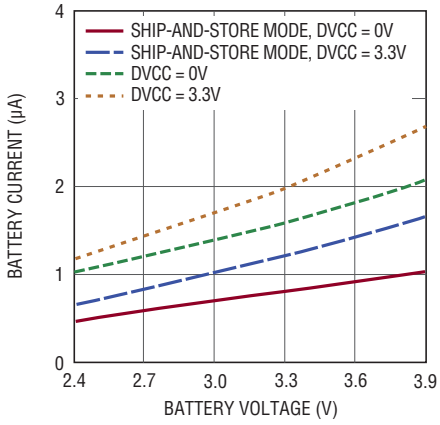
### Undervoltage Lockout Thresholds vs Temperature



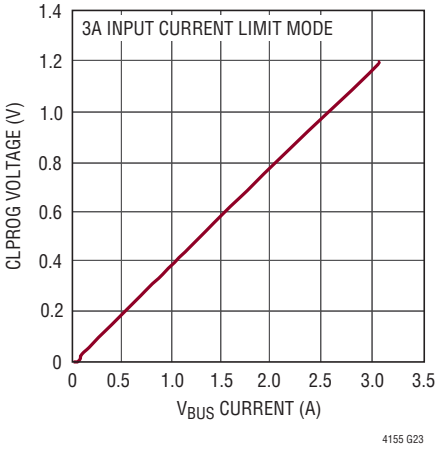

### OVP Charge Pump Output vs Input Voltage



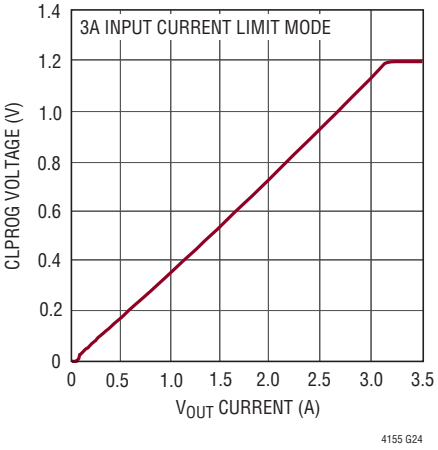

### Battery Drain Current vs Battery Voltage



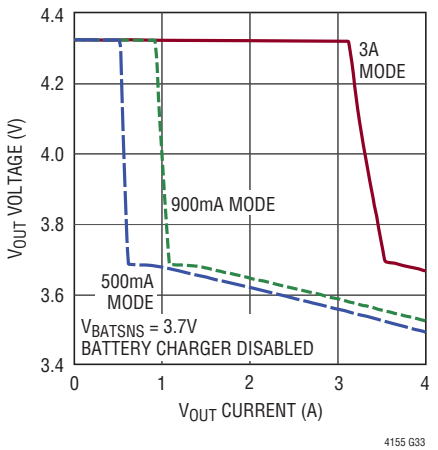

### CLPROG Voltage vs $V_{BUS}$ Current




### CLPROG Voltage vs $V_{OUT}$ Current




### $V_{OUT}$ Voltage vs $V_{OUT}$ Current



## PIN FUNCTIONS

**SDA (Pin 1):** Data Input/Output for the $I^2C$ Serial Port. The $I^2C$ input levels are scaled with respect to DVCC for $I^2C$ compliance.

**DVCC (Pin 2):** Logic Supply for the $I^2C$ Serial Port. DVCC sets the reference level of the SDA and SCL pins for $I^2C$ compliance. It should be connected to the same power supply used to power the $I^2C$ pull-up resistors.

**$\overline{IRQ}$ (Pin 3):** Open-Drain Interrupt Output. The $\overline{IRQ}$ pin can be used to generate an interrupt due to a variety of maskable status change events within the LTC4156.

**ID (Pin 4):** USB A-Device Detection Pin. When wired to a mini- or micro-USB connector, the ID pin detects when the "A" side of a mini or micro-USB cable is connected to the product. If the ID pin is pulled down, and the LOCKOUT_ID_PIN bit is not set in the $I^2C$ port, the switching PowerPath operates in reverse providing USB power to the $V_{BUS}$ pin from the battery. USB On-The-Go power can only be delivered from the USB multiplexer path.

**CLPROG1 (Pin 5):** Primary $V_{BUS}$ Current Limit Programming Pin. A resistor from CLPROG1 to ground determines the upper limit of the current drawn from the $V_{BUS}$ pin when CLPROG1 is selected. A precise measure of $V_{BUS}$ current, $h_{CLPROG1}^{-1}$, is sent to the CLPROG1 pin. The switching regulator increases power delivery until CLPROG1 reaches 1.2V. Therefore, the current drawn from $V_{BUS}$ will be limited to an amount given by the 1.2V reference voltage, $h_{CLPROG1}$ and $R_{CLPROG1}$.

Typically CLPROG1 is used to override the USB compliant input current control pin, CLPROG2, in applications where USB compliance is not a requirement. This would be useful for applications that use a dedicated wall adapter and would rather not be limited to the 500mW start-up value required by USB specifications. If USB compliance is a requirement at start-up, CLPROG1 should be connected to CLPROG2 and a single resistor should be used. See the CLPROG2 pin description.

In USB noncompliant designs, the user is encouraged to use an $R_{CLPROG1}$ value that best suits their application for start-up current limit. See the Operation section for more details.

**CLPROG2 (Pin 6):** Secondary $V_{BUS}$ Current Limit Program Pin. CLPROG2 controls the $V_{BUS}$ current limit when either selected via $I^2C$ command or when CLPROG1 and CLPROG2 are shorted together. When selected, a resistor from CLPROG2 to ground determines the upper limit of the current drawn from the $V_{BUS}$ pin. Like CLPROG1, a precise fraction of $V_{BUS}$ current, $h_{CLPROG2}^{-1}$, is sent to the CLPROG2 pin. The switching regulator increases power delivery until CLPROG2 reaches 1.2V. Therefore, the current drawn from $V_{BUS}$ will be limited to an amount given by the 1.2V reference voltage, $h_{CLPROG2}$ and $R_{CLPROG2}$.

There are a multitude of ratios for $h_{CLPROG2}$ available by $I^2C$ control, three of which correspond to the 100mA, 500mA and 900mA USB specifications. CLPROG2 is also used to regulate maximum input current in the USB suspend mode and maximum output current in USB On-The-Go mode.

If CLPROG1 and CLPROG2 are shorted together at the onset of available input power, the LTC4156 selects CLPROG2 in the 100mA USB mode to limit input current. This ensures USB compliance if so desired. For USB compliance in all modes, the user is encouraged to make $R_{CLPROG2}$ equal to the value declared in the Electrical Characteristics.

**WALLSNS (Pin 7):** Highest Priority Multiplexer Input and Overvoltage Protection Sense Input. WALLSNS should be connected through a 3.6k resistor to a high priority input power connector and one drain of two source-connected N-channel MOSFET pass transistors. When voltage is detected on WALLSNS, it draws a small amount of current to power a charge pump which then provides gate drive to WALLGT to energize the external transistors. If the input voltage exceeds $V_{OVLO}$, WALLGT will be pulled to GND to disable the pass transistors and protect the LTC4156 from high voltage.

**USBSNS (Pin 8):** Lowest Priority Multiplexer Input and Overvoltage Protection Sense Input. USBSNS should be connected through a 3.6k resistor to a low priority input power connector and one drain of two source-connected N-channel MOSFET pass transistors. When voltage is detected on USBSNS, and no voltage is detected on WALLSNS, USBSNS draws a small amount of current to power a charge pump which then provides gate drive to

## PIN FUNCTIONS

USBGT to energize the external transistors. If the input voltage exceeds $V_{OVLO}$, USBGT will be pulled to GND to disable the pass transistors and protect the LTC4156 from high voltage.

Power detected on WALLSNS is prioritized over USBSNS. If power is detected on both WALLSNS and USBSNS, by default, only WALLGT will receive drive for its pass transistors. See the Operations section for further information about programmable priority.

**USBGT (Pin 9):** Overvoltage Protection and Priority Multiplexer Gate Output. Connect USBGT to the gate pins of two source-connected external N-channel MOSFET pass transistors. One drain of the transistors should be connected to $V_{BUS}$ and the other drain should be connected to a low priority DC input connector. In the absence of an overvoltage condition, this pin is driven from an internal charge pump capable of creating sufficient overdrive to fully enhance the pass transistors. If an overvoltage condition is detected, USBGT is brought rapidly to GND to prevent damage to the LTC4156. USBGT works in conjunction with USBSNS to provide this protection. USBGT also works in conjunction with WALLSNS to determine power source prioritization. See the Operation section.

**OVGCAP (Pin 10):** Overvoltage Protection Capacitor Output. A 0.1µF capacitor should be connected from OVGCAP to GND. OVGCAP is used to store charge so that it can be rapidly moved to WALLGT or USBGT. This feature provides faster power switchover when multiple inputs are supported by the end product.

**WALLGT (Pin 9):** Overvoltage Protection and Priority Multiplexer Gate Output. Connect WALLGT to the gate pins of two source-connected external N-channel MOSFET pass transistors. One drain of the transistors should be connected to $V_{BUS}$ and the other drain should be connected to a high priority input connector. In the absence of an overvoltage condition, this pin is driven from an internal charge pump capable of creating sufficient gate drive to fully enhance the pass transistors. If an overvoltage condition is detected, WALLGT is brought rapidly to GND to prevent damage to the LTC4156. WALLGT works in conjunction with WALLSNS to provide this protection. WALLGT also works in conjunction with USBSNS to determine power source prioritization. See the Operation section.

**$V_C$ (Pin 12):** Compensation Pin. A 0.047µF ceramic capacitor on this pin compensates the switching regulator control loops.

**$V_{OUTSNS}$ (Pin 13):** Output Voltage Sense Input. Connecting $V_{OUTSNS}$ directly to the $V_{OUT}$ bypass capacitor ensures that $V_{OUT}$ regulates at the correct level.

**NTCBIAS (Pin 14):** NTC Thermistor Bias Output. Connect a bias resistor between NTCBIAS and NTC, and a thermistor between NTC and GND. The value of the bias resistor should usually be equal to the nominal value of the thermistor.

**NTC (Pin 15):** Input to the Negative Temperature Coefficient Thermistor Monitoring Circuit. The NTC pin connects to a negative temperature coefficient thermistor, which is typically copackaged with the battery, to determine if the battery is too cold to charge or if the battery is dangerously hot. If the battery's temperature is out of range, charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground. The thermistor's temperature reading is continually digitized by an analog-to-digital converter and may be read back at any time via the $I^2C$ port.

**BATSNS (Pin 16):** Battery Voltage Sense Input. For proper operation, this pin must always be connected to the battery. For fastest charging, connect BATSNS physically close to the lithium iron phosphate cell's positive terminal. Depending upon available power and load, a $LiFePO_4$ battery connected to the BATSNS pin will either be charged from $V_{OUT}$ or will deliver system power to $V_{OUT}$ via the required external P-channel MOSFET transistor.

**BATGATE (Pin 17):** Battery Charger and Ideal Diode Amplifier Control Output. This pin controls the gate of an external P-channel MOSFET transistor used to charge the $LiFePO_4$ cell and to provide power to $V_{OUT}$ when the system load exceeds available input power. The source of the P-channel MOSFET should be connected to CHGSNS and the drain should be connected to BATSNS and the battery.

## PIN FUNCTIONS

**PROG (Pin 18):** Charge Current Program and Monitor Pin. A resistor from PROG to GND programs the maximum battery charge rate. The LTC4156 features I²C programmability enabling software selection of fifteen charge currents that are inversely proportional to a single user-supplied programming resistor.

**CHGSNS (Pins 19, 20):** Battery Charger Current Sense Pin. An internal current sense resistor between $V_{OUT}$ and CHGSNS monitors battery charge current. CHGSNS should be connected to the source of an external P-channel MOSFET transistor.

**$V_{OUT}$ (Pins 21, 22):** Output Voltage of the Switching PowerPath Controller and Input Voltage of the Battery Charging System. The majority of the portable product should be powered from $V_{OUT}$. The LTC4156 will partition the available power between the external load on $V_{OUT}$ and the battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode control function from BATSNS to $V_{OUT}$ ensures that $V_{OUT}$ is powered even if the load exceeds the allotted power from $V_{BUS}$ or if the $V_{BUS}$ power source is removed. $V_{OUT}$ should be bypassed with a low impedance multilayer ceramic capacitor of at least 22µF.

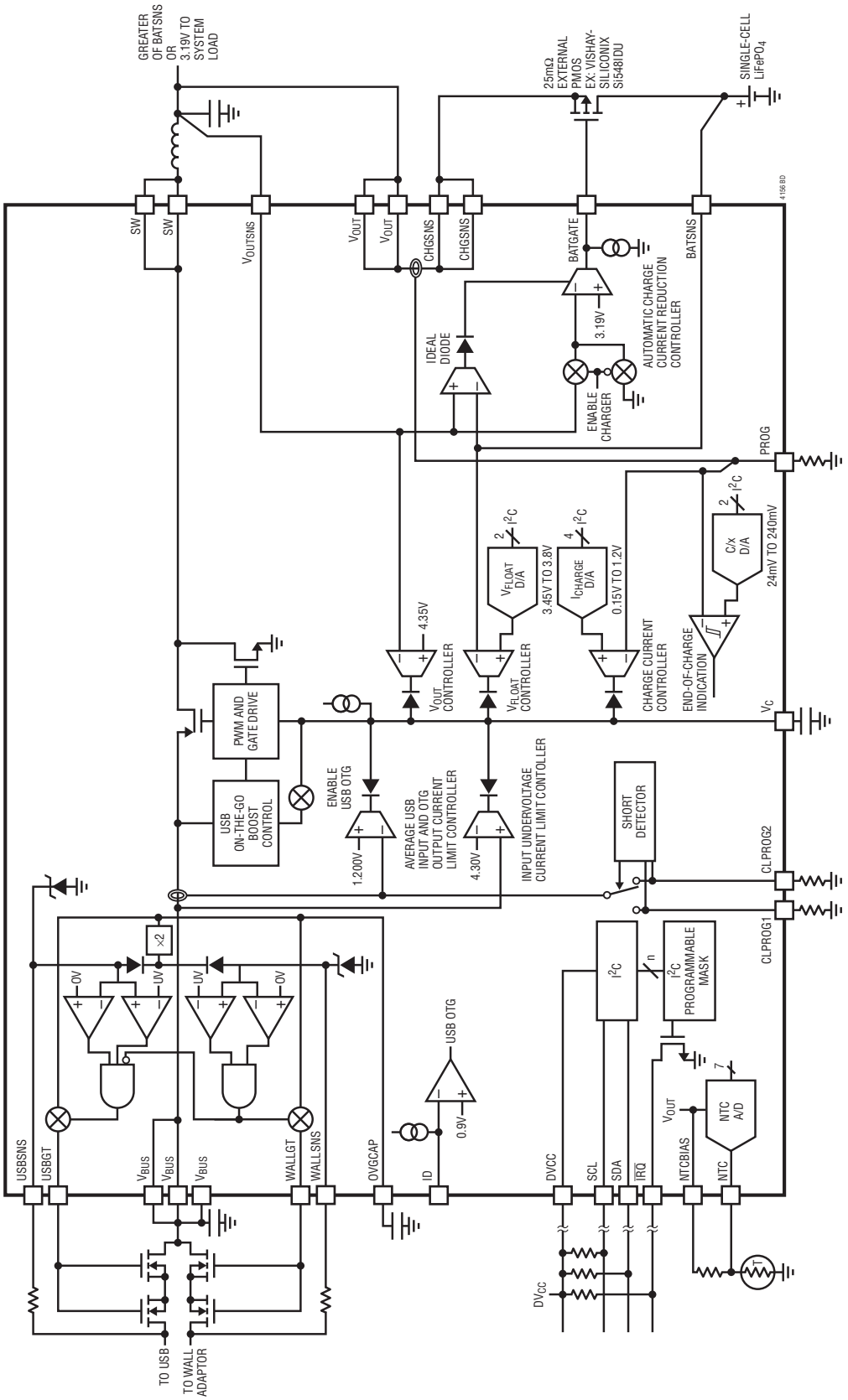
**$V_{BUS}$ (Pins 23, 24, 25):** Input Voltage for the PowerPath Step-Down Switching Regulator and Output Voltage for the USB On-The-Go Step-Up Switching Regulator. $V_{BUS}$ may be connected to the USB port of a computer or a DC output wall adapter or to one or both optional overvoltage protection/multiplexer compound transistors. $V_{BUS}$ should be bypassed with a low impedance multilayer ceramic capacitor.

**SW (Pins 26, 27):** Switching Regulator Power Transmission Pin. The SW pin delivers power from $V_{BUS}$ to $V_{OUT}$ via the step-down switching regulator and from $V_{OUT}$ to $V_{BUS}$ via the step-up switching regulator. A 1µH inductor should be connected from SW to $V_{OUT}$. See the Applications Information section for a discussion of current rating.

**SCL (Pin 28):** Clock Input for the I²C Serial Port. The I²C input levels are scaled with respect to DVCC for I²C compliance.

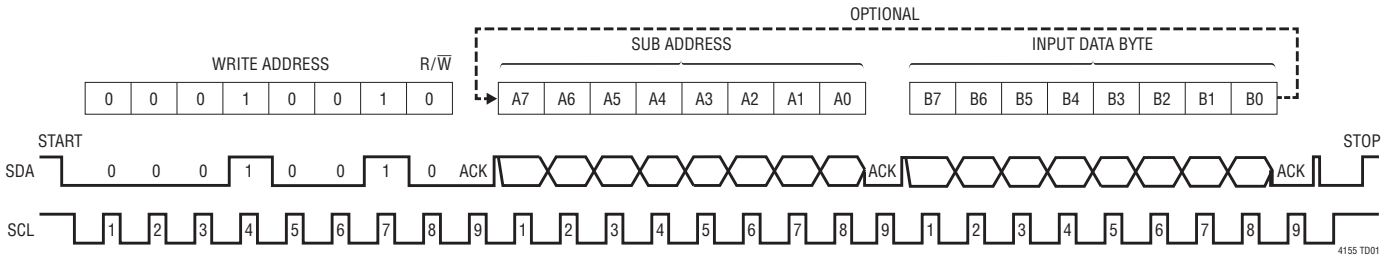
**GND (Exposed Pad Pin 29):** The exposed pad must be soldered to the PCB to provide a low electrical and thermal impedance connection to the printed circuit board's ground. A continuous ground plane on the second layer of a multilayer printed circuit board is strongly recommended.

## BLOCK DIAGRAM

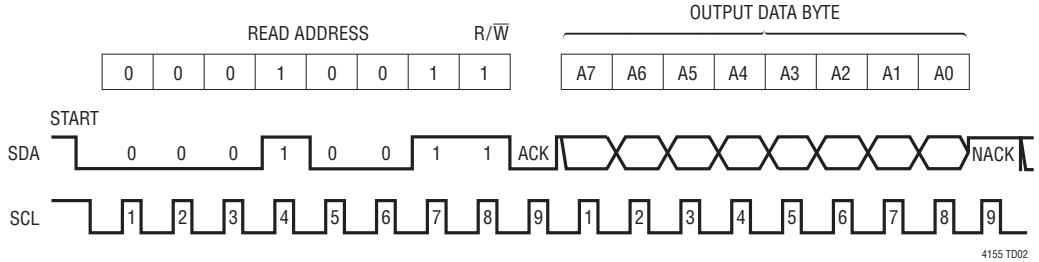


# TIMING DIAGRAMS

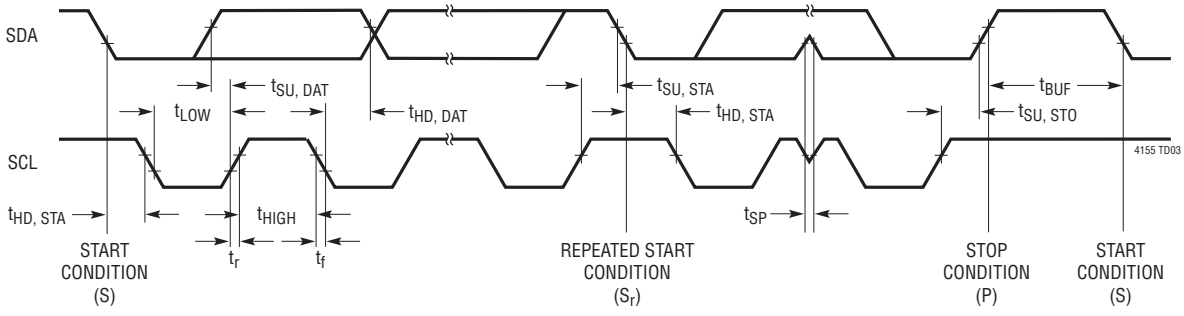
### I²C Write Protocol




### I²C Read Protocol




### Timing Diagram



# OPERATION

## I²C

**Table 2. I²C Map**

| REGISTER | ACCESS | SUB ADDRESS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|
| **REG0** | WRITE/ READBACK | 0x00 | DISABLE INPUT UVCL | 0 RESERVED | LOCKOUT USB OTG ID PIN | USB CURRENT LIMIT | | | | |
| **REG1** | WRITE/ READBACK | 0x01 | INPUT PRIORITY | SAFETY TIMER | | WALL CURRENT LIMIT | | | | |
| **REG2** | WRITE/ READBACK | 0x02 | CHARGE CURRENT | | | | FLOAT VOLTAGE | | C/x DETECTION | |
| **REG3** | READ | 0x03 | CHARGER STATUS | | | ID PIN DETECTION STATUS | BOOST ENABLE STATUS | THERMISTOR STATUS | | LOW BATTERY STATUS |
| **REG4** | READ | 0x04 | EXTERNAL POWER GOOD | USBSNS GOOD | WALLSNS GOOD | INPUT CURRENT LIMIT ACTIVE | INPUT UVCL ACTIVE | OVP ACTIVE | OTG FAULT | BAD CELL FAULT |
| **REG5** | READ | 0x05 | THERMISTOR VALUE | | | | | | | THERMIS-TOR WARNING |
| **REG6** | WRITE/ READBACK<br>CLEAR INTERRUPT*<br>DISARM SHIP-AND-STORE MODE* | 0x06 | ENABLE CHARGER INTERRUPTS | ENABLE FAULT INTERRUPTS | ENABLE EXTERNAL POWER INTERRUPTS | ENABLE USB OTG INTERRUPTS | ENABLE INPUT CURRENT LIMIT INTERRUPTS | ENABLE INPUT UVCL INTERRUPTS | ENABLE USB On-The-Go | 0 RESERVED |
| **REG7** | WRITE<br>ARM SHIP-AND-STORE MODE** | 0x07 | 0 REQUIRED | 0 REQUIRED | 0 REQUIRED | 0 REQUIRED | 0 REQUIRED | 0 REQUIRED | 0 REQUIRED | 0 REQUIRED |

*Interrupts are cleared and ship-and-store mode is disarmed during the acknowledge clock cycle following a full data byte written to sub address 0x06. Reading data from sub address 0x06 has no effect.

**Ship-and-store mode is armed during the acknowledge clock cycle following a full data byte written to sub address 0x07. The data written to sub address 0x07 is ignored. Reading from sub address 0x07 has no effect and the returned data is undefined, independent of the arming state of ship-and-store mode.

## OPERATION

### Introduction

The LTC4156 is an advanced I²C controlled power manager and $LiFePO_4$ battery charger designed to efficiently transfer up to 15W from a variety of sources while minimizing power dissipation and easing thermal budgeting constraints. By decoupling $V_{OUT}$ and the battery, the innovative instant-on PowerPath architecture ensures that the application is powered immediately after external voltage is applied, even with a completely dead battery, by prioritizing power to the application.

Since $V_{OUT}$ and the battery are decoupled, the LTC4156 includes an ideal diode controller. The ideal diode from the battery to $V_{OUT}$ guarantees that ample power is always available to $V_{OUT}$ even if there is insufficient or absent power at $V_{BUS}$.

The LTC4156 includes a monolithic step-down switching battery charger for USB support, wall adapters and other 5V sources. By incorporating a unique input current measurement and control system, the switching charger interfaces seamlessly to wall adapters and USB ports without requiring application software to monitor and adjust system loads. Because power is conserved, the LTC4156 allows the load current on $V_{OUT}$ to exceed the current drawn by the USB port or wall adapter, making maximum use of the allowable power for battery charging without exceeding the USB or wall adapter power delivery specifications. A wide range of input current settings as well as battery charge current settings are available for selection by I²C.

Using only one inductor, the switching PowerPath can operate in reverse, boosting the battery voltage to provide 5V power at its input pin for USB On-The-Go applications. In the USB-OTG mode, the switching regulator supports USB high power loads up to 500mA. Protection circuits ensure that the current is limited and ultimately the channel is shut down if a fault is detected on the USB connector.

To support USB low power mode, the LTC4156 can deliver power to the external load and charge the battery through a linear regulator while limiting input current to less than 100mA.

The LTC4156 also features a combination overvoltage protection circuit/priority multiplexer which prevents damage to its input caused by accidental application of high voltage and selects one of two high power input connectors based on priority.

A thermistor measurement subsystem periodically monitors and reports the battery's thermistor value via the onboard I²C port. The same circuit then reports when dangerous battery temperatures are reached and can autonomously pause charging.

To minimize battery drain when a device is connected to a suspended USB port, an LDO from $V_{BUS}$ to $V_{OUT}$ provides the allowable USB suspend current to the application.

An interrupt subsystem can be enabled to alert the host microprocessor of various status change events so that system parameters can be varied as needed by system software. Several status change event categories are maskable for maximum flexibility.

To eliminate battery drain between manufacture and sale, a ship-and-store feature reduces the already low battery standby current to nearly zero and optionally disconnects power from downstream circuitry.

An input undervoltage amplifier optionally prevents the input voltage from decreasing below 4.3V when a resistive cable or current limited supply is providing input power to the LTC4156.

Finally, the LTC4156 has considerable adjustability built in so that power levels and status information can be controlled and monitored via the simple 2-wire I²C port.

### Input Current-Limited Step-Down Switching Charger

Power delivery from $V_{BUS}$ to $V_{OUT}$ is controlled by a 2.25MHz constant-frequency step-down switching regulator. The switching regulator reduces output power in response to one of six regulation loops, including battery voltage, battery charge current, output voltage, input current, input undervoltage, and external PMOS charger FET power dissipation. For USB low power (100mA) and USB suspend (2.5mA) modes, the switching regulator is disabled and power is transmitted through a linear regulator.

## OPERATION

### Battery Float Voltage Regulation

When the battery charger is enabled, the switching regulator will reduce its output power to prevent $V_{BATSNS}$ from exceeding the programmed battery float voltage, $V_{FLOAT}$. The float voltage may be selected from among four possible choices via the $I^2C$ interface using bits VFLOAT[1:0]. Refer to Table 11.

### Battery Charge Current Regulation and Low Cell Trickle Charge

The switching regulator will also reduce its output power to limit battery charge current, $I_{CHARGE}$, to a programmed maximum value. The battery charge current is programmed using both a resistor, $R_{PROG}$, between PROG and ground to set default maximum charge current plus $I^2C$ adjustability to optionally reduce programmed charge current. The battery charge current loop mirrors a precise fraction of the battery charge current, $I_{BAT}$, to the PROG pin, then reduces switching regulator output power to limit the resultant voltage, $V_{PROG}$, to one of fifteen possible servo reference voltages.

The following expression may be used to determine the battery charge current at any time by sampling the PROG pin voltage.

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000$$

This expression may also be used to calculate the required value of $R_{PROG}$ for any desired charge current. The resistor value required to program default maximum charge current may be found by substituting $V_{PROG}$ = 1.200 and solving for $R_{PROG}$. The other fourteen settings are $I^2C$ selectable using ICHARGE[3:0] and reduce the charge current in 6.25% steps. The resulting limits may be found by substituting $R_{PROG}$ and the relevant $V_{PROG}$ servo voltage from Table 10.

The maximum charge current should be set based on the cell size and maximum charge rate without regard to input current setting or input power source.

The LTC4156 monitors the voltage across the external PMOS transistor and automatically reduces the current regulation servo voltage at $V_{PROG}$ to limit power dissipation in the transistor. During normal operation, the PMOS channel is fully enhanced and power dissipation is typically under 100mW. Starting when the battery voltage is below approximately 2.94V, the charge current servo voltage will be gradually reduced from its $I^2C$ programmed value to a minimum value between 75mV and 100mV when the battery is below $V_{LOWBAT}$, typically 2.8V. This charge current reduction has the combined effect of protecting the external PMOS transistor from damage due to excessive heat, while also trickle charging the excessively depleted cell to maximize battery health and lifetime. Peak power dissipation in the external PMOS transistor is limited to approximately 700mW. Figure 1 shows the relationship between battery voltage, charge current and power dissipation.

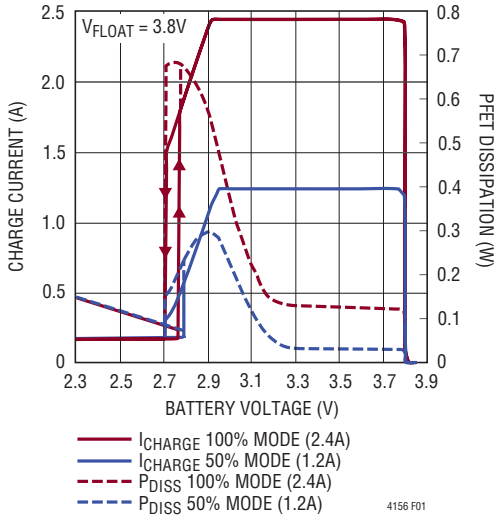



**Figure 1. $V_{OUT}$ Minimum Voltage Regulation**

### $V_{OUT}$ Voltage Regulation

A third control loop reduces power delivery by the switching regulator in response to the voltage at $V_{OUT}$, which has a nonprogrammable servo voltage of 4.35V. When the battery charger is enabled, $V_{OUT}$ is connected to BATSNS through the internal charge current sense resistor and the external PMOS battery FET. The two node voltages will differ only by the I • R drop through the two devices, effectively keeping $V_{OUT}$ below its servo point for the duration of the charge cycle.

The LTC4156 will attempt to prevent $V_{OUT}$ from falling below approximately 3.19V when the battery is deeply

## OPERATION

discharged. This feature allows instant-on operation when the low state of charge would otherwise prevent operation of the system. If the system load plus battery charger load exceeds the available input power, battery charge current will be sacrificed to prioritize the system load and maintain the switching regulator output voltage while continuing to observe the input current limit. If the system load alone exceeds the power available from the input, the output voltage must fall to deliver the additional current, with supplemental current eventually being supplied by the battery.

### Input Current Regulation

To meet the maximum load specification of the available supply (USB/wall adapter), the switching regulator contains a measurement and control system which ensures that the average input current is below the level programmed at the CLPROG1 or CLPROG2 pin and the $I^2C$ port. Connecting a single 1% tolerance resistor of the recommended value to both the CLPROG1 and CLPROG2 pins guarantees compliance with the 2.5mA, 100mA, 500mA, and 900mA USB 2.0/3.0 current specifications, while also permitting other $I^2C$ selectable current limits up to 3A. The input current limit is independently selectable for each of the two inputs, with the USBILIM[4:0] and WALLILIM[4:0] bits in the $I^2C$ port. The USB input current limit setting resets to 100mA when power is removed from its respective input. The WALL input current limit setting resets to 100mA when power is removed from both the USB and WALL inputs. Refer to Alternate Default Input Current Limit in the Operation section to program a non USB compliant default input current limit for use with wall adapters or other power sources. Refer to Table 7 for a complete listing of $I^2C$ programmable input current limit settings.

If the combined external load plus battery charge current is large enough to cause the switching power supply to reach the programmed input current limit, the battery charger will reduce its charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the battery charge current is programmed to exceed the allowable input power, the specification for average input current will not be violated; the battery charger will reduce its current as needed. Furthermore, if the load at $V_{OUT}$ exceeds the programmed power level from $V_{BUS}$, the extra load current will be drawn from the battery via the ideal diode independent of whether the battery charger is enabled or disabled.

### Input Undervoltage Current Limit

The LTC4156 can tolerate a resistive connection to the input power source by automatically reducing power transmission as the $V_{BUS}$ pin drops to 4.3V preventing a possible UVLO oscillation. The undervoltage current limit feature can be disabled by $I^2C$ using the DISABLE_INPUT_UVCL bit. Refer to Table 5.

### USB On-The-Go 5V Boost Converter

The LTC4156 switching regulator can be operated in reverse to deliver power from the battery to $V_{BUS}$ while boosting the $V_{BUS}$ voltage to 5V. This mode can be used to implement features such as USB On-The-Go without any additional magnetics or other external components.

The step-up switching regulator may be enabled in one of two ways. The LTC4156 can optionally monitor the ID pin of a USB cable and autonomously start the step-up regulator when a host-side A/B connector is detected with a grounded ID pin. The switching regulator may also be enabled directly with the REQUEST_OTG $I^2C$ command. Note that the step-up regulator will not operate if input power is present on either the USB or WALL input, or if the battery voltage is below $V_{LOWBAT}$, typically 2.8V. The $I^2C$ status bits OTG_ENABLED, LOWBAT and OTG_FAULT can be used to determine if the step-up converter is running. Refer to ID Pin Detection in the Operation section for more information about the autonomous step-up regulator start-up.

The step-up regulator only provides power to the USB input. It is not possible to provide power to the WALL input. The $I^2C$ PRIORITY setting has no effect on step-up regulator operation. Refer to Dual Input Overvoltage Protection and Undervoltage Lockout in the Operation section for more information about multiple input operation.

The switching regulator is guaranteed to deliver 500mA to $V_{BUS}$ and will limit its output current to approximately 1.4A while allowing $V_{BUS}$ to fall when overloaded. If a short-circuit fault is detected, the channel will be shut down after approximately 8ms and the problem will be reported with the $I^2C$ status bit OTG_FAULT.

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### ID Pin Detection

For USB On-The-Go compatibility, the step-up switching regulator can optionally start autonomously when the grounded ID pin in the A side of an On-The-Go cable is detected.

The ID pin is monitored at all times. Its status is reported in the I²C bit ID_DETECT, reporting true when the ID pin is grounded. Optionally, any change in ID_PIN_DETECT may trigger an interrupt request to notify the system processor. Unless the I²C LOCKOUT_ID_PIN bit has been set, ID pin detection will also automatically start the step-up regulator. Note that LOCKOUT_ID_PIN locks out automatic start-up, but not monitoring of the ID pin. Also, the REQUEST_OTG command may be used to enable the step-up regulator, independent of the state of ID_PIN_DETECT and LOCKOUT_ID_PIN. Note that the regulator will not start if input power is already present on either input. The I²C status bits OTG_ENABLED and OTG_FAULT can be used to determine if the regulator is running.

The ID pin detection circuit will report a short on the ID pin for ID pin impedances lower than approximately 24k. The USB Battery Charging Specification Rev 1.1 added additional signaling to the ID pin, specifying other possible ID pin resistances of RID_A, RID_B and RID_C. These impedances are all larger than the 24k threshold and will typically not cause an ID pin short detection.

### Dual Input Overvoltage Protection and Undervoltage Lockout

The LTC4156 can provide overvoltage protection to its two power inputs with minimal external components, as shown in Figure 2.

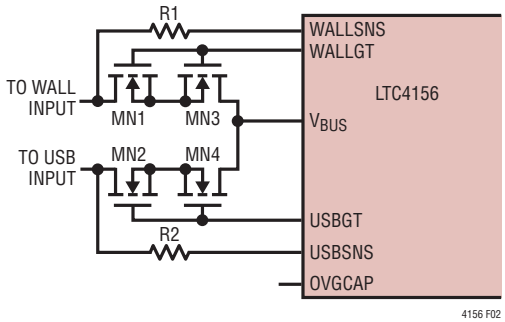



**Figure 2. Dual-Input Overvoltage Protection Multiplexer**

The LTC4156 acts as a shunt regulator when the input is overvoltage, clamping USBSNS or WALLSNS to 6V. Resistors R1 and R2 should be 3.6k and be rated appropriately for the worst-case power dissipation during an overvoltage event. The power dissipated in the resistor is given by the following expression:

$$P_{RESISTOR} = \frac{(V_{OVERVOLTAGE} - 6V)^2}{3.6k}$$

For example, a typical 0201 size resistor would be appropriate for possible overvoltage events up to 19V. An 0402 size resistor would be appropriate up to 20V, an 0603 up to 24V, an 0805 up to 27V, and a 1206 up to 35V. Additional power derating may be necessary at elevated ambient temperature. The maximum allowed shunt current into the USBSNS and WALLSNS pins constrains the upper limit of protection to 77V.

The drain-source voltage rating, $V_{DS}$, of N-channel FETs MN1-MN2 must be appropriate for the level of overvoltage protection desired, as the full magnitude of the input voltage is applied across one of these devices.

The drain-source voltage rating of N-channel FETs MN3-MN4 need only be as high as the protection threshold, typically 6.0V. MN3-MN4 are not required for overvoltage protection, but are required to block current from circulating from one input to the other through the unused channel's FET body diode. For single-input applications, only a single power FET is required. Refer to Alternate Input Power Configurations in the Applications Information section for implementation details.

Negative voltage protection can be added by reconfiguring the circuit without adding any additional power transistors. Refer to Alternate Input Power Configurations in the Applications Information section for implementation details.

For an input (USB or WALL) to be considered a valid power source, it must satisfy three conditions. First, it must be above a minimum voltage, $V_{UVLO}$. Second, it must be greater than the battery voltage by a minimum of $V_{DUVLO}$. Lastly, it must be below the overvoltage protection threshold voltage, $V_{OVLO}$. The USBSNS and WALLSNS pins each draw a small current which causes a voltage offset between the USB and WALL inputs and the USBSNS and

## OPERATION

WALLSNS pins. The voltage threshold values previously listed and specified in the Electrical Characteristics table are valid when each input is connected to its respective sense pin through a 3.6k resistor.

The status of the USB and WALL inputs is monitored continuously and reported by I²C, with the option of generating several interrupts. When all three conditions previously listed are true, the LTC4156 will report the input valid by asserting USBSNSGD or WALLSNSGD in the I²C port. Optionally, if external power interrupts are enabled, an interrupt request will be generated.

When power is applied simultaneously to both inputs, the LTC4156 will draw power from the WALL input by default. If the I²C PRIORITY bit is asserted, the LTC4156 will instead draw power from the USB input when both inputs are present. The USB On-The-Go step-up regulator delivers power only to the USB input, and the PRIORITY bit is ignored in this mode. The input current limits USBILIM[4:0] and WALLILIM[4:0] also reset to 100mA default mode under different criteria. In all other respects, the two inputs are identical.

An optional capacitor may be placed between the OVGCAP pin and GND to minimize input current disruption when switching from one input to the other while operating at high power levels. The capacitor must be rated to withstand at least 13V and should be approximately ten times larger than the total gate capacitance of the series NMOS power transistors. Capacitance on this pin can also be used to slow the gate charging if the application requires controlled inrush current to any additional input capacitance on the $V_{BUS}$ pin. If fast switching between input or inrush control is not necessary, OVGCAP may be left unconnected.

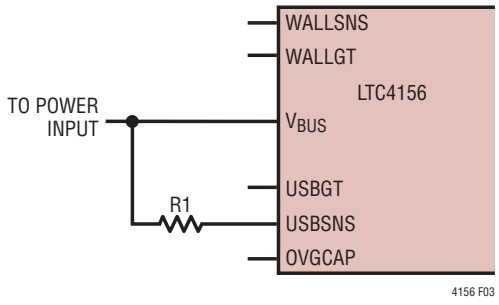



**Figure 3. No Overvoltage Protection**

If overvoltage protection is not necessary in the application, connect USBSNS to $V_{BUS}$ with a 3.6k resistor, as shown in Figure 3. If the USB On-The-Go step-up regulator is not used in the application, it is also possible to connect WALLSNS to $V_{BUS}$ through 3.6k and leave USBSNS open.

### 100mA Linear Battery Charger Mode

The LTC4156 features a mode to support USB low power operation. Total input current to the LTC4156 is guaranteed to remain below 100mA in this mode when the recommended resistor is used on the CLPROG2 pin. The step-down switching regulator does not operate in this mode. Instead, a linear regulator provides power from $V_{BUS}$ to $V_{OUT}$ and the battery. The linear battery charger follows the same constant-current/constant-voltage algorithm as the switching regulator, but regulates input current rather than battery charge current. The voltage on the CLPROG2 pin represents the input current in this mode, using the expression:

$$I_{VBUS} = \frac{V_{CLPROG2}}{R_{CLPROG2}} \bullet (80)$$

Battery charge current is represented by the voltage on the PROG pin, but it is not regulated in this mode.

$$I_{CHARGE} = \frac{V_{PROG}}{R_{PROG}} \bullet (1000)$$

$V_{OUT}$ will generally be very close to the battery voltage when the battery charger is enabled, except when the battery voltage is very low, the LTC4156 will increase the impedance between $V_{OUT}$ and BATSNS to facilitate instant-on operation. If the system load plus battery charge current exceeds the available input current, battery charge current will be sacrificed to give priority to the load. If the system load alone exceeds the available input current, $V_{OUT}$ must fall to the battery voltage so that the battery may provide the supplemental current.

The battery will charge to the float voltage specified by the I²C setting VFLOAT[1:0]. See Table 11.

When the battery charger is disabled or terminated, $V_{OUT}$ will be regulated to 4.35V.

## OPERATION

### 2.5mA Linear Suspend Mode

The LTC4156 can supply a small amount of current from $V_{BUS}$ to $V_{OUT}$ to power the system and reduce battery discharge when the product has access to a suspended USB port. When the system load current is less than the current available from the suspended USB port, the voltage at $V_{OUT}$ will be regulated to 4.35V. If the system load current exceeds USB input current limit, the voltage at $V_{OUT}$ will fall to the battery voltage and any supplemental current above that available from the USB port will be supplied by the battery. CLPROG2 will servo to 103mV in current limit. Battery charging is disabled in suspend mode. Either the USB or WALL input may utilize this current limited suspend mode by programming the appropriate setting in the respective USBILIM or WALLILIM register.

### Ideal Diode and Minimum $V_{OUT}$ Controller

The LTC4156 features an ideal diode controller to ensure that the system is provided with sufficient power even when input power is absent or insufficient. This requires an external PMOS transistor with its source connected to CHGSNS, gate to BATGATE, and drain to BATSNS. The controller modulates the gate voltage of the PMOS transistor to allow current to flow from the battery to $V_{OUT}$ to power the system while blocking current in the opposite direction to prevent overcharging of the battery.

The ideal diode controller has several modes of operation. When input power is available and the battery is charging, the PMOS gate will generally be grounded to maximize conduction between the switching regulator and the battery for maximum efficiency. If the battery is deeply discharged, the LTC4156 will automatically increase the impedance between the switching regulator and the battery enough to prevent $V_{OUT}$ from falling below approximately 3.19V. Power to the system load is always prioritized over battery charge current. Increasing the impedance between $V_{OUT}$ and the battery does not necessarily affect the battery charge current, but it may do so for one of the following two reasons:

1. The charge current will be limited to prevent excessive power dissipation in the external PMOS as it becomes more resistive. Charge current reduction begins when the voltage across the PMOS reaches approximately 250mV, and can reduce the charge current as low as 8% full scale. Maximum power dissipation in the PMOS is limited to approximately 700mW with $R_{PROG}$ = 499Ω.
2. When limited power is available to the switching regulator because either the programmed input current limit or input undervoltage current limit is active, charge current will automatically be reduced to prioritize power delivery to the system at $V_{OUT}$. $V_{OUT}$ will be maintained at 3.19V as long as possible without exceeding the input power limitation. If the system load alone requires more power than is available from the input after charge current has been reduced to zero, $V_{OUT}$ must fall to the battery voltage as the battery begins providing supplemental power.

When input power is available, but the battery charger is disabled or charging has terminated, $V_{OUT}$ and the battery are normally disconnected to prevent overcharging the battery. If the power required by the system should exceed the power available from the input, either because of input current limit or input undervoltage current limit, $V_{OUT}$ will fall to the battery voltage and any additional current required by the load will be supplied by the battery through the ideal diode.

When input power is unavailable, the ideal diode switches to a low power mode which maximizes conduction and power transmission efficiency between $V_{OUT}$ and the battery by grounding the PMOS gate.

Finally, when ship-and-store mode is activated, the ideal diode is shut down and BATGATE is driven to the battery voltage to prevent conduction through the PMOS. Note that with a single FET, conduction to $V_{OUT}$ is still possible through the body connection diode. Refer to Low Power Ship-and-Store Mode in the Operation section for more information about this mode.

## OPERATION

### Low Power Ship-and-Store Mode

The LTC4156 can reduce its already low standby current to approximately 1µA in a special mode designed for shipment and storage. Unlike normal standby mode, in this mode the external PMOS gate is driven to the battery voltage to disable FET conduction through the external PMOS. This mode may be used to cut off all power to any downstream load on $V_{OUT}$ to maximize battery life between product manufacture and sale. Note that the bulk connection inside the external PMOS will provide a conductive path from the battery to $V_{OUT}$, independent of the voltage on its gate. To block conduction to $V_{OUT}$, typically two PMOS transistors must be connected in series with either the sources or drains of each device connected in the center, as shown in Figure 4. If the application does not require the battery to be isolated from downstream devices, significant power savings in the LTC4156 may still be realized by activating this mode.

Ship-and-store mode is armed following the acknowledge of any data byte written to sub address 0x07 by the I²C bus master. The contents of the data byte are ignored, but the full byte and acknowledge clock cycle must be sent. Ship-and-store mode is activated as $V_{BUS}$ falls below approximately 1V, or immediately if no input power is present when the I²C command is issued. $V_{BUS}$ quiescent current falls to nearly zero when power is removed from the USB and WALL inputs, resulting in a delay of up to several hours for $V_{BUS}$ to self-discharge to the 1V activation threshold. Faster activation may be achieved by connecting a 1M resistor between $V_{BUS}$ and GND. Reading from sub address 0x07 has no effect on arming or activation and the returned data is undefined, independent of the arming or activation state.

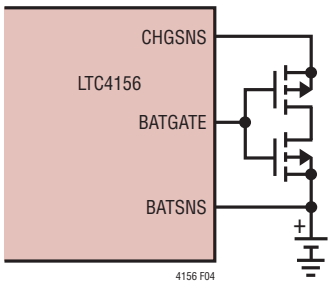



**Figure 4. Ship-and-Store Mode Required Components to Enforce Downstream ($V_{OUT}$) Shutdown**

Once engaged, ship-and-store mode can be disengaged by applying power to the USB or WALL input or by writing any full data byte and acknowledge clock cycle to sub address 0x06 if the I²C bus master is still powered.

### I²C Interface

The LTC4156 may communicate with a bus master using the standard I²C 2-wire interface. The Timing Diagram shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be HIGH when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines. The LTC4156 is both a slave receiver and slave transmitter. The I²C control signals, SDA and SCL, are scaled internally to the DVCC supply. DVCC should be connected to the same power supply as the bus pull-up resistors.

The I²C port has an undervoltage lockout on the DVCC pin. When DVCC is below approximately 1V, the I²C serial port is cleared, the LTC4156 is set to its default configuration, pending interrupts will be cleared, and future interrupts will be disabled.

### Bus Speed

The I²C port is designed to operate at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches.

### START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LTC4156, the master may transmit a STOP condition which commands the LTC4156 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH.

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### Byte Format

Each frame sent to or received from the LTC4156 must be eight bits long, followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC4156 most significant bit (MSB) first.

### Master and Slave Transmitters and Receivers

Devices connected to an I²C bus may be classified as either master or slave. A typical bus is composed of one or more master devices and a number of slave devices. Some devices are capable of acting as either a master or a slave, but they may not change roles while a transaction is in progress.

The transmitter/receiver relationship is distinct from that of master and slave. The transmitter is responsible for control of the SDA line during the eight bit data portion of each frame. The receiver is responsible for control of SDA during the ninth and final acknowledge clock cycle of each frame.

All transactions are initiated by the master with a START or repeat START condition. The master controls the active (falling) edge of each clock pulse on SCL, regardless of its status as transmitter or receiver. The slave device never brings SCL LOW, but may extend the SCL LOW time to implement clock stretching if necessary. The LTC4156 does not clock stretch and will never hold SCL LOW under any circumstance.

The master device begins each I²C transaction as the transmitter and the slave device begins each transaction as the receiver. For bus write operations, the master acts as the transmitter and the slave acts as receiver for the duration of the transaction. For bus read operations, the master and slave exchange transmit/receive roles following the address frame for the remainder of the transaction.

### Acknowledge

The acknowledge signal (ACK) is used for handshaking between the transmitter and receiver. When the LTC4156 is written to, it acknowledges its write address as well as the subsequent data bytes as a slave receiver. When it is read from, the LTC4156 acknowledges its read address as a slave receiver. The LTC4156 then changes to a slave transmitter and the master receiver may optionally acknowledge receipt of the following data byte from the LTC4156.

The acknowledge related clock pulse is always generated by the bus master. The transmitter (master or slave) releases the SDA line (HIGH) during the acknowledge clock cycle. The receiver (slave or master) pulls down the SDA line during the acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

When the LTC4156 is read from, it releases the SDA line after the eighth data bit so that the master may acknowledge receipt of the data. The I²C specification calls for a not acknowledge (NACK) by the master receiver following the last data byte during a read transaction. Upon receipt of the NACK, the slave transmitter is instructed to release control of the bus. Because the LTC4156 only transmits one byte of data under any circumstance, a master acknowledging or not acknowledging the data sent by the LTC4156 has no consequence. The LTC4156 will release the bus in either case.

### Slave Address

The LTC4156 responds to a 7-bit address which has been factory programmed to 0b0001_001[R/$\overline{W}$]. The LSB of the address byte, known as the read/write bit, should be 0 when writing data to the LTC4156, and 1 when reading data from it. Considering the address an 8-bit word, then the write address is 0x12, and the read address is 0x13. The LTC4156 will acknowledge both its read and write addresses.

### Sub Addressed Access

The LTC4156 has four command registers for control input and three status registers for status reporting. They are accessed by the I²C port via a sub addressed pointer system where each sub address value points to one of the seven control or status registers within the LTC4156. The sub address pointer is always the first byte written immediately following the LTC4156 write address during bus write operations. The sub address pointer value persists after the bus write operation and will determine which data byte is returned by the LTC4156 during any

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subsequent bus read operations. The sub address pointer register is equivalent to the command code byte within the SMBus write byte and read byte protocols explained in detail under the SMBus Protocol Compatibility section.

### Bus Write Operation

The bus master initiates communication with the LTC4156 with a START condition and the LTC4156's write address. If the address matches that of the LTC4156, the LTC4156 returns an acknowledge. The bus master should then deliver the sub address. The sub address value is transferred to a special pointer register within the LTC4156 upon the return of the sub address acknowledge bit by the LTC4156. If the master wishes to continue the write transaction, it may then deliver the data byte. The data byte is transferred to an internal pending data register at the location of the sub address pointer when the LTC4156 acknowledges the data byte. The LTC4156 is then ready to receive a new sub address, optionally repeating the [SUB ADDRESS][DATA] cycle indefinitely. After the write address, the odd position bytes always represent a sub address pointer assignment and the even position bytes always represent data to be stored at the location referenced by the sub address pointer. The master may terminate communication with the LTC4156 after any even or odd number of bytes with either a repeat START or a STOP condition. If a repeat START condition is initiated by the master, the LTC4156, or any other chip on the $I^2C$ bus, can then be addressed. The LTC4156 will remember, but not act on, the last input of valid data that it received at each sub address location. This cycle can also continue indefinitely. Once all chips on the bus have been addressed and sent valid data, a global STOP can be sent and the LTC4156 will immediately update all of its command registers with the most recent pending data that it had previously received. This delayed execution behavior is compliant with the PMBus group command protocol.

### Bus Read Operation

The LTC4156 contains seven readable registers. Three are read only and contain status information. Four contain control information which may be both written and read back by the bus master.

Only one of the seven sub addressed data registers is accessible during each bus read operation. The data returned by the LTC4156 is from the data register pointed to by the contents of the sub address pointer register. The pointer register contents are determined by the most recent previous bus write operation.

In preparation for a bus read operation, it may be advantageous for a bus master to prematurely terminate a write transaction with a STOP or repeat START condition after transmitting only an odd number of bytes. The last transmitted byte then represents a pointer to the register of interest for the subsequent bus read operation.

The bus master reads status data from the LTC4156 with a START or repeat START condition followed by the LTC4156 read address. If the read address matches that of the LTC4156, the LTC4156 returns an acknowledge. Following the acknowledgement of its read address, the LTC4156 returns one bit of status information for each of the next eight clock cycles from the register selected by the sub address pointer. Additional clock cycles from the master after the single data byte has been read will leave the SDA line high (0xFF transmitted). The LTC4156 will never acknowledge any bytes during a bus read operation with the exception of its read address.

To read the same register again, the transaction may be repeated starting with a START followed by the LTC4156 read address. It is not necessary to rewrite the sub address pointer register if the sub address has not changed. To read a different register, a write transaction must be initiated with a START or repeat START followed by the LTC4156 write address and sub address pointer byte before the read transaction may be repeated.

When the contents of the sub address pointer register point to a writeable command register, the data returned in a bus read operation is the pending command data at that location if it had been modified since the last STOP condition. After a STOP condition, all pending data is copied to the command registers for immediate effect. The contents of several writeable registers within the LTC4156 are modified upon removal of input power without an $I^2C$ transaction. USBILIM[4:0] and WALLILIM[4:0] default to either 100mA mode (0x00) or CLPROG1 mode (0x1F)

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as explained in the Alternate Default Input Current Limit section of Operation. Thus, the contents of these registers may be different from the last value written by the bus master, and reading back the contents may be useful to determine the state of the system.

When the contents of the sub address pointer register point to a read-only status register, the data returned is a snapshot of the state of the LTC4156 at a particular instant in time. If no interrupt requests are pending, the status data is sampled when the LTC4156 acknowledges its read address, just before the LTC4156 begins data transmission during a bus read operation. When an unmasked interrupt event takes place, the $\overline{IRQ}$ pin is driven low and data is latched in the three read-only status registers at that moment. Any subsequent read operation from any status registers will return this frozen data to facilitate determination of the cause of the interrupt request. After the bus master clears the LTC4156 interrupt request, the status latches are cleared. Bus read operations will then again return either a snapshot of the data at the read address acknowledge, or at the time of the next interrupt assertion, whichever comes first.

### SMBus Protocol Compatibility

The SMBus specification is generally compatible with the $I^2C$ bus specification, but extends beyond $I^2C$ to define and standardize specific protocol formats for various types of transactions. The LTC4156 $I^2C$ interface is fully compatible with four of the protocols defined by the SMBus specification. All control and status features of the LTC4156 can be accessed using the SMBus protocols, although if high bus utilization is a concern, certain operations can be accomplished more efficiently by $I^2C$ bus operations that do not adhere to any of the SMBus defined protocols.

### SMBus Write Byte Protocol

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND CODE | A | DATA BYTE | A | P |

The SMBus write byte protocol can be used to modify the contents of any single control register in the LTC4156. The transaction is initiated by the bus master with a START condition. The SMBus slave address corresponds to the LTC4156 write address, which is 0x09 when interpreted as a 7-bit word (0b 000 1001), followed by WR (value 0b0). The LTC4156 will acknowledge its write address. The SMBus command code corresponds to the sub address pointer value and will be written to the sub address pointer register in the LTC4156. Only the register locations with write access (0x00 to 0x02, 0x06 to 0x07) are meaningful values for the sub address pointer when using this protocol. The LTC4156 will acknowledge the SMBus command code byte. The SMBus data byte corresponds to the command data to be written to the location pointed to by the sub address pointer register. The LTC4156 will acknowledge the SMBus data byte. The STOP condition at the end of the sequence will force an update to the command registers, causing the new command data to take immediate effect.

### SMBus Read Byte Protocol

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND CODE | A | Sr | SLAVE ADDRESS | RD | A | DATA BYTE | A | P |

The SMBus read byte protocol can be used to read the contents of any one of the seven control or status registers with one bus transaction. The transaction is initiated by the bus master with a START condition. The SMBus slave address corresponds to the LTC4156 write address, which is 0x09 when interpreted as a 7-bit word (0b 000 1001), followed by WR (value 0b0). The LTC4156 will acknowledge its write address. The SMBus command code corresponds to the sub address pointer value and will be written to the sub address pointer register in the LTC4156. The LTC4156 will acknowledge the SMBus command code byte. The master then issues a repeat START condition, followed by the LTC4156 slave address (0x09) and RD (0b1). The LTC4156 will acknowledge its read address. At this time the bus master becomes a receiver while continuing to clock SCL. The LTC4156 becomes a slave transmitter and controls SDA to place data on the bus. Following the single data byte, the bus master has the option of transmitting either an ACK or a NACK bit. According to the $I^2C$ specification, a master

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must transmit a NACK at the end of a read transaction to instruct the slave to terminate data transmission. Because the LTC4156 terminates data transmission after one byte in all cases, whether the bus master transmits an ACK or a NACK is irrelevant. Finally, a STOP condition returns the bus to the idle state.

### SMBus Send Byte Protocol

| 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | DATA BYTE | A | P |

The SMBus send byte protocol can be used to modify the contents of the sub address pointer register without modifying the contents of any control registers. It has utility when preparing to later read status information from the LTC4156 using the SMBus receive byte protocol. The transaction is initiated by the bus master with a START condition. The SMBus slave address corresponds to the LTC4156 write address, which is 0x09 when interpreted as a 7-bit word (0b 000 1001) followed by WR (value 0b0). The LTC4156 will acknowledge its write address. The SMBus data byte corresponds to the sub address pointer value and will be written to the sub address pointer register in the LTC4156. Note that the data byte in this protocol is analogous to the command code in the write byte and read byte protocols. The LTC4156 will acknowledge the SMBus data byte. Finally, a STOP condition returns the bus to the idle state.

### SMBus Receive Byte Protocol

| 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | RD | A | DATA BYTE | A | P |

The SMBus receive byte protocol can be used to read the contents of the command or status register already selected by the sub address pointer register. This protocol is incapable of modifying the contents of the sub address pointer register, but may be useful to poll a single status register repeatedly with much less bus overhead than the other SMBus protocols. The sub address pointer register can be modified by any of the SMBus write byte, read byte or send byte protocols and the register contents will persist until they are modified again by one of these three protocols.

The receive byte transaction is initiated by the bus master with a START condition. The SMBus slave address corresponds to the LTC4156 read address, which is 0x09 when interpreted as a 7-bit word (0b 000 1001), followed by RD (value 0b1). The LTC4156 will acknowledge its read address. At this time the bus master becomes a receiver while continuing to clock SCL. The LTC4156 becomes a slave transmitter and controls SDA to place data on the bus. Following the single data byte, the bus master has the option of transmitting either an ACK or a NACK bit. According to the $I^2C$ specification, a master must transmit a NACK at the end of a read transaction to instruct the slave to terminate data transmission. Because the LTC4156 terminates data transmission after one byte in all cases, whether the bus master transmits an ACK or a NACK is irrelevant. Finally, a STOP condition returns the bus to the idle state.

### Programmable Interrupt Controller

The LTC4156 can optionally generate active LOW, level-triggered interrupt requests on the $\overline{IRQ}$ pin in response to a number of status change or fault events. The three available bytes of status information are also frozen at the time the interrupt is triggered to aid in determining the cause of a transient interrupt. The contents of the four writeable command registers are never frozen by interrupts. The interrupt trigger events are grouped into six individually maskable categories corresponding to battery charger status, faults, input power detection, USB On-The-Go, input current limit and input undervoltage current limit. The interrupt mask register (IMR) is located at sub address location 0x06, with the six most significant bits representing the mask programming. Refer to Table 3. Table 4 lists the status triggers for each interrupt category. Upon power-up, all interrupts default to disabled (masked). Each interrupt category may be enabled by writing a "1" to the appropriate position in the IMR. Any data written to sub address 0x06 also has the side effect of clearing the pending interrupt upon the acknowledge bit of the data (third) byte. Clearing the interrupt releases the $\overline{IRQ}$ pin and resumes status reporting of live data until the next interrupt. If no change to the interrupt mask is desired, the bus master must rewrite the previous data to sub address 0x06 to clear an interrupt request.

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**Table 3. Interrupt Mask Register**

| INTERRUPT MASK REGISTER (IMR) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **SUB ADDRESS** | 0x06 | REG6 | | | | | | |
| **DIRECTION** | Write/Clear Interrupt, Read | | | | | | | |
| | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| ENABLE_CHARGER_INT | 1 | | | | | | | |
| ENABLE_FAULT_INT | | 1 | | | | | | |
| ENABLE_EXTPWR_INT | | | 1 | | | | | |
| ENABLE_OTG_INT | | | | 1 | | | | |
| ENABLE_AT_ILIM_INT | | | | | 1 | | | |
| ENABLE_INPUT_UVCL_INT | | | | | | 1 | | |

**Table 4. Interrupt Trigger Sources**

| MASK CATEGORY | STATUS TRIGGERS | STATUS REGISTERS |
|---|---|---|
| ENABLE_CHARGER_INT | CHARGER_STATUS[2:0] | 0x03 |
| ENABLE_FAULT_INT | OVP_ACTIVE<br>BAD_CELL<br>OTG_FAULT<br>NTC_HOT_FAULT | 0x03<br>0x04 |
| ENABLE_EXTPWR_INT | USBSNS_GOOD<br>WALLSNS_GOOD<br>EXT_PWR_GOOD | 0x04 |
| ENABLE_OTG_INT | OTG_ENABLED<br>ID_PIN_DETECT | 0x03 |
| ENABLE_AT_ILIM_INT | AT_INPUT_ILIM | 0x04 |
| ENABLE_INPUT_UVCL_INT | INPUT_UVCL_ACTIVE | 0x04 |

### Alternate Default Input Current Limit

For USB compatible operation, connect both the CLPROG1 and CLPROG2 pins to a single 1.21k 1% resistor, as shown in Figure 5. When input power is applied, the LTC4156 will default to the 100mA input current limit mode. The I²C bus master may then subsequently change the input current limit to any of the other modes listed in Table 8, where the 500mA and 900mA settings also correspond to USB compatible current limits. If input power is removed and reapplied, the LTC4156 will once again default to 100mA mode until commanded to do otherwise by I²C.

If the 100mA USB default current limit is insufficient for the application and USB compliance is not necessary, an alternate non-USB compliant default input current may be programmed with a second resistor on the CLPROG1 pin, as shown in Figure 6.

The resistor should be sized using the following equation:

$$R_{CLPROG1} = \frac{1.200V}{\left(I_{VBUSLIM} - I_{VBUSQ}\right)} \bullet (991)$$

When input power is applied, the LTC4156 will default to the current limit set by the resistor connected to the CLPROG1 pin. The I²C bus master may then subsequently change the input current limit to any of the other modes listed in Table 8, which require a second 1.21k programming resistor on the CLPROG2 pin. The I²C master may also change back to the default input current limit at any time by setting the appropriate USBILIM or WALLILIM bits to the CLPROG1 mode. If input power is removed and reapplied at any time, the LTC4156 will again default to the CLPROG1 custom input current limit.

The contents of USBILIM[4:0] and WALLILIM[4:0] always contain the currently selected input current modes, which may be different from the data last written by the I²C bus master if input power was subsequently removed or was not present. The I²C bus master can read the above two registers at any time to determine the active input current limit mode.

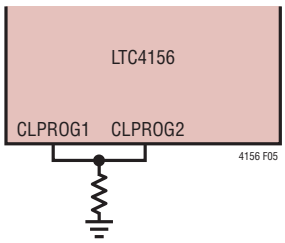



**Figure 5. USB Default Input Current Limit**

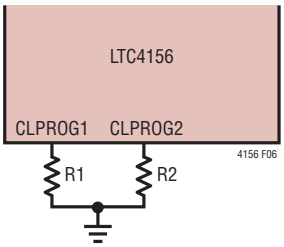



**Figure 6. Non-USB Default Input Current Limit**

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### Battery Charger Operation

The LTC4156 contains a fully featured constant-current/constant-voltage $LiFePO_4$ battery charger with automatic recharge, bad cell detection, trickle charge, programmable safety timer, thermistor temperature qualified charging, programmable end-of-charge indication, programmable float voltage, programmable charge current, detailed $I^2C$ status reporting, and programmable interrupt generation.

### Precharge/Low Battery

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below $V_{LOWBAT}$, typically 2.7V, the LTC4156 will report the LOWBAT condition via $I^2C$ (see Table 17). If the low battery voltage persists for more than one-half hour, the battery charger automatically terminates and indicates via the $I^2C$ port that the battery was unresponsive. When the battery voltage is low, charge current is reduced, both to protect the battery and to prevent excessive power dissipation in the external PMOS transistor. Figure 1 shows the relationship between battery voltage and charge current reduction. When input power (USB or WALL) is unavailable, the $I^2C$ LOWBAT indication will always be true, independent of the actual state of charge of the battery and can be disregarded.

### Constant-Current

When the battery voltage is above approximately 2.8V, the charger will attempt to deliver the programmed charge current in constant-current mode. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. Likewise, the USB and WALL input current limit programming will always be observed and only additional power will be available to charge the battery. When system loads are light, battery charge current will be maximized.

The upper limit of charge current is programmed by the combination of a resistor from PROG to ground and the PROG servo voltage value set in the $I^2C$ port. The maximum charge current will be given by the following expression:

$$I_{CHARGE} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000$$

$V_{PROG}$ can be set by the $I^2C$ port and ranges from 150mV to 1.2V in 75mV steps. The default value of $V_{PROG}$ is 1.2V. $V_{PROG}$ is controlled by bits ICHARGE[3:0] located at sub address 0x02. See Table 10.

In either the constant-current or constant-voltage charging modes, the voltage at the PROG pin will be proportional to the actual charge current delivered to the battery. The charge current can be determined at any time by monitoring the PROG pin voltage and using the following relationship:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1000$$

Recall, however, that in some cases the actual battery charge current, $I_{BAT}$, will be lower than the programmed current, $I_{CHARGE}$, due to limited input power available and prioritization of the system load drawn from $V_{OUT}$. $R_{PROG}$ should be set to match the capacity of the battery without regard to input power limitations.

### Constant-Voltage

Once the battery terminal voltage reaches the preset float voltage, the battery charger will hold the voltage steady and the charge current will decrease naturally toward zero. Four voltage settings are available for final float voltage selection via the $I^2C$ port using bits VFLOAT[1:0] (Table 11).

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### Full Capacity Charge Indication (C/x)

Since the PROG pin always represents the actual charge current flowing, even in the constant-voltage phase of charging, the PROG pin voltage represents the battery's state-of-charge during that phase. The LTC4156 has a full capacity charge indication comparator on the PROG pin which reports its results via the $I^2C$ port. Selection levels for the C/x comparator of 24mV, 60mV, 120mV and 240mV are available by $I^2C$ control bits CXSET[1:0] (Table 12). Recall that the PROG pin servo voltage can be programmed between 150mV to 1.2V. If the 1.2V servo setting represents the full-charge rate of the battery (1C), then the 120mV C/x setting would be equivalent to C/10. Likewise, the 240mV C/x setting would represent C/5, the 24mV setting C/50 and the 60mV C/20. C/x indication is masked unless the battery charger is in constant-voltage mode to prevent false indication caused by limited input power.

### Charge Termination

The battery charge cycle is terminated either at the expiration of a built-in programmable termination safety timer, or optionally at the full capacity charge indication (C/x). When the voltage on the battery reaches the user-programmed float voltage, the safety timer is started and the C/x comparator is enabled. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered. The safety timer's default expiration time of one hour may be altered from one-fourth to four hours in four settings using the $I^2C$ bits TIMER[1:0] (Table 9). The four hour timer termination setting will also terminate the charge cycle before the expiration of the four hour timer when the battery charge current falls to the programmed full capacity (C/x) charge indication threshold.

### Automatic Recharge

After the battery charger terminates, it will remain off, drawing only single microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a new charge cycle will automatically begin when the battery voltage falls below $V_{RECHRG}$ (typically 97.6% of the programmed $V_{FLOAT}$). The termination safety timer will also reset back to zero. To prevent brief excursions below $V_{RECHRG}$ from resetting the safety timer, the battery voltage must be below $V_{RECHRG}$ for more than 2.5ms. A new charge cycle will also be initiated if input (USB or WALL) power is cycled or if the charger is momentarily disabled using the $I^2C$ port. The flow chart in Figure 7 represents the battery charger's algorithm.

### NTC Thermistor Monitor

The LTC4156 includes a 7-bit expanded scale analog to digital converter (ADC) to monitor the battery temperature using an external negative temperature coefficient (NTC) thermistor placed close to the battery pack. To use this feature, connect the thermistor, $R_{NTC}$, between the NTC pin and ground, and a bias resistor, $R_{BIAS}$, between NTCBIAS and NTC, as shown in Figure 8. $R_{BIAS}$ should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C ($r_{25}$).

The thermistor measurement result is available via $I^2C$ port status reporting, except when the ship-and-store feature has been activated. When not in ship-and-store mode, the thermistor is automatically measured approximately every 2.4 seconds. The thermistor measurement result available to the $I^2C$ port is updated at the end of each sample period. The low duty cycle of thermistor bias reduces

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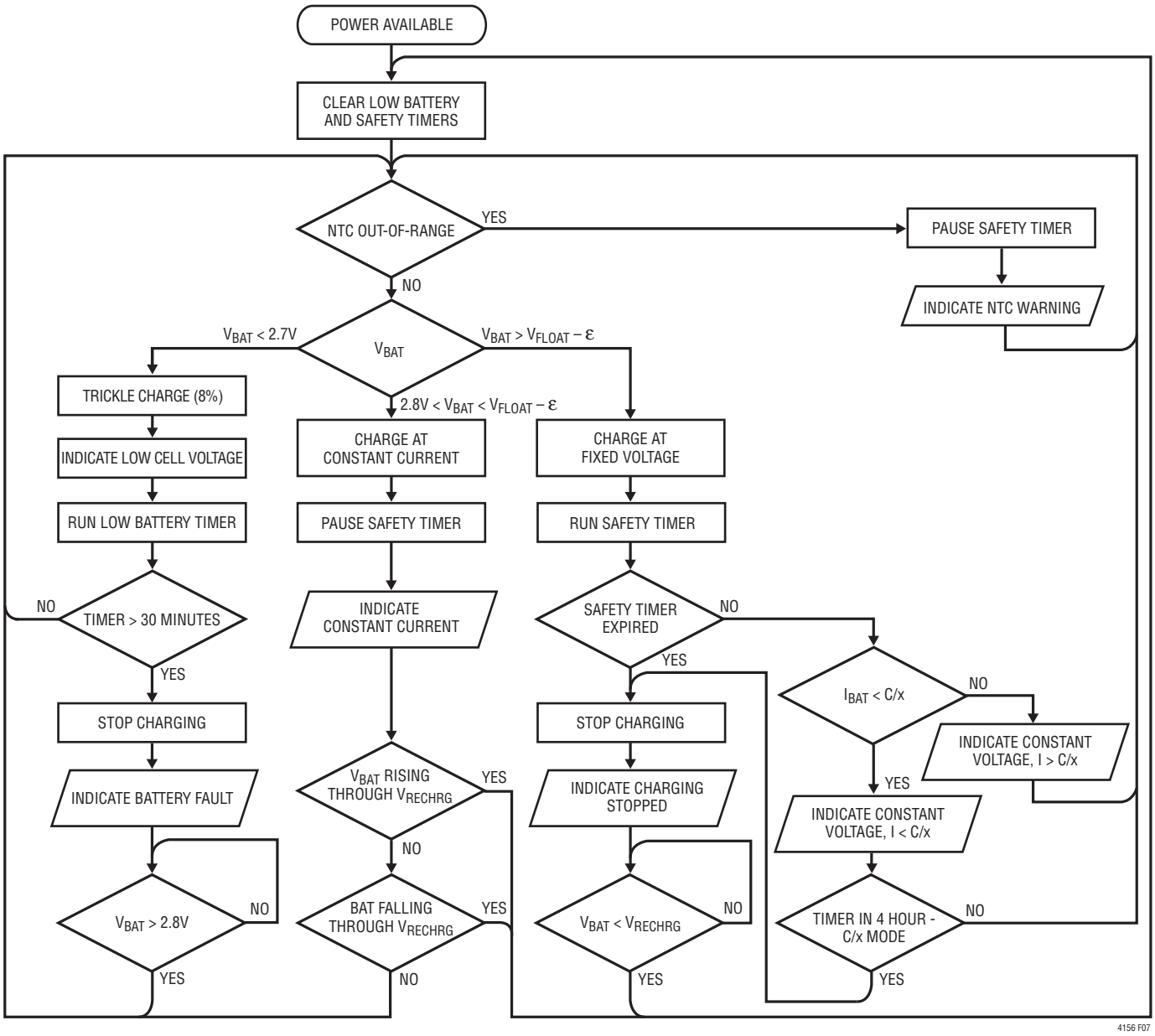



**Figure 7. Battery Charger Flow Chart**

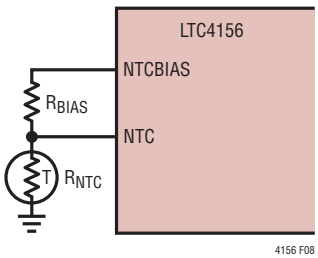



**Figure 8. Standard Thermistor Network**

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thermistor current, and its associated battery drain by a factor of 2000 from its DC value. A typical network using a 10k thermistor causes 115nA of battery drain. A 100k thermistor would reduce this drain to 11.5nA.

To improve measurement resolution over the temperature range of interest, the full-scale range of the analog-to-digital converter is restricted to the range 0.113 to 0.895 NTCBIAS. The NTC ADC result can be interpreted as follows:

$$\alpha_T \equiv \frac{r_T}{r_{25}} = \frac{\kappa_{SPAN} \bullet NTCVAL + \kappa_{OFFSET}}{1 - \kappa_{SPAN} \bullet NTCVAL - \kappa_{OFFSET}}$$

where NTCVAL is the decimal representation of the NTCVAL[6:0] status report in the range [0-127], ADC constant $\kappa_{SPAN}$ = 0.006162, ADC constant $\kappa_{OFFSET}$ = 0.1127, $r_T$ is the resistance of the thermistor at temperature T, and $\alpha_T$ is the resistance ratio of the thermistor at the two temperatures T and 25°C.

Thermistor manufacturer data sheets will either provide a temperature lookup table relating $\alpha_T$ to T, or will supply a curve fit parameter $\beta$ which can be used with the following equations to determine the thermistor temperature:

$$T = \frac{\beta}{\ln(\alpha_T) + \frac{\beta}{T_0}}$$

$$T = \frac{\beta}{\ln\left(\frac{\kappa_{SPAN} \bullet NTCVAL + \kappa_{OFFSET}}{1 - \kappa_{SPAN} \bullet NTCVAL - \kappa_{OFFSET}}\right) + \frac{\beta}{T_0}}$$

where:

T = Temperature result expressed in Kelvin

$T_0$ = Thermistor model nominal temperature, expressed in Kelvin. Typically 298.15K (25°C + 273.15°C)

$\beta$ = Thermistor model material constant, expressed in Kelvin.

In addition to thermistor value reporting, the LTC4156 automatically pauses battery charging if the thermistor reading falls outside of limits corresponding to the range 0°C to 60°C for a Vishay curve 2 thermistor. The NTC_TOO_COLD and NTC_HOT_FAULT conditions are encoded in the I²C status report NTCSTAT[1:0]. CHARGER_STATUS[2:0] will also report temperature warnings and faults when the battery charger is enabled. See Table 13 and Table 16. Optionally, a charger status interrupt request may be generated when the thermistor reading enters or exits this temperature range. If the temperature reading is above a limit corresponding to 60°C for a Vishay curve 2 thermistor, an optional NTC_HOT_FAULT interrupt may also be generated.

The NTC_TOO_COLD temperature indication is triggered when NTCVAL rises to decimal result 102. This corresponds to a $\alpha_{COLD,WARNING}$ = 2.86 and 0°C for a Vishay curve 2 thermistor. The low temperature indication is cleared when the NTCVAL falls to decimal result 98. This corresponds to $\alpha_{COLD,RESET}$ = 2.53 and 2°C for a Vishay curve 2 thermistor.

The NTC_HOT_FAULT temperature indication is triggered when NTCVAL falls to decimal result 19. This corresponds to $\alpha_{CRITICAL,FAULT}$ = 0.298 and 60°C for a Vishay curve 2 thermistor. The critically hot temperature indication is cleared when NTCVAL rises to decimal result 23. This corresponds to $\alpha_{CRITICAL,RESET}$ = 0.341 and 55.5°C for a Vishay curve 2 thermistor.

It is possible to modify the thermistor bias network to adjust either one or both of the above temperature thresholds. See Alternate NTC Thermistors and Biasing in the Applications Information section for implementation details.

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**Table 5. Input Undervoltage Current Limit Control**

| INPUT UNDERVOLTAGE CURRENT LIMIT CONTROL | | | | | | | | REG0 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x00 | DISABLE_INPUT_UVCL | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| DISABLE_INPUT_UVCL | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Enabled* | 0 | | | | | | | |
| Disabled | 1 | | | | | | | |

*Default setting

**Table 6. USB On-The-Go ID Pin Autonomous Start-Up**

| USB On-The-Go ID PIN AUTONOMOUS START-UP | | | | | | | | REG0 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x00 | LOCKOUT_ID_PIN | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| LOCKOUT_ID_PIN | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Autonomous Start-Up Allowed* | | | 0 | | | | | |
| Autonomous Start-Up Disabled | | | 1 | | | | | |

*Default setting

**Table 7. Input Current Limit Settings**

| INPUT CURRENT LIMIT SETTINGS | | | | | | | | REG0, REG1 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x00 | USB Input Current Limit USBILIM[4.0] | | | | | | |
| SUB ADDRESS | 0x01 | Wall Input Current Limit WALLILIM[4:0] | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| WALLILIM USBILIM | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 100mA Max (USB Low Power)* | | | | 0 | 0 | 0 | 0 | 0 |
| 500mA Max (USB High Power) | | | | 0 | 0 | 0 | 0 | 1 |
| 600mA Max | | | | 0 | 0 | 0 | 1 | 0 |
| 700mA Max | | | | 0 | 0 | 0 | 1 | 1 |
| 800mA Max | | | | 0 | 0 | 1 | 0 | 0 |
| 900mA Max (USB 3.0) | | | | 0 | 0 | 1 | 0 | 1 |
| 1000mA Typical | | | | 0 | 0 | 1 | 1 | 0 |
| 1250mA Typical | | | | 0 | 0 | 1 | 1 | 1 |
| 1500mA Typical | | | | 0 | 1 | 0 | 0 | 0 |
| 1750mA Typical | | | | 0 | 1 | 0 | 0 | 1 |
| 2000mA Typical | | | | 0 | 1 | 0 | 1 | 0 |
| 2250mA Typical | | | | 0 | 1 | 0 | 1 | 1 |
| 2500mA Typical | | | | 0 | 1 | 1 | 0 | 0 |
| 2750mA Typical | | | | 0 | 1 | 1 | 0 | 1 |
| 3000mA Typical | | | | 0 | 1 | 1 | 1 | 0 |
| 2.5mA Max (USB Suspend) | | | | 0 | 1 | 1 | 1 | 1 |
| SELECT CLPROG1** | | | | 1 | 1 | 1 | 1 | 1 |

*Default setting CLPROG1 and CLPROG2 shorted. Automatically reset when input power is absent.

**Default setting two CLPROG resistors. Automatically reset when input power is absent.

## OPERATION

**Table 8. Input Connector Priority Swap**

| INPUT CONNECTOR PRIORITY SWAP | | | | | | | REG1 | |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x01 | PRIORITY | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| PRIORITY | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Wall Input Prioritized* | 0 | | | | | | | |
| USB Input Prioritized | 1 | | | | | | | |

*Default setting

**Table 9. Battery Charger Safety Timer**

| BATTERY CHARGER SAFETY TIMER | | | | | | | REG1 | |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x01 | TIMER[1:0] | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| TIMER[1:0] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1 Hr* | | 0 | 0 | | | | | |
| 4 Hr or C/x Indication | | 0 | 1 | | | | | |
| 0.25 Hr | | 1 | 0 | | | | | |
| 0.50 Hr | | 1 | 1 | | | | | |

*Default setting.

**Table 10. Battery Charger Current Limit**

| BATTERY CHARGER CURRENT LIMIT | | | | | | | | REG2 | |
|---|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | | 0x02 | ICHARGE[3.0] | | | | | | |
| DIRECTION | | Write and Readback | | | | | | | |
| FULL-SCALE CURRENT (%) | $V_{PROG}$ SERVO (V) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Charger Disabled | 0.000 | 0 | 0 | 0 | 0 | | | | |
| 12.50 | 0.150 | 0 | 0 | 0 | 1 | | | | |
| 18.75 | 0.225 | 0 | 0 | 1 | 0 | | | | |
| 25.00 | 0.300 | 0 | 0 | 1 | 1 | | | | |
| 31.25 | 0.375 | 0 | 1 | 0 | 0 | | | | |
| 37.50 | 0.450 | 0 | 1 | 0 | 1 | | | | |
| 43.75 | 0.525 | 0 | 1 | 1 | 0 | | | | |
| 50.00 | 0.600 | 0 | 1 | 1 | 1 | | | | |
| 56.25 | 0.675 | 1 | 0 | 0 | 0 | | | | |
| 62.50 | 0.750 | 1 | 0 | 0 | 1 | | | | |
| 68.75 | 0.825 | 1 | 0 | 1 | 0 | | | | |
| 75.00 | 0.900 | 1 | 0 | 1 | 1 | | | | |
| 81.25 | 0.975 | 1 | 1 | 0 | 0 | | | | |
| 87.50 | 1.050 | 1 | 1 | 0 | 1 | | | | |
| 93.75 | 1.125 | 1 | 1 | 1 | 0 | | | | |
| 100.00* | 1.200* | 1 | 1 | 1 | 1 | | | | |

*Default setting.

## OPERATION

**Table 11. Battery Charger Float Voltage**

| Battery Charger Float Voltage | | | | | | | REG2 | |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x02 | VFLOAT[1:0] | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| BATTERY VOLTAGE (V) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 3.45* | | | | | 0 | 0 | | |
| 3.55 | | | | | 0 | 1 | | |
| 3.60 | | | | | 1 | 0 | | |
| 3.80 | | | | | 1 | 1 | | |

*Default setting.

**Table 12. Full Capacity Charge Indication Threshold**

| FULL CAPACITY CHARGE INDICATION THRESHOLD | | | | | | | | REG2 | |
|---|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | | 0x02 | CXSET[1:0] | | | | | | |
| DIRECTION | | Write and Readback | | | | | | | |
| FULL-SCALE CURRENT (%) | $V_{PROG}$ THRESHOLD (V) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 10* | 0.120* | | | | | | | 0 | 0 |
| 20 | 0.240 | | | | | | | 0 | 1 |
| 2 | 0.024 | | | | | | | 1 | 0 |
| 5 | 0.060 | | | | | | | 1 | 1 |

*Default setting.

**Table 13. Battery Charger Status Report**

| BATTERY CHARGER STATUS REPORT | | | | | | | | REG3 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x03 | CHARGER_STATUS[2:0] | | | | | | |
| DIRECTION | Read | | | | | | | |
| BATTERY CHARGER STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Charger Off | 0 | 0 | 0 | | | | | |
| Low Battery Voltage | 0 | 0 | 1 | | | | | |
| Constant Current | 0 | 1 | 0 | | | | | |
| Constant Voltage, VPROG>VC/X | 0 | 1 | 1 | | | | | |
| Constant Voltage, VPROG<VC/X | 1 | 0 | 0 | | | | | |
| NTC TOO COLD, Charging Paused | 1 | 1 | 0 | | | | | |
| NTC HOT FAULT, Charging Paused | 1 | 1 | 1 | | | | | |

**Table 14. USB On-The-Go ID Pin Detection**

| USB On-The-Go ID PIN DETECTION | | | | | | | | REG3 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x03 | ID_PIN_DETECT | | | | | | |
| DIRECTION | Read | | | | | | | |
| ID PIN STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| No Detection | | | | 0 | | | | |
| ID Pin Shorted to GND* | | | | 1 | | | | |

*LOCKOUT_ID_PIN has no effect on pin detection.

**Table 15. USB On-The-Go Enabled Status**

| USB On-The-Go ENABLED STATUS | | | | | | | | REG3 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x03 | OTG_ENABLED | | | | | | |
| DIRECTION | Read | | | | | | | |
| STEP-UP REGULATOR STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Step-Up Switching Regulator Inactive | | | | | 0 | | | |
| Step-Up Switching Regulator Active | | | | | 1 | | | |

**Table 16. NTC Thermistor Status Report**

| NTC THERMISTOR STATUS REPORT | | | | | | | | REG3 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x03 | NTCSTAT[1:0] | | | | | | |
| DIRECTION | Read | | | | | | | |
| NTC THERMISTOR STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| NTC Normal | | | | | | 0 | 0 | |
| NTC_TOO_COLD | | | | | | 0 | 1 | |
| NTC_HOT_FAULT | | | | | | 1 | 1 | |

**Table 17. Low Battery Detection**

| LOW BATTERY DETECTION | | | | | | | | REG3 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x03 | LOWBAT | | | | | | |
| DIRECTION | Read | | | | | | | |
| BATTERY VOLTAGE STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Normal | | | | | | | | 0 |
| Low Cell Voltage* | | | | | | | | 1 |

*Low cell voltage is only meaningful when input (WALL or USB) power is available and the battery charger is enabled, or when automatic or manual enable of the step-up regulator has been requested.

## OPERATION

**Table 18. External Power (Wall or USB) Available**

| EXTERNAL POWER (WALL OR USB) AVAILABLE | | | | | | | | REG4 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x04 | EXT_PWR_GOOD | | | | | | |
| DIRECTION | Read | | | | | | | |
| POWER AVAILABLE STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Battery Power Only | 0 | | | | | | | |
| External Power Available* | 1 | | | | | | | |

*Never true when On-The-Go step-up converter is active.

**Table 19. USB Input Voltage Valid**

| USB INPUT VOLTAGE VALID | | | | | | | | REG4 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x04 | USBSNS_GOOD | | | | | | |
| DIRECTION | Read | | | | | | | |
| USBSNS STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| USBSNS Voltage Invalid | | 0 | | | | | | |
| USBSNS Voltage Valid* | | 1 | | | | | | |

*Will be true with applied input voltage within valid range or On-The-Go in regulation.

**Table 20. WALL Input Voltage Valid**

| WALL INPUT VOLTAGE VALID | | | | | | | | REG4 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x04 | WALLSNS_GOOD | | | | | | |
| DIRECTION | Read | | | | | | | |
| WALLSNS STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| WALLSNS Voltage Invalid | | | 0 | | | | | |
| WALLSNS Voltage Valid | | | 1 | | | | | |

**Table 21. Input Current Limit Status**

| INPUT CURRENT LIMIT STATUS | | | | | | | | REG4 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x04 | AT_INPUT_ILIM | | | | | | |
| DIRECTION | Read | | | | | | | |
| INPUT CURRENT LIMIT STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Input Current Limit Inactive | | | | 0 | | | | |
| Input Current Limit Active | | | | 1 | | | | |

**Table 22. Input Undervoltage Current Limit (Brownout) Status**

| INPUT UNDERVOLTAGE CURRENT LIMIT (BROWNOUT) STATUS | | | | | | | | REG4 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x04 | INPUT_UVCL_ACTIVE | | | | | | |
| DIRECTION | Read | | | | | | | |
| INPUT UNDERVOLTAGE CURRENT LIMIT STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Input UVCL Inactive | | | | | 0 | | | |
| Input UVCL Active | | | | | 1 | | | |

**Table 23. Overvoltage Protection Fault**

| OVERVOLTAGE PROTECTION FAULT | | | | | | | | REG4 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x04 | OVP_ACTIVE | | | | | | |
| DIRECTION | Read | | | | | | | |
| INPUT OVERVOLTAGE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| No Fault | | | | | | 0 | | |
| Input (USB or WALL) Overvoltage | | | | | | 1 | | |

**Table 24. USB On-The-Go Step-Up Regulator Fault Shutdown**

| USB On-The-Go STEP-UP REGULATOR FAULT SHUTDOWN | | | | | | | | REG4 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x04 | OTG_FAULT | | | | | | |
| DIRECTION | Read | | | | | | | |
| STEP-UP REGULATOR STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| No Fault | | | | | | | 0 | |
| Regulator Over Current Shutdown | | | | | | | 1 | |

**Table 25. Battery Unresponsive to Charging**

| BATTERY UNRESPONSIVE TO CHARGING | | | | | | | | REG4 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x04 | BAD_CELL | | | | | | |
| DIRECTION | Read | | | | | | | |
| BATTERY STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| No Fault | | | | | | | | 0 |
| Low Cell Voltage Timeout | | | | | | | | 1 |

## OPERATION

**Table 26. NTC Analog-to-Digital Converter Result**

| NTC ANALOG-TO-DIGITAL CONVERTER RESULT | | | | | | | | REG5 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x05 | NTCVAL[6:0] | | | | | | |
| DIRECTION | Read | | | | | | | |
| NTC CONVERSION RESULT | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| NTCVAL[6:0]* | d | d | d | d | d | d | d | |

See NTC Thermistor Monitor in Operation section to convert ADC result to temperature.

**Table 27. NTC Temperature Out of Range for Battery Charging**

| NTC TEMPERATURE OUT OF RANGE FOR BATTERY CHARGING | | | | | | | | REG5 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x05 | NTC_WARNING | | | | | | |
| DIRECTION | Read | | | | | | | |
| NTC TEMP RANGE | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Temperature Normal | | | | | | | | 0 |
| Too Hot or Too Cold to Charge | | | | | | | | 1 |

**Table 28. Battery Charger Interrupt Mask**

| BATTERY CHARGER INTERRUPT MASK | | | | | | | | REG6 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x06 | ENABLE_CHARGER_INT | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| INTERRUPT ENABLE STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Charger Interrupts Disabled* | 0 | | | | | | | |
| Charger Interrupts Enabled | 1 | | | | | | | |

*Default.

Interrupt triggered by any change in CHARGER_STATUS[2:0].Any data written to sub address 0x06 has side effect of clearing any pending interrupt request.

**Table 29. Fault Interrupt Mask**

| FAULT INTERRUPT MASK | | | | | | | | REG6 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x06 | ENABLE_FAULT_INT | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| INTERRUPT ENABLE STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Fault Interrupts Disabled* | | 0 | | | | | | |
| Fault Interrupts Enabled | | 1 | | | | | | |

*Default.

Interrupt triggered by any change in OVP_ACTIVE, BAD_CELL, OTG_FAULT or NTC_HOT_FAULT. Any data written to sub address 0x06 has side effect of clearing any pending interrupt request.

**Table 30. External Power Available Interrupt Mask**

| EXTERNAL POWER AVAILABLE INTERRUPT MASK | | | | | | | | REG6 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x06 | ENABLE_EXTPWR_INT | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| INTERRUPT ENABLE STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| External Power Interrupts Disabled* | | | 0 | | | | | |
| External Power Interrupts Enabled | | | 1 | | | | | |

*Default.

Interrupt triggered by any change in USBSNSGD, WALLSNSGD, or EXTPWRGD. Any data written to sub address 0x06 has side effect of clearing any pending interrupt request.

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**Table 31. USB On-The-Go Interrupt Mask**

| USB On-The-Go INTERRUPT MASK | | | | | | | | REG6 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x06 | ENABLE_OTG_INT | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| INTERRUPT ENABLE STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| USB On-The-Go Interrupts Disabled* | | | | 0 | | | | |
| USB On-The-Go Interrupts Enabled | | | | 1 | | | | |

*Default.

Interrupt triggered by any change in EN_BOOST, ID_DETECT. Any data written to sub address 0x06 has side effect of clearing any pending interrupt request.

**Table 32. Input Current Limit Interrupt Mask**

| INPUT CURRENT LIMIT INTERRUPT MASK | | | | | | | | REG6 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x06 | ENABLE_AT_ILIM_INT | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| INTERRUPT ENABLE STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Input Current Limit Interrupts Disabled* | | | | | 0 | | | |
| Input Current Limit Interrupts Enabled | | | | | 1 | | | |

*Default.

Interrupt triggered by any change in AT_INPUT_ILIM. Any data written to sub address 0x06 has side effect of clearing any pending interrupt request.

**Table 33. Input Undervoltage Current Limit (Brownout Detection) Interrupt Mask**

| INPUT UNDERVOLTAGE CURRENT LIMIT (BROWNOUT DETECTION) INTERRUPT MASK | | | | | | | | REG6 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x06 | ENABLE_INPUT_UVCL_INT | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| INTERRUPT ENABLE STATUS | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Input Undervoltage Current Limit Interrupts Disabled* | | | | | | 0 | | |
| Input Undervoltage Current Limit Interrupts Enabled | | | | | | 1 | | |

*Default.

Interrupt triggered by any change in INPUT_UVCL_ACTIVE. Any data written to sub address 0x06 has side effect of clearing any pending interrupt request.

**Table 34. USB On-The-Go Step-Up Voltage Converter Manual Activation**

| USB On-The-Go STEP-UP VOLTAGE CONVERTER MANUAL ACTIVATION | | | | | | | | REG6 |
|---|---|---|---|---|---|---|---|---|
| SUB ADDRESS | 0x06 | REQUEST_OTG | | | | | | |
| DIRECTION | Write and Readback | | | | | | | |
| STEP-UP REGULATOR ACTIVATION | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Step-Up Regulator Activation Automatic or Disabled* | | | | | | | 0 | |
| Enable Step-Up Voltage Regulator | | | | | | | 1 | |

*Default.

Regulator cannot be activated if voltage is applied to either the USB or WALL inputs. Automatic activation controlled by LOCKOUT_ID_PIN. Any data written to sub address 0x06 has side effect of clearing any pending interrupt request.

## APPLICATIONS INFORMATION

### Alternate NTC Thermistors and Biasing

The LTC4156 provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to the NTC pin. Charging is paused if the temperature rises above an NTC_HOT_FAULT limit or falls below an NTC_TOO_COLD limit. By using a Vishay curve 2 thermistor and a bias resistor whose value is equal to the room temperature resistance of the thermistor ($r_{25}$), the upper and lower temperatures are preprogrammed to approximately 60°C and 0°C, respectively. The NTC_HOT_FAULT threshold also optionally generates an interrupt.

With minor modifications to the thermistor bias network as shown in Figure 9, it is possible to adjust either one or both of the temperature thresholds with the constraint that it is usually not possible to move the temperature thresholds closer together. Intuitively, this would require increased temperature sensitivity from the thermistor.

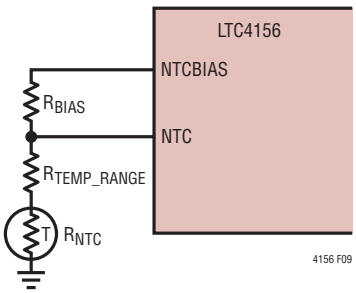



**Figure 9. Alternate NTC Bias Network**

In the explanation below, the following notation is used.

$r_{25}$

*NTC thermistor value at 25°C.*

$R_{BIAS}$

*Low drift bias resistor, connected between the NTCBIAS and NTC pins.*

$R_{TEMP_RANGE}$

*Optional dilution resistor, connected in series with the thermistor.*

$$\alpha_T \equiv \frac{r_T}{r_{25}}$$

*Thermistor resistance ratio at any temperature T relative to its reference temperature.*

$$\alpha_{TOO_COLD} \equiv \frac{r_{TOO_COLD}}{r_{25}}$$

*Thermistor resistance ratio at desired NTC_TOO_COLD threshold temperature relative to its reference temperature.*

$$\alpha_{HOT_FAULT} \equiv \frac{r_{HOT_FAULT}}{r_{25}}$$

*Thermistor resistance ratio at desired NTC_HOT_FAULT threshold temperature relative to its reference temperature.*

$$\alpha_{BIAS} \equiv \frac{R_{BIAS}}{r_{25}}$$

*Ratio of low drift bias resistor to $r_{25}$.*

$$\alpha_{TEMP_RANGE} \equiv \frac{R_{TEMP_RANGE}}{r_{25}}$$

*Ratio of optional low drift dilution resistor to $r_{25}$.*

Note that $r_{25}$, $r_T$, $r_{TOO_COLD}$ and $r_{HOT_FAULT}$ and are all resistance values of the thermistor at different temperatures, while $R_{BIAS}$ and $R_{TEMP_RANGE}$ are actual low drift resistors.

In all of the following calculations, it will be necessary to determine the thermistor's $\alpha_T$ at various temperatures. This parameter is dependent only upon the material properties of the thermistor. $\alpha_T$ for a given thermistor and temperature may be found in one of two ways. Thermistor manufacturers often provide a lookup table relating $\alpha_T$ to temperature in their data sheets. For any temperature T, $\alpha_T$ may be referenced directly.

The second way to obtain $\alpha_T$ for any T requires the use of a modeling equation and a material constant specific to the thermistor:

$$\alpha_T = e^{\beta\left[\left(\frac{1}{T}\right)-\left(\frac{1}{T_0}\right)\right]}$$

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where:

e = Natural logarithm base, approximately 2.71828

T = Temperature of interest, expressed in Kelvin

$T_0$ = Thermistor model nominal temperature, expressed in Kelvin. Typically 298.15K (25°C + 273.15°C)

$\beta$ = Model material constant, expressed in Kelvin. This model is a curve fit at $T_0$ and a second temperature. $\beta$ is close to 4000K for most thermistors. Higher $\beta$ results in increased temperature sensitivity at the expense of reduced linearity over a wide temperature range

### Simple Alternate Thermistor Bias Network

By simply adjusting the bias resistor, $R_{BIAS}$, and omitting the optional $R_{TEMP_RANGE}$, one of the temperature thresholds may be adjusted. The other temperature comparator threshold will be determined by the choice of the first temperature threshold and the NTCVAL thresholds fixed in the LTC4156. Increasing $R_{BIAS}$ above $r_{25}$ shifts both temperature thresholds colder while simultaneously slightly compressing the temperature span between thresholds. Likewise, decreasing $R_{BIAS}$ below $r_{25}$ shifts both temperature thresholds warmer while simultaneously slightly expanding the temperature span between thresholds. To program a single temperature threshold, obtain the value of either $\alpha_{TOO_COLD}$ or $\alpha_{HOT_FAULT}$ for the chosen temperature threshold using one of the aforementioned methods and substitute into the appropriate following equation to calculate the value $\alpha_{BIAS}$ and then $R_{BIAS}$.

$\alpha_{BIAS} = 0.34917 \bullet \alpha_{TOO_COLD}$

$\alpha_{BIAS} = 3.35249 \bullet \alpha_{HOT_FAULT}$

$R_{BIAS} = \alpha_{BIAS} \bullet r_{25}$

With $\alpha_{BIAS}$ for the newly programmed temperature threshold now determined, the other dependent temperature threshold may be found by substituting $\alpha_{BIAS}$ into the remaining equation.

The following equation may be used to convert any other NTC ADC result (NTCVAL) by substituting the $\kappa_{SPAN}$ and $\kappa_{OFFSET}$ values found in the Electrical Characteristics table.

$$\alpha_T = \left[ \frac{\kappa_{SPAN} \bullet NTCVAL + \kappa_{OFFSET}}{1 - \kappa_{SPAN} \bullet NTCVAL - \kappa_{OFFSET}} \right] \alpha_{BIAS}$$

$\alpha_T$ may then be used to determine the temperature using either the lookup table provided by the thermistor manufacturer or the curve fit model:

$$T = \frac{\beta}{\ln(\alpha_T) + \frac{\beta}{T_0}}$$

### Advanced Alternate Thermistor Bias Network

If an adjustment to $R_{BIAS}$ does not yield an acceptable span between temperature thresholds, a second low drift bias resistor may be added to the bias network between the NTC pin and the top of the thermistor. This resistor has the net effect of diluting the high thermal sensitivity of the thermistor with low drift resistance. The result is reduced thermal gain and a wider temperature span between the preprogrammed voltage thresholds of the LTC4156. Using this additional resistor, both of the temperature comparator thresholds may be adjusted. After determining the $\alpha_T$ values for the two temperature thresholds of interest, the following equations may be used to determine $\alpha_{BIAS}$ and $\alpha_{TEMP_RANGE}$.

$\alpha_{TEMP_RANGE} = 0.11626 \bullet \alpha_{TOO_COLD} - 1.11626 \bullet \alpha_{HOT_FAULT}$

$R_{TEMP_RANGE} = \alpha_{TEMP_RANGE} \bullet r_{25}$

$\alpha_{BIAS} = 0.38976 \bullet (\alpha_{TOO_COLD} - \alpha_{HOT_FAULT})$

$R_{BIAS} = \alpha_{BIAS} \bullet r_{25}$

It is possible to obtain a negative result for $R_{TEMP_RANGE}$ which is not physically realizable using the previous equations. A negative result indicates that the two chosen temperature thresholds are too close in temperature and require more thermal sensitivity than the thermistor can provide.

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$$\alpha_T = \left[\frac{\kappa_{SPAN} \bullet NTCVAL + \kappa_{OFFSET}}{1 - \kappa_{SPAN} \bullet NTCVAL - \kappa_{OFFSET}}\right] \alpha_{BIAS} - \alpha_{TEMP_RANGE}$$

$$T = \frac{\beta}{\ln\left(\left[\frac{\kappa_{SPAN} \bullet NTCVAL + \kappa_{OFFSET}}{1 - \kappa_{SPAN} \bullet NTCVAL - \kappa_{OFFSET}}\right] \alpha_{BIAS} - \alpha_{TEMP_RANGE}\right) + \frac{\beta}{T_0}}$$

The generalized form of the NTC equations provided in the Operations section are included above to facilitate interpretation of the thermistor analog to digital converter results using the custom bias network. If only $R_{BIAS}$ was modified, let $\alpha_{TEMP_RANGE} = 0$.

### Choosing the Input Multiplexer/Overvoltage Protection MOSFETs

The LTC4156 contains an internal charge pump voltage doubler to drive N-channel MOSFETS via the USBGT and WALLGT pins. The gate-source voltage available to drive the input multiplexer/protection FETS is approximately equal to the input voltage, typically 4V to 6V. To ensure that the FET channels are sufficiently enhanced to provide a low resistance conduction path, the FET threshold voltage should be less than approximately 2.5V. Total gate leakage current should be below 1µA to guarantee ample charge pump output voltage. The gate oxide breakdown voltage should be higher than 7V. The FET $R_{DS(ON)}$ will negatively impact the switching regulator and battery charger efficiency at high current levels. With two protection FETs in series (MN1 and MN3, MN2 and MN4), the total resistance is the sum of the individual $R_{DS(ON)}$s. This combined resistance should be negligible compared to the typical 80mΩ to 90mΩ resistance of the LTC4156 internal switches for maximum performance. The drain breakdown voltage of devices MN1 and MN2 must be appropriate for the level of overvoltage protection desired. The drains will be exposed to the full magnitude of applied input voltage. The drains of devices MN3 and MN4 are exposed only to the operating voltage range of the LTC4156. Therefore the drain breakdown voltage of devices MN3 and MN4 should be rated for at least 7V. Table 35 lists several suitable N-channel transistors. Transistors with lower $BV_{DSS}$ may be appropriate for devices MN3 and MN4 if reverse protection is not required. Note that resistors R1 and R2 must also be sized appropriately for power dissipation based on the level of overvoltage protection desired, as explained in the Operation section.

**Table 35. Recommended N-Channel Input Multiplexer MOSFETs**

| MANUFACTURER | PART NUMBER | $R_{DS(ON)}$ (mΩ) | $V_T$ (V) | $BV_{DSS}$ (V) |
|---|---|---|---|---|
| Fairchild | FDMC8651 | 4.3 | 1.1 | 30 |
| Fairchild | FDMC8030 | 10.7 | 2.8 | 40 |
| Vishay | Si7938DP | 5.6 | 2.5 | 40 |

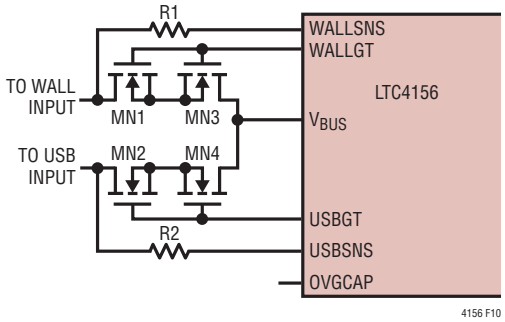



**Figure 10. Dual-Input Overvoltage Protection**

## APPLICATIONS INFORMATION

### Alternate Input Power Configurations

For applications requiring only a single input, the external circuit required for overvoltage protection is considerably simplified. Only a single N-channel MOSFET and resistor are required for positive voltage protection, as shown in Figure 11, and OVGCAP may be left unconnected. Applications using the USB On-The-Go step-up regulator should connect R1 to USBSNS and the gate of MN1 to USBGT. Applications not using USB On-The-Go may use either the USBSNS/USBGT pins or the WALLSNS/WALLGT pins. The unused pins may be left unconnected.

For dual-input applications requiring reverse-voltage protection, no additional power transistors are required. The circuit in Figure 12 provides positive protection up to the drain breakdown voltage rating of MN3 and MN4 and negative protection down to the drain breakdown voltage rating of MN1 and MN2. Q1 and Q2 are small-signal transistors to protect the gate oxides of MN1 and MN2. Note that it is necessary to orient the N-channel MOSFETs with the drain connections common and the source/body connections to the input connector and the $V_{BUS}$ pin.

### Choosing the Inductor

The LTC4156 is designed to operate with a 1µH inductor, with core saturation, winding resistance, and thermal rise characteristics appropriate for the application's peak currents. The inductor current ripple magnitude is approximately 400mA under normal conditions, resulting in a peak inductor current 200mA higher than the average output current of the switching regulator. The average output current of the step-down regulator is higher than the average input current by the ratio $V_{BUS}/V_{OUT}$, neglecting efficiency losses. The LTC4156 can tolerate transient excursions beyond the inductor's core saturation level, but the inductor current will increase rapidly to the LTC4156's peak current clamp as incremental inductance tends toward zero. If an overload condition persists with a small inductor, it is possible that the inductor could be damaged by its own resistive temperature rise.

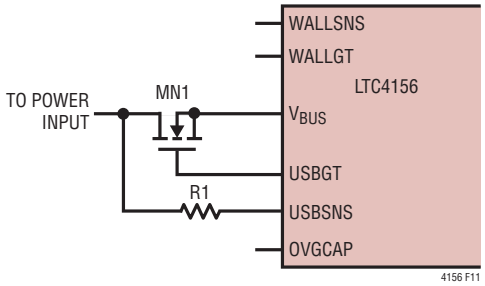



**Figure 11. Single-Input Overvoltage Protection**

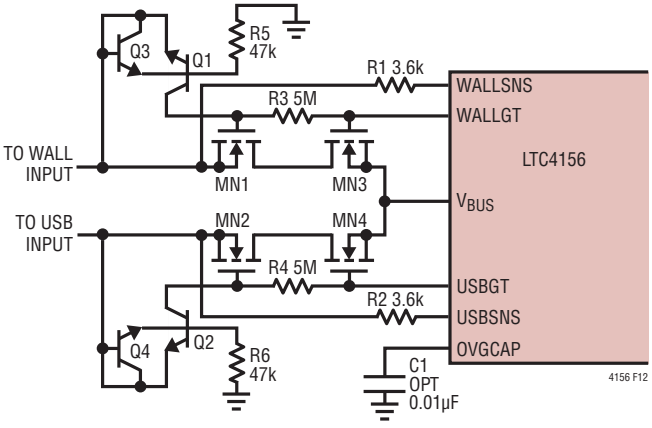



**Figure 12. Dual-Input Positive and Negative Voltage Protection**

## APPLICATIONS INFORMATION

The inductor core should be made from a material such as ferrite, suitable for switching at 2.25MHz without excessive hysteretic losses. Table 36 lists several suitable inductors.

**Table 36. Recommended Inductors**

| MANUFACTURER | PART NUMBER | $R_{DC}$ (mΩ) | $I_{MAX}$ (A) | PACKAGE (mm) |
|---|---|---|---|---|
| Vishay | IHLP2525AHE-B1ROMO1 | 17.5 | 7 | 6.5 × 6.9 × 3.2 |
| Coilcraft | XFL4020-102ME | 10.8 | 5.4 | 4 × 4 × 2.1 |
| TDK | TDKLTF5022T1R2N4R2-LF | 21 | 4.2 | 5 × 5.2 × 2.2 |

$I_{MAX}$ is the lower of the typical 30% saturation current and self-heating current specifications.

### Choosing the Battery Charger MOSFETs

The LTC4156 requires a single external P-channel MOSFET connected between the CHGSNS and BATSNS pins to conduct battery charge and ideal diode currents. The threshold voltage magnitude should be less than approximately 2.5V. (The P-channel threshold might be expressed as a negative number, $V_{GS(th)}$, or as a positive number $V_{SG(th)}$). Gate leakage current should be below 500nA. Drain voltage breakdown and gate oxide breakdown voltages should both be above 5V in magnitude. The LTC4156 contributes approximately 40mΩ resistance in the current sense circuitry in series with the battery charger FET. Channel resistance, $R_{DS(ON)}$, should be small relative to the 40mΩ for maximum efficiency both charging the battery and delivering power from the battery to the system load. Table 37 lists several suitable P-channel transistors.

Optionally, a second P-channel MOSFET may be connected in series with the first if the application requires that power be cut off from any downstream devices on $V_{OUT}$ in low power ship-and-store mode. Further details about low power ship-and-store mode may be found in the Operation section. The requirements for the second device are the same as those enumerated above, with the caveats that total gate leakage current is the sum of the individual leakage currents and total $R_{DS(ON)}$ is the sum of the individual $R_{DS(ON)}$s.

**Table 37. Recommended P-Channel Battery Charger MOSFETs**

| MANUFACTURER | PART NUMBER | $R_{DS(ON)}$ (mΩ) | $V_T$ (V) | $BV_{DSS}$ (V) |
|---|---|---|---|---|
| Fairchild | FDMC510P | 7.6 | –0.5 | –20 |
| Vishay | Si7123DN | 11.2 | –1 | –20 |
| Vishay | Si5481DU | 24 | –1 | –20 |

### $V_{BUS}$ and $V_{OUT}$ Bypass Capacitors

The style and value of the capacitors used with the LTC4156 determine several important parameters such as regulator control loop stability and input voltage ripple. Because the LTC4156 uses a step-down switching power supply from $V_{BUS}$ to $V_{OUT}$, its input current waveform contains high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor be used to bypass $V_{BUS}$. Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on $V_{BUS}$ directly controls the amount of input ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple. The USB specification allows a maximum of 10µF to be connected directly across the USB power bus. If the overvoltage protection circuit is used to protect $V_{BUS}$, then its soft-starting nature can be exploited and a larger $V_{BUS}$ capacitor can be used if desired. If one or both of the input channels are never used for USB, additional capacitance placed upstream of the overvoltage protection NMOS devices can absorb significant high frequency current ripple.

To prevent large $V_{OUT}$ voltage steps during transient load conditions, it is also recommended that a ceramic capacitor be used to bypass $V_{OUT}$. The output capacitor is used in the compensation of the switching regulator. At least 22µF with low ESR are required on $V_{OUT}$. Additional capacitance will improve load transient performance and stability.

## APPLICATIONS INFORMATION

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions.

The actual in-circuit capacitance of a ceramic capacitor should be measured with a small AC signal and DC bias, as is expected in-circuit. Many vendors specify the capacitance versus voltage with a $1V_{RMS}$ AC test signal and, as a result, overstate the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure, or request from the vendor, the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

### Programming the Input and Battery Charge Current Limits

The LTC4156 features independent resistor programmability of the input current limit and battery charge current limit to facilitate optimal charging from a wide variety of input power sources. The battery charge current should be programmed based on the size of the battery and its associated safe charging rate. With the full-scale (default) charge current programmed with a resistor between PROG and GND, all other $I^2C$ selectable charge current settings are lower and may be appropriate for custom charge algorithms at extreme temperature or battery voltage. If the battery charge current limit requires more power than is available from the selected input current limit, the input current limit will be enforced and the battery will charge with less than the programmed current. Thus, the battery charger should be programmed optimally for the battery without concern for the input source.

### Resistive Inputs and Test Equipment

Care must be exercised in the laboratory while evaluating the LTC4156 with inline ammeters. The combined resistance of the internal current sense resistor and fuse of many meters can be 0.5Ω or more. At currents of 3A to 4A, it is possible to drop several volts across the meter, possibly resulting in unusual voltage readings or artificially high switch duty cycles.

A resistive connection to the source of input power can be particularly troublesome. With the undervoltage current limit feature enabled, the switching regulator output power will be automatically reduced to prevent $V_{BUS}$ from falling below 4.3V. This feature greatly improves tolerance of resistive input power sources (from either undersized wiring and connectors or test equipment) and facilitates stable behavior, but if engaged, it will result in much less power delivery to the system load and battery, depending on the magnitude of input resistance.

If the undervoltage current limit feature is disabled and the input power source is resistive, the voltage will continue to fall through the falling undervoltage lockout threshold, eventually shutting down that input channel and resetting its input current limit back to the default setting. When the input voltage recovers, the channel will restart in the default current limit setting.

## APPLICATIONS INFORMATION

### Board Layout Considerations

The Exposed Pad on the backside of the LTC4156 package must be securely soldered to the PC board ground. This is the primary ground pin in the package, and it serves as the return path for both the control circuitry and the synchronous rectifier. Furthermore, due to its high frequency switching circuitry, it is imperative that the input capacitor be as close to the LTC4156 as possible, and that there be an unbroken ground plane under the LTC4156 and its external input bypass capacitors. Additionally, minimizing the area between the SW pin trace and inductor will limit high frequency radiated energy.

The output capacitor carries the inductor ripple current. While not as critical as the input capacitor, an unbroken ground plane from this capacitor's ground return to the inductor, input capacitor, and LTC4156 exposed pad will reduce output voltage ripple.

High frequency currents, such as the input current on the LTC4156, tend to find their way on the ground plane along a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur (see Figure 13). There should be a group of vias directly under the grounded backside leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (layer 2).

The BATGATE pin has limited drive current. Care must be taken to minimize leakage to adjacent PC board traces, which may significantly compromise the 15mV ideal diode forward voltage. To minimize leakage, the trace can be guarded on the PC board by surrounding it with $V_{OUT}$ connected metal, which should generally be less than 1V higher than BATGATE.

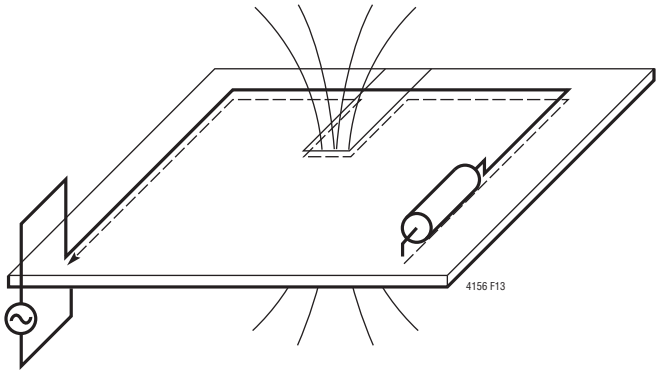
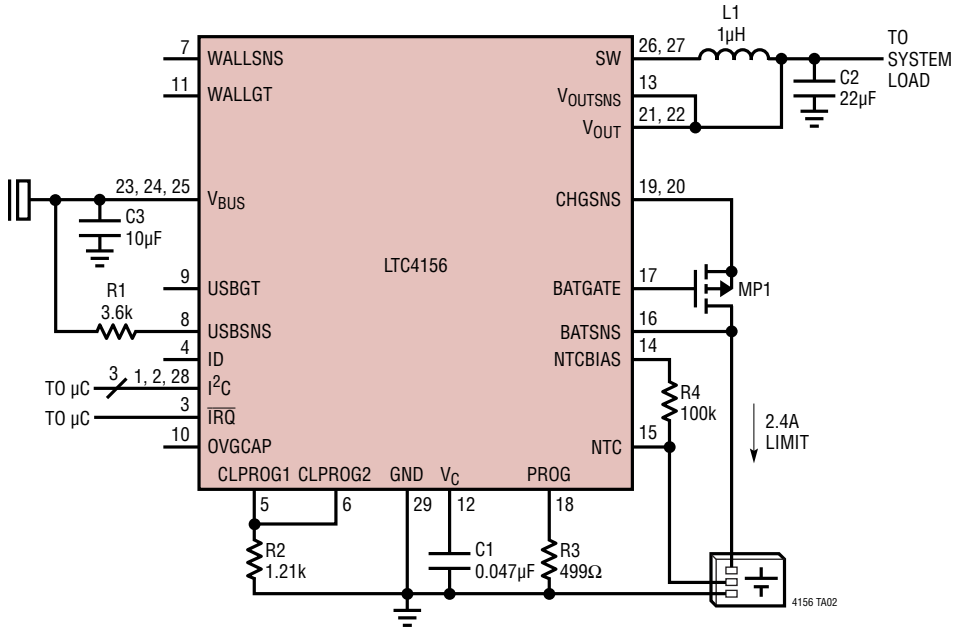



**Figure 13. Higher Frequency Ground Currents Follow Their Incident Path. Slices in the Ground Plane Cause High Voltage and Increased Emissions**

# TYPICAL APPLICATIONS

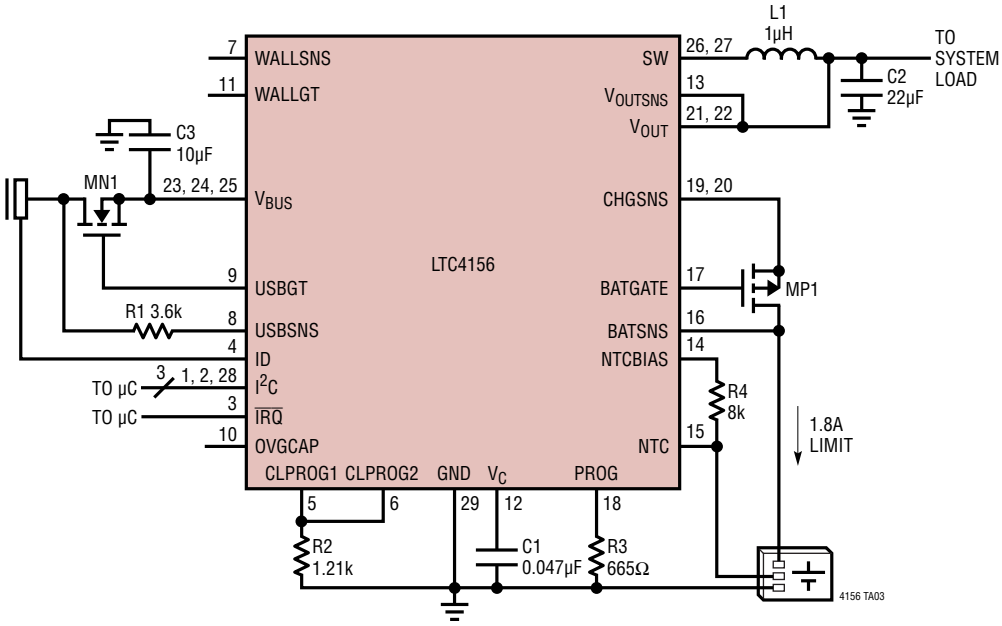
**Single Input USB Default Current Limit with Minimum Component Count**




L1: COILCRAFT XFL4020-102ME
MP1: VISHAY Si5481DU-T1-GE3

# TYPICAL APPLICATIONS

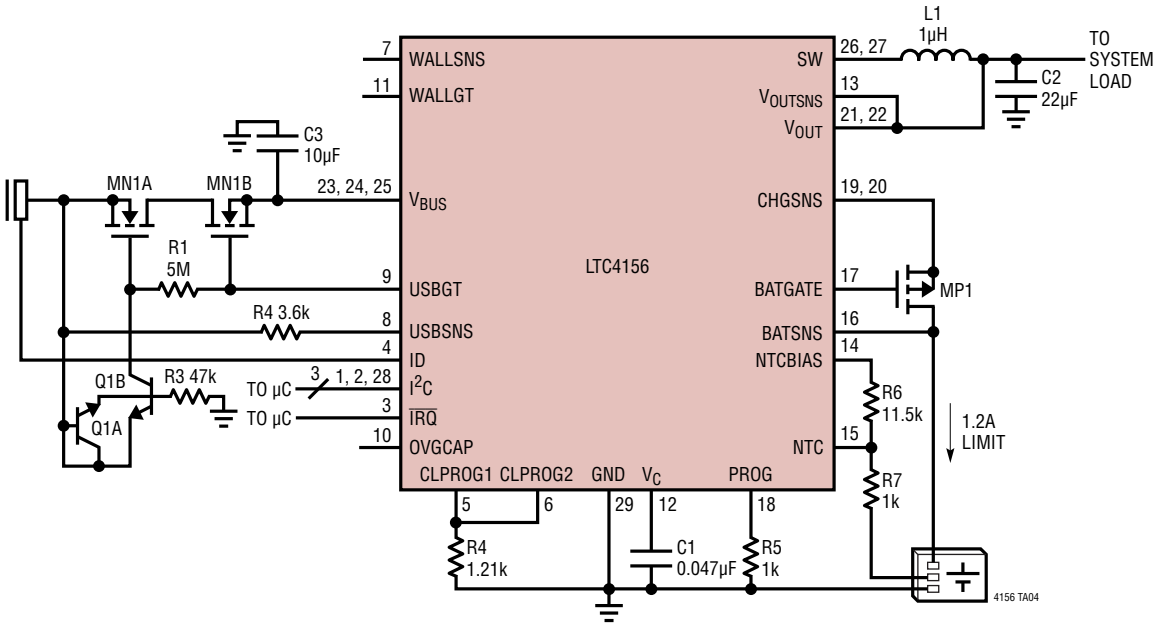
**Single Input Overvoltage Protection with USB 100mA Default Input Current Limit and 5°C/67°C Thermistor Thresholds**




L1: COILCRAFT XFL4020-102ME
MN1: Si4430BDY
MP1: VISHAY Si5481DU-T1-GE3
PACK NTC: VISHAY NTCS0402E3103FLT

# TYPICAL APPLICATIONS

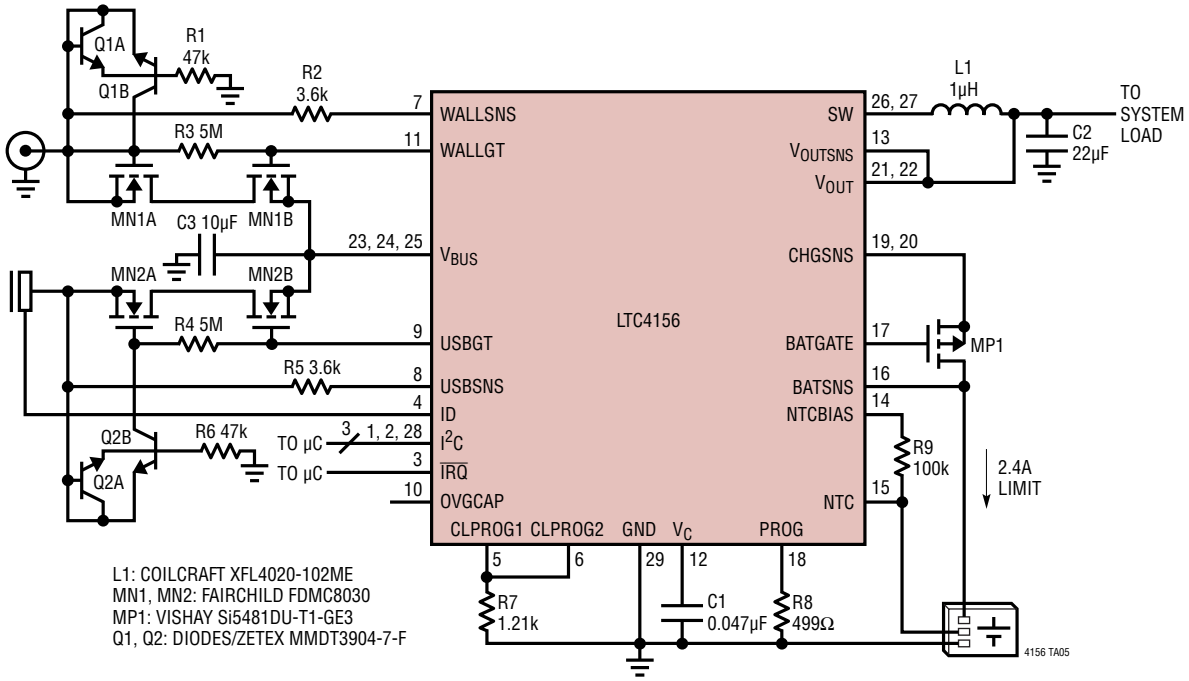
**Single Input Over/Reverse Voltage Protection, USB Default Input Current Limit and –3°C/66°C Thermistor Thresholds**




L1: COILCRAFT XFL4020-102ME
MN1: FAIRCHILD FDMC8030
MP1: VISHAY Si5481DU-T1-GE3
PACK NTC: VISHAY NTCS0402E3103FLT
Q1: DIODES/ZETEX MMDT3904-7-F

## TYPICAL APPLICATIONS

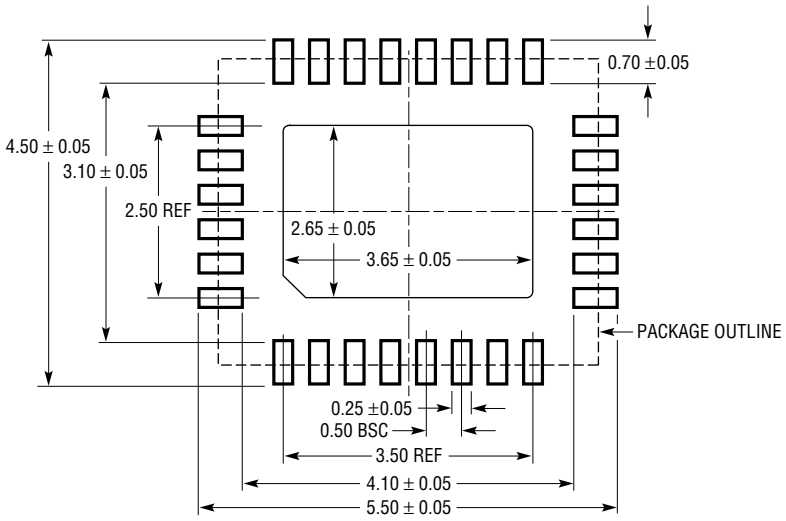
**Dual Input Over/Undervoltage Protection with 100mA USB Default Current Limit**



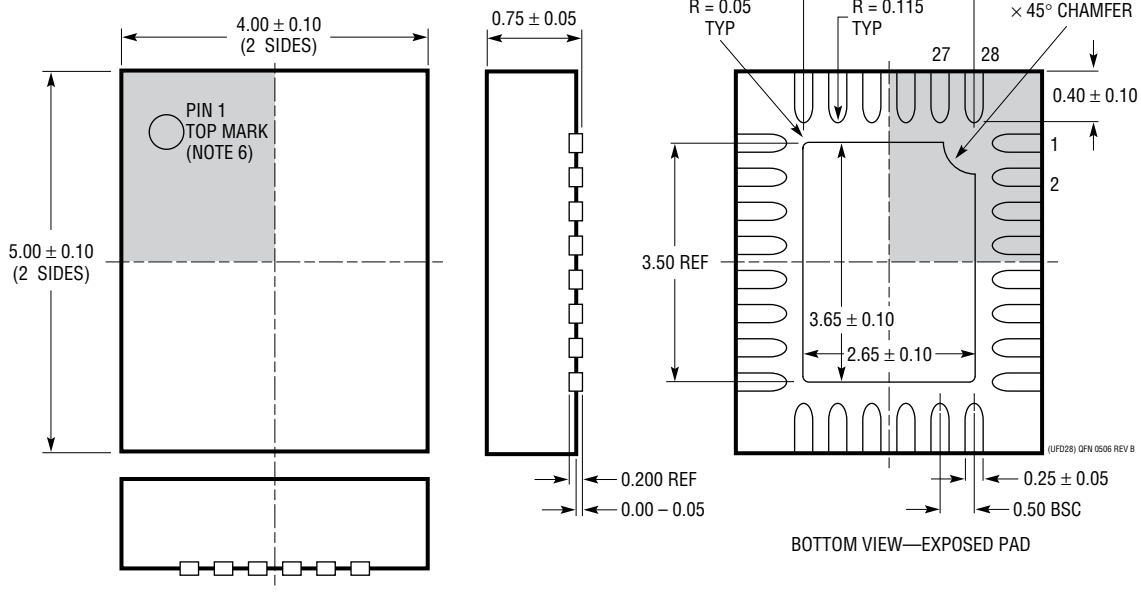
# PACKAGE DESCRIPTION

**Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.**

**UFD Package**
**28-Lead Plastic QFN (4mm × 5mm)**
(Reference LTC DWG # 05-08-1712 Rev B)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED




BOTTOM VIEW—EXPOSED PAD

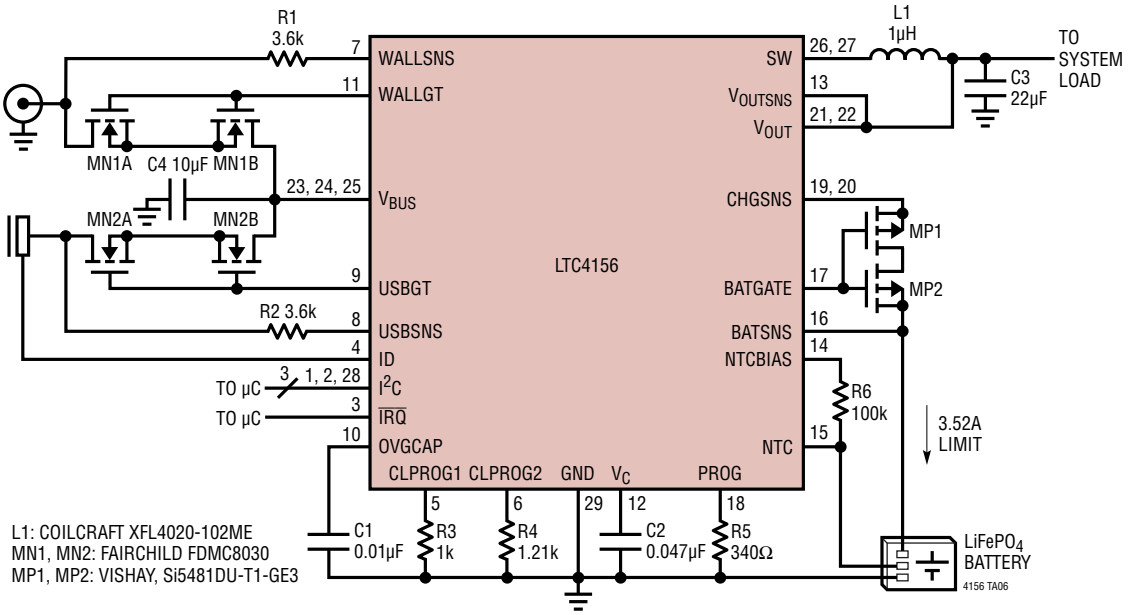
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE



Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

## TYPICAL APPLICATION

**Dual Input Overvoltage Protection with 1.21A Default Input Current Limit and Output Voltage Disconnect**




## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC4155 | Dual Input Power Manager/3.5A Li-Ion Battery Charger with I²C Control and USB OTG | High Efficiency 3.5A Charger Specifically Designed for Li-Ion/Polymer; Monolithic Switching Regulator Makes Optimal Use of Limited Power and Thermal Budget; Float Voltages: 4.05V, 4.10V, 4.15V, 4.20V; I²C/SMBus Control and Status Feedback; 4mm × 5mm QFN-28 Package. |
| LTC4085/LTC4085-1 | Linear USB Power Manager with Ideal Diode Controller and Li-Ion Charger | Charges Single Cell Li-Ion Batteries Directly from a USB Port, Thermal Regulation, 200mΩ Ideal Diode with <50mΩ Option, LTC4085-1 Has 4.1V $V_{FLOAT}$, 3mm × 4mm DFN-14 Package |
| LTC4088 | High Efficiency USB Power Manager and Battery Charger | Maximizes Available Power from USB Port, Bat-Track™, Instant-On Operation, 1.5A Max Charge Current, 3mm × 4mm DFN-14 Package |
| LTC4089/LTC4089-1 LTC4089-5 | High Voltage USB Power Manager with Ideal Diode Controller and High Efficiency Li-Ion Battery Charger | High Efficiency 1.2A Charger from 6V to 36V (40V Max) Input; Bat-Track Adaptive Output Control (LTC4089); Fixed 5V Output (LTC4089-5/LTC4089-1); LTC4089-1 for 4.1V Float Voltage Batteries, 3mm × 6mm DFN-22 Package; |
| LTC4090/LTC4090-5 | High Voltage USB Power Manager with Ideal Diode Controller and High Efficiency Li-Ion Battery Charger | High Efficiency 1.2A Charger from 6V to 38V (60V Max) Input Bat-Track Adaptive Output Control; LTC4090-5 Has No Bat-Track. 3mm × 6mm DFN-22 Package |
| LTC4098/ LTC4098-3.6 | USB-Compatible Switchmode Power Manager with OVP | LTC4098-3.6 Option for $LiFePO_4$ Cells; 66V OVP. 1.5A Max Charge Current from Wall, 600mA Charge Current from USB, 3mm × 4mm QFN-20 Package |
| LTC4099 | I²C Controlled USB Switchmode Power Manager with OVP | 66V OVP. I²C for Control and Status Readback, 1.5A Max Charge Current from Wall, 600mA Charge Current from USB, 3mm × 4mm QFN-20 Package |
| LTC4160/LTC4160-1 | Switchmode Power Manager with OVP and USB-OTG | USB-OTG 5V Output, Overvoltage Protection, Maximizes Available Power from USB Port, Bat-Track, Instant-On Operation, 1.5A Max Charge Current from Wall, 600mA Charge Current from USB, 3mm × 4mm QFN-20 Package |




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