LTC2374/LTC2373/LTC2372
16-Bit/18-Bit, 1.6Msps/1Msps/500ksps 8-Channel, SAR ADCs

DESCRIPTION

Demonstration circuit 2071A features the LTC®2373 family. The LTC2374/LTC2373/LTC2372 are low noise, high speed, 8-channel, 16-/18-bit successive approximation register (SAR) ADCs. The following text refers to the LTC2373-18 but applies to all parts in the family, the only differences being the number of bits and the maximum sample rate. Operating from a single 5V supply, the LTC2373-18 has a highly configurable, low crosstalk, 8-channel input multiplexer, supporting fully differential, pseudo-differential unipolar and pseudo-differential bipolar analog input ranges.

The DC2071 demonstrates the DC and AC performance of the LTC2373-18 in conjunction with the DC590 and DC890 data collection boards. Use the DC590 to demonstrate DC performance such as peak-to-peak noise and DC linearity. Use the DC890 if precise sampling rates are required or to demonstrate AC performance such as SNR, THD, SINAD and SFDR. The demonstration circuit 2071 is intended to demonstrate recommended grounding, component placement and selection, routing and bypassing for this ADC. Several suggested driver circuits for the analog inputs will be presented.

Design files for this circuit board, including the schematic and BOM, are available at http://www.linear.com/demo/DC2071A

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ASSEMBLY OPTIONS

Table 1. DC2071A Assembly Options

Assembly Version	U1 Part Number	Max Conversion Rate	Number of Bits	Max CLK IN Frequency
DC2071A-A	LTC2373CUH-18	1Msps	18	62MHz
DC2071A-B	LTC2372CUH-18	0.5Msps	18	31MHz
DC2071A-C	LTC2374CUH-16	1.6Msps	16	86.4MHz
DC2071A-D	LTC2373CUH-16	1Msps	16	50MHz
DC2071A-E	LTC2372CUH-16	0.5Msps	16	25MHz

BOARD PHOTO

DEFAULT INPUT LEVELS

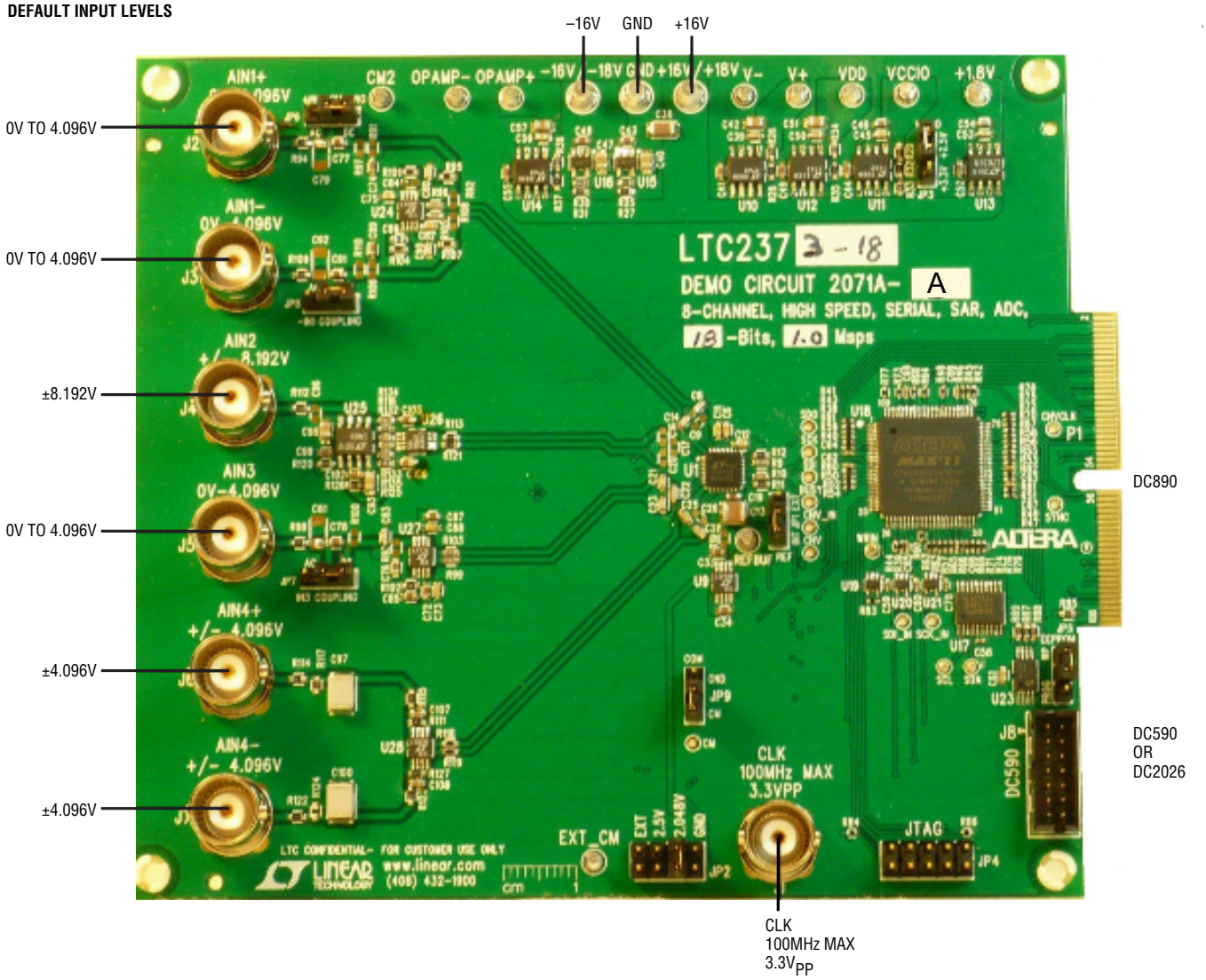

Figure 1. DC2071A Connection Diagram

DC890 QUICK START PROCEDURE

Check to make sure that all switches and jumpers are set as shown in the connection diagram of Figure 1. The default connections configure the ADC to use the onboard reference and regulators to generate the required common mode voltages. The analog input is DC coupled. Connect the DC2071A to a DC890 USB High Speed Data Collection Board using connector P1. Then, connect the DC890 to a host PC with a standard USB A/B cable. Apply ±16V to the indicated terminals. Then apply a low jitter signal source to J2–J7. Observe the recommended input voltage range for each analog input. Connect a low jitter $2.5V_{PP}$ sine wave or square wave to connector J1. See Table 1 for the appropriate clock frequency. Note that J1 has a 50Ω termination resistor to ground.

Run the PScope™ software (Pscope.exe version K88 or later) which can be downloaded from www.linear.com/designtools/software.

Complete software documentation is available from the Help menu. Updates can be downloaded from the Tools menu. Check for updates periodically as new features may be added.

The PScope software should recognize the DC2071A and configure itself automatically.

Click the Collect button (See Figure 7) to begin acquiring data. The Collect button then changes to Pause, which can be clicked to stop data acquisition.

DC590 QUICK START PROCEDURE

IMPORTANT! To avoid damage to the DC2071A, make sure that VCCIO (JP6) of the DC590 is set to 3.3V before connecting the DC590 to the DC2071A.

To use the DC590 with the DC2071A, it is necessary to apply ±16V and ground to the ±16V and GND terminals on the DC2071A. Connect the DC590 to a host PC with a standard USB A/B cable. Connect the DC2071A to a DC590 USB serial controller using the supplied 14-conductor ribbon cable. Apply a signal source to J2-J7. No clock is required on J1 when using the DC590. The clock is provided by the DC590.

Run the QuikEval™ software (quikeval.exe version K109 or later) which is available from www.linear.com/designtools/software. The correct control panel will be loaded automatically. Click the Collect button (Figure 10) to begin reading the ADC.

DC2071A SETUP

DC Power

The DC2071A requires ±16VDC and draws +100mA/–40mA. Most of the supply current is consumed by the CPLD, op amps, regulators and discrete logic on the board. The +16VDC input voltage powers the ADC through LT1763 regulators which provide protection against accidental reverse bias. Additional regulators provide power for the CPLD and op amps. See Figure 1 for connection details.

Clock Source

You must provide a low jitter $2.5V_{PP}$ sine or square wave to the clock input, J1. The clock input is AC coupled so the DC level of the clock signal is not important. A generator like the Rohde & Schwarz SMB100A high speed clock source is recommended. Even a good generator can start to produce noticeable jitter at low frequencies. Therefore it is recommended for lower sample rates to divide down a higher frequency clock to the desired sample rate. The ratio of clock frequency to conversion rate is 62:1 for 18-bit parts and 50:1 or 54:1 for 16-bit parts. If the clock input is to be driven with logic, it is recommended that the 49.9Ω terminator (R3) be removed. Slow rising edges may compromise the SNR of the converter in the presence of high-amplitude higher frequency input signals.

Data Output

Parallel data output from this board (0V to 2.5V default), if not connected to the DC890, can be acquired by a logic analyzer and subsequently imported into a spreadsheet or mathematical package depending on what form of digital signal processing is desired. Alternatively, the data can be fed directly into an application circuit. Use pin-50 of P1 to latch the data. The data should be latched using the positive edge of this signal. The data output signal levels at P1 can also be increased to 0V to 3.3V if the application circuit requires a higher voltage. This is accomplished by moving JP3 to the 3.3V position.

Reference

The default reference is the LTC2373-18 internal 4.096V reference. Alternatively, if an external reference voltage is desired, the LTC6655-4.096 reference (U9) can be used by setting the REF jumper (JP1) to the EXT position and installing a 0Ω resistor in the R19 position.

Analog Inputs

The four default driver circuits for the analog inputs of the LTC2373-18 on the DC2071A are shown in Figures 2 to 5. The circuit of Figure 2 is a fully differential driver with 0V to 4.096V inputs. The output of this circuit is band limited to approximately 13MHz. The circuit of Figure 3 is a single-ended to differential driver with an input signal range of ±8.192V. This circuit is band limited to 1.6MHz at the output. The circuit of Figure 4 is a single-ended to differential driver with an input range of 0V to 4.096V. The output bandwidth of this circuit is 1.6MHz. The circuit of Figure 5 is a single-ended/fully differential input driver circuit with an input range of ±4.096V. The input bandwidth of this circuit is 4.8kHz. The output is band limited to 3MHz. The default for this circuit is single-ended drive. Drive the A_{IN4}^- input to ±4.096V. Alternatively, by removing R117 and changing R114 to 100Ω this circuit can be driven fully differentially.

The A_{IN1} and A_{IN3} driver circuits can be DC or AC coupled. The default setting is DC coupled. AC coupling the inputs may degrade the distortion performance of the ADC due to nonlinearity of the coupling capacitors. AC coupling can be implemented on the DC2071A by putting the coupling jumpers (JP6, JP8 for A_{IN1} and JP7 for A_{IN3}) in the AC position, and adding two 1kΩ resistors at the optional resistor locations on the other side of each coupling capacitor (R91, R97, R106, R110 for A_{IN1} and R93, R100 for A_{IN3}).

Another option available on the demo board is to drive each input single-ended and then convert the single-ended inputs to fully differential at the MUX outputs. This allows the user to have eight single-ended inputs but still have the SNR of a fully differential input. To accomplish this, remove C31, R8, R15 and R128 then add C15, C24, C27, C29, R7, R13, R16, R17, R18, R129, R130, R131 and U7. The values for the passive devices are shown in the schematic of Figure 6.

DC2071A SETUP

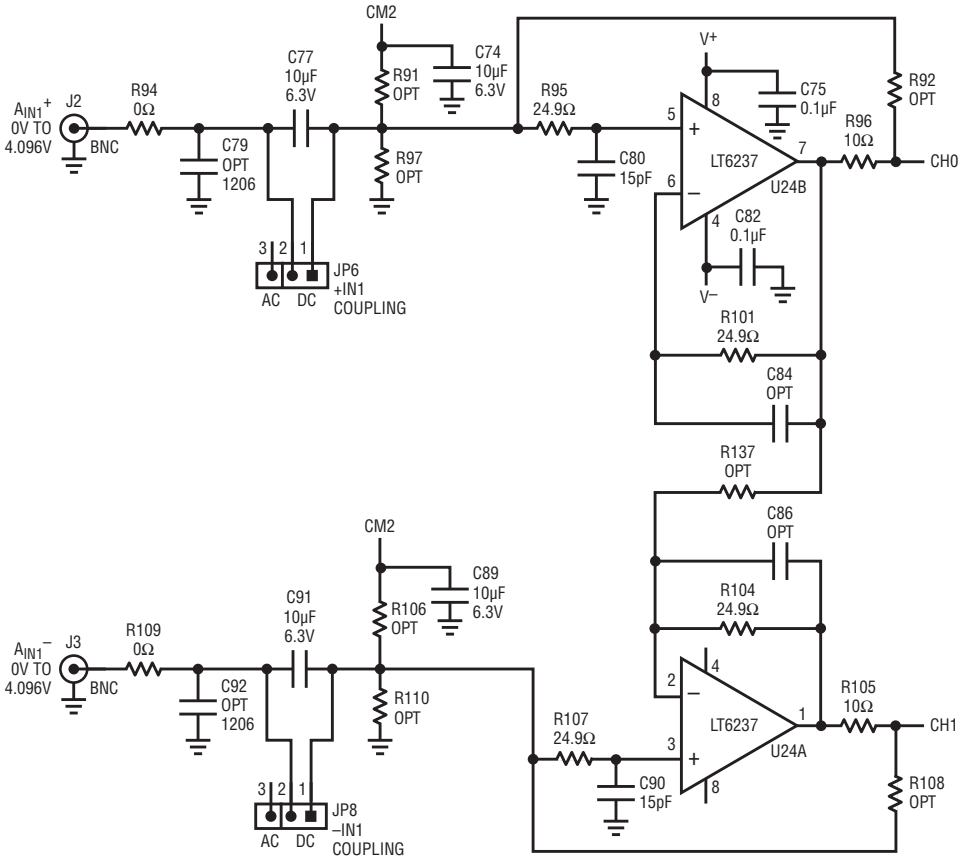

Figure 2. 0V to 4.096V Fully Differential AC/DC Coupled Driver

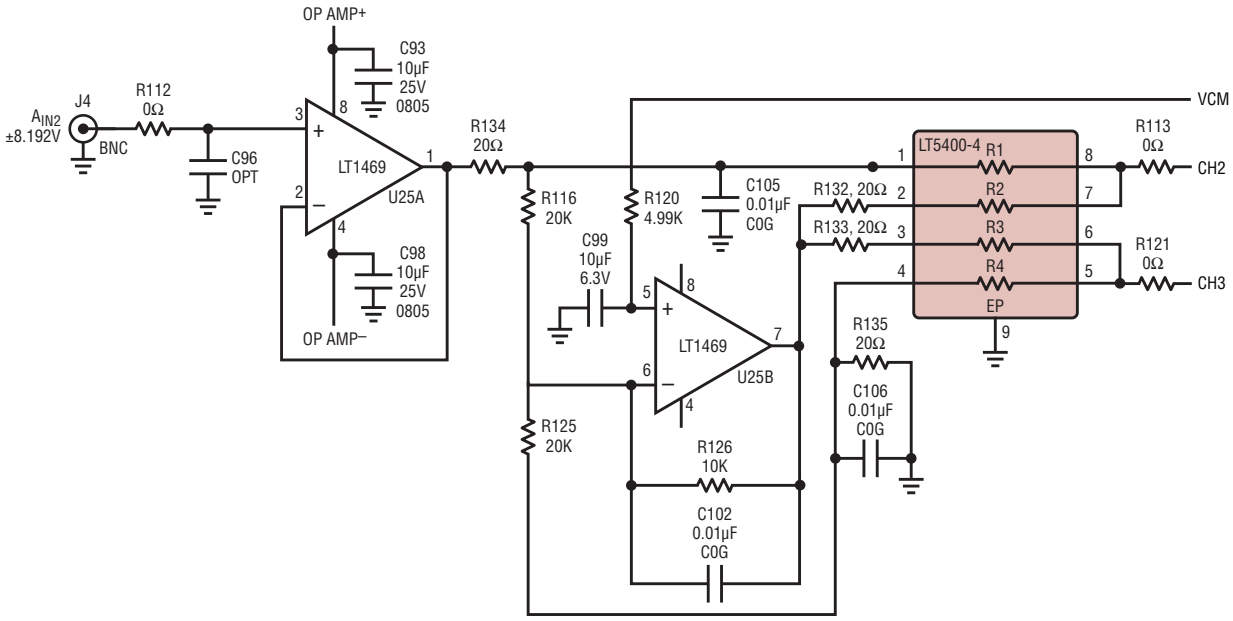

Figure 3. ±8.192V Single-Ended to Differential DC Coupled Driver

DC2071A SETUP

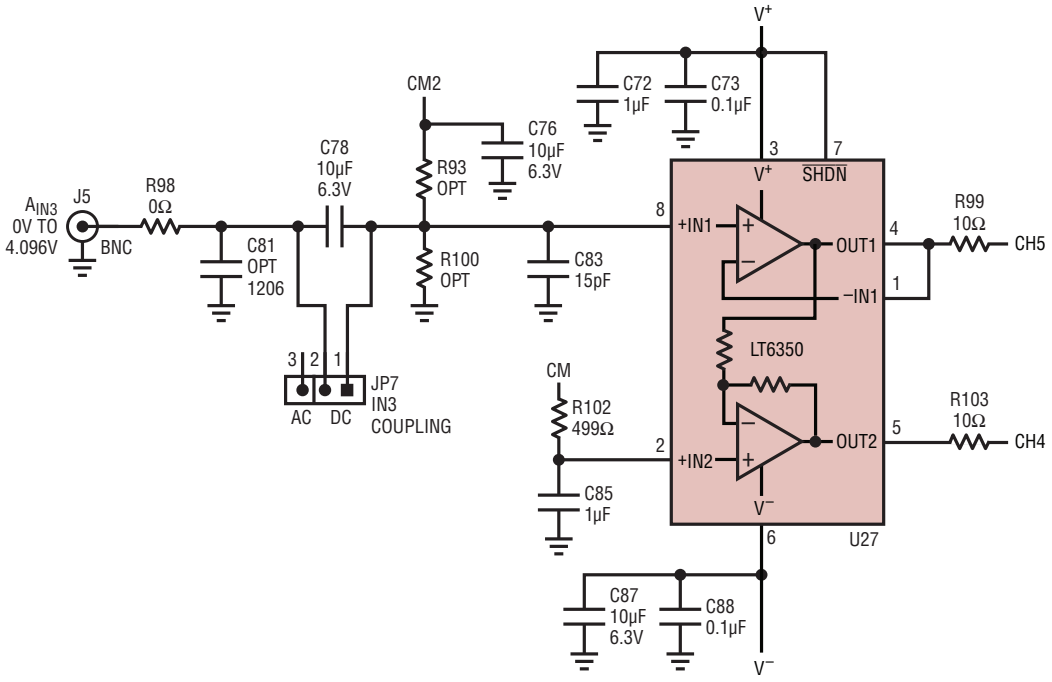

Figure 4. 0V to 4.096V Single-Ended to Differential AC/DC Coupled Driver

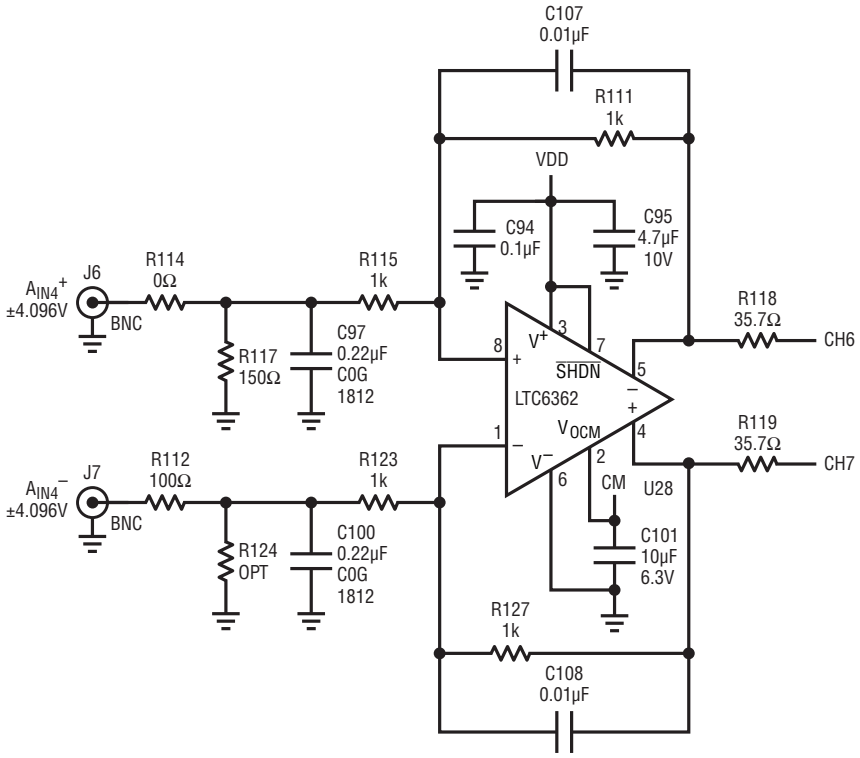

Figure 5. Single-Ended/Fully Differential Input to Fully Differential DC Coupled Driver

DC2071A SETUP

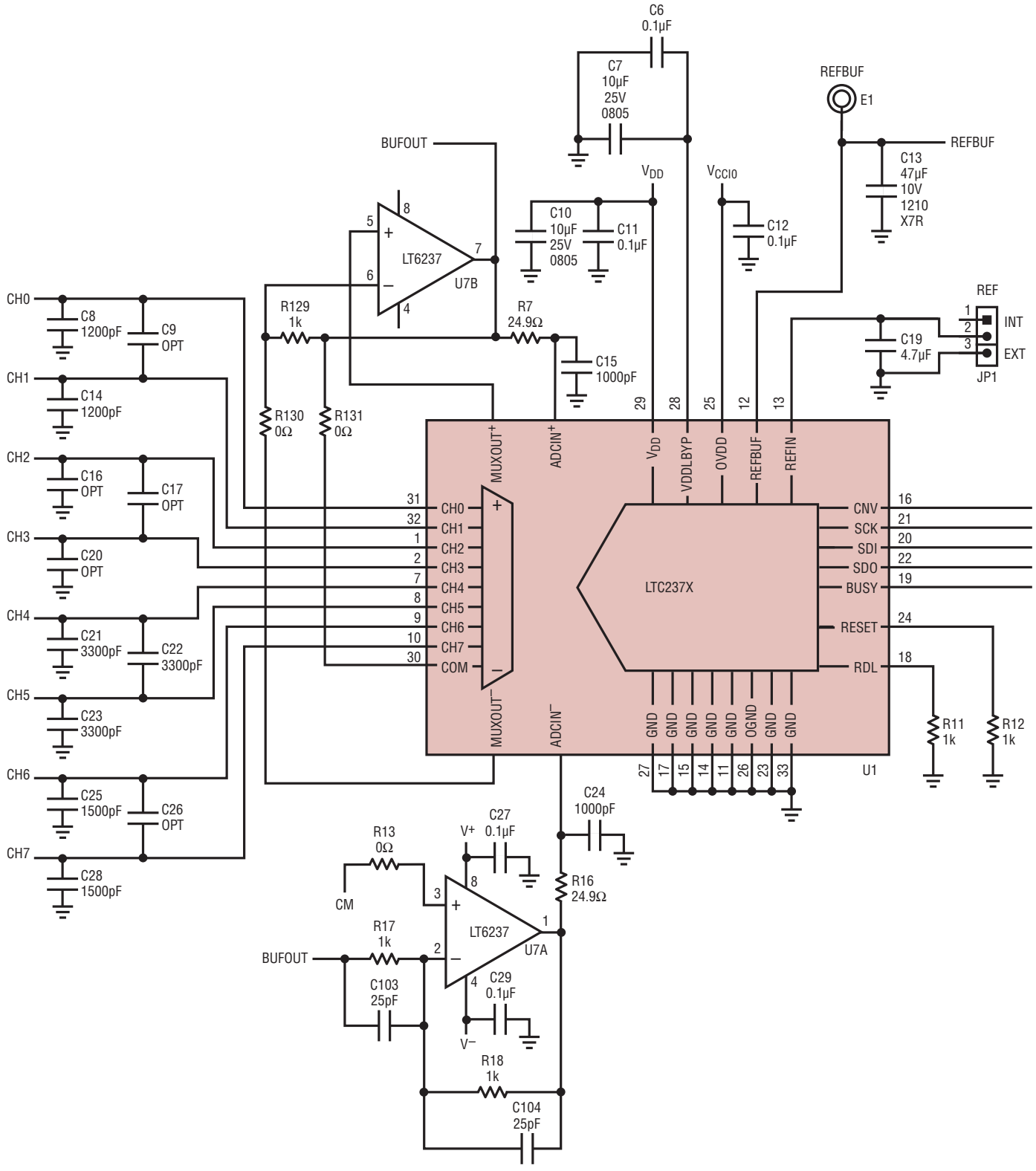

Figure 6. Eight Single-Ended Inputs Converted to Fully Differential

DC2071A SETUP

DC890 Data Collection

For SINAD, THD or SNR testing, a low noise, low distortion generator such as the B&K Type 1051 or Stanford Research SR1 should be used. A low jitter RF oscillator such as the Rohde & Schwarz SMB100A or DC1216A-A high speed clock source is used to drive the clock input. This demo board is tested in-house by attempting to duplicate the FFT plot shown in the Typical Performance Characteristics section of the LTC2373-18 data sheet. This involves using a 62MHz clock source, along with a sinusoidal generator at a frequency of approximately 1kHz. The input signal level is approximately –1dBFS. A typical FFT obtained with DC2071A is shown in Figure 7. Note that to calculate the real SNR, the signal level (F1 amplitude = –1.001dB) has to be added back to the SNR that PScope displays. With the example shown in Figure 7 this means that the actual SNR would be 100.60dB instead of the 99.60dB that PScope displays. Taking the RMS sum of the recalculated SNR and the THD yields a SINAD of 100.4dB which is fairly close to the typical number for this ADC.

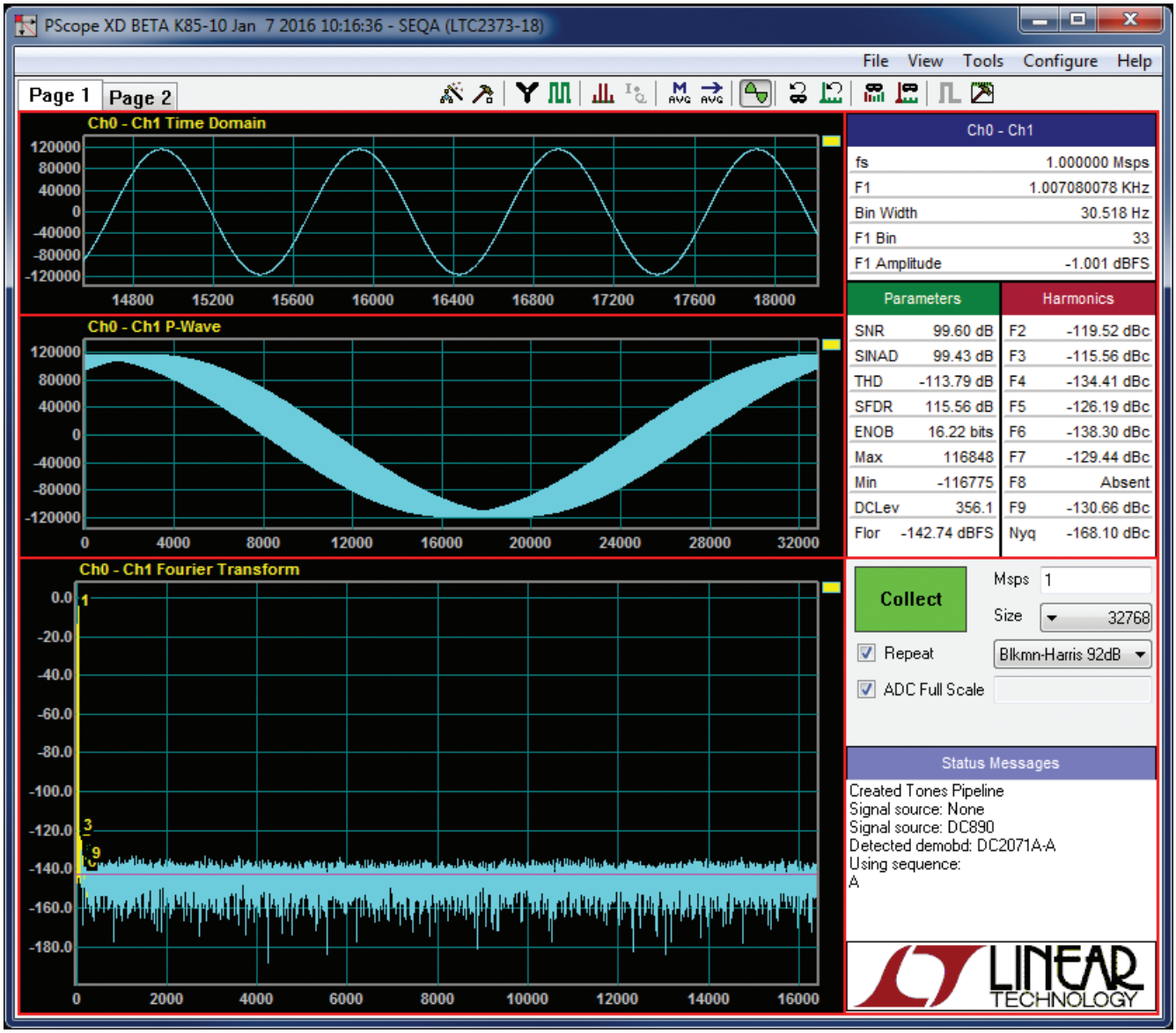

Figure 7. PScope Screen Shot

DC2071A SETUP

To change the default settings for the LTC2373-18 sequencer in PScope, click on the Set Demo Bd Options button in the PScope tool bar shown in Figure 8. This will open the Configure Sequencer menu of Figure 9. In this menu it is possible to set the number of sequences up to 16, the channel configuration, format and gain compression setting for each sequence. There is also a button to return PScope to the default DC2071 settings which are optimized for the default hardware settings of the DC2071A.

There are a number of scenarios that can produce misleading results when evaluating an ADC. One that is common is feeding the converter with an input frequency that is a sub-multiple of the sample rate and which will only exercise a small subset of the possible output codes. The proper method is to pick an M/N frequency for the input sine wave frequency. N is the number of samples in the FFT. M is a prime number between one and N/2. Multiply M/N by the sample rate to obtain the input sine wave frequency. Another scenario that can yield poor results is if you do not have a signal generator capable of ppm frequency accuracy or if it cannot be locked to the clock frequency. You can use an FFT with windowing to reduce the leakage, or spreading of the fundamental, to get a close approximation of the ADC performance. If an amplifier or clock source with poor phase noise is used, the windowing will not improve the SNR.

Figure 8. PScope Tool Bar

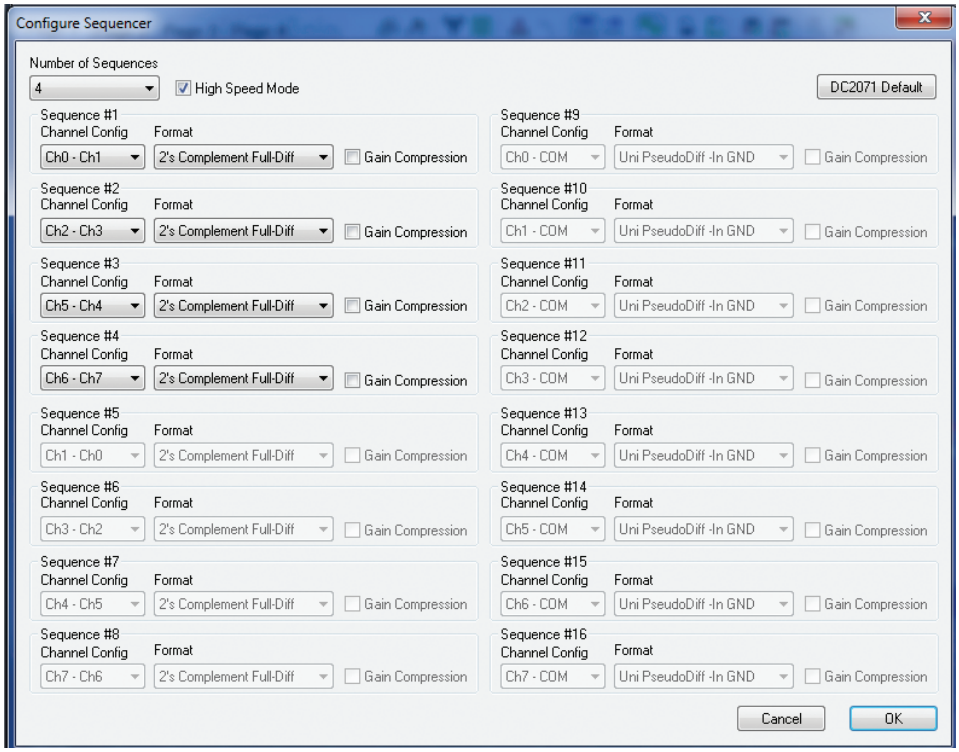

Figure 9. PScope Configure Sequencer Menu

DC2071A SETUP

DC590 Data Collection

Due to the relatively low and somewhat unpredictable sample rate of the DC590, its usefulness is limited to noise measurement and data collection of slowly moving signals. A typical data capture and histogram are shown in Figure 10. To change the default settings for the LTC2373-18 sequencer in QuikEval click on the Sequence Config. button. This will open the Sequence Configuration menu of Figure 11. In this menu, it is possible to set the number of sequences up to 16, the channel configuration, format and gain compression setting for each sequence. There is also a button to return QuikEval to the default DC2071 settings which are optimized for the default hardware settings of the DC2071A.

To get the best noise performance from the DC2071 it is recommended to place the demo board in a grounded metal enclosure filled with tissue paper.

Layout

As with any high performance ADC, this part is sensitive to layout. The area immediately surrounding the ADC on the DC2071A should be used as a guideline for placement and routing of the various components associated with the ADC. Here are some things to remember when laying out a board for the LTC2373-18. A ground plane is necessary to obtain maximum performance. Keep bypass capacitors as close to supply pins as possible. Use individual low impedance returns for all bypass capacitors. Use of a symmetrical layout around the analog inputs will minimize the effects of parasitic elements. Shield analog input traces with ground to minimize coupling from other traces. Keep traces as short as possible.

Component Selection

When driving a low noise, low distortion ADC such as the LTC2373-18, component selection is important so as to not degrade performance. Resistors should have low values to minimize noise and distortion. Metal film resistors are recommended to reduce distortion caused by self heating. Because of their low voltage coefficients, to further reduce distortion, NP0 or silver mica capacitors should be used. Any buffer used to drive the LTC2373-18 should have low distortion, low noise and a fast settling time, such as the LT1469, LT6237, LT6350 or LTC6362.

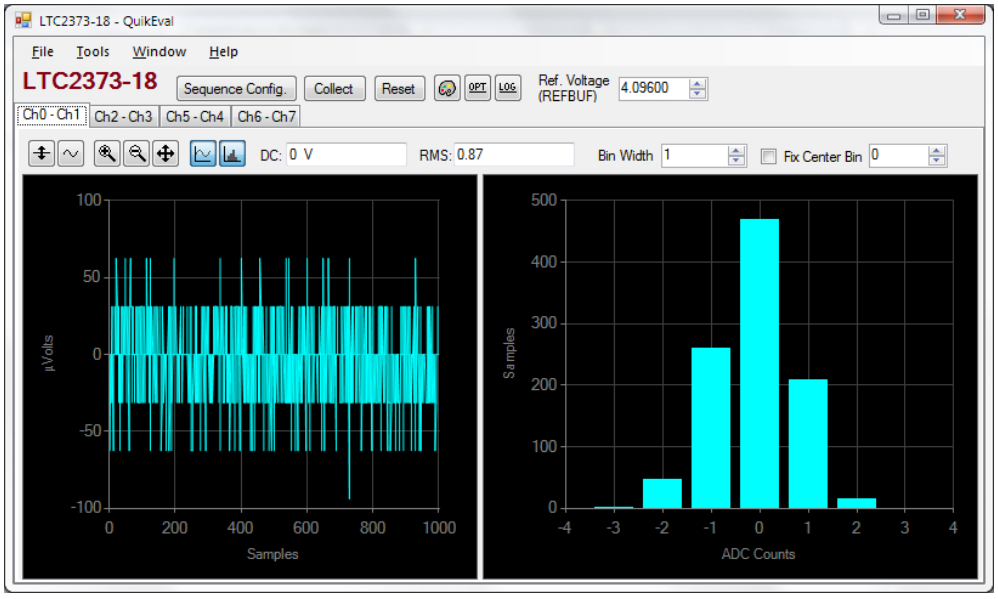

Figure 10. QuikEval Screen Shot

DC2071A SETUP

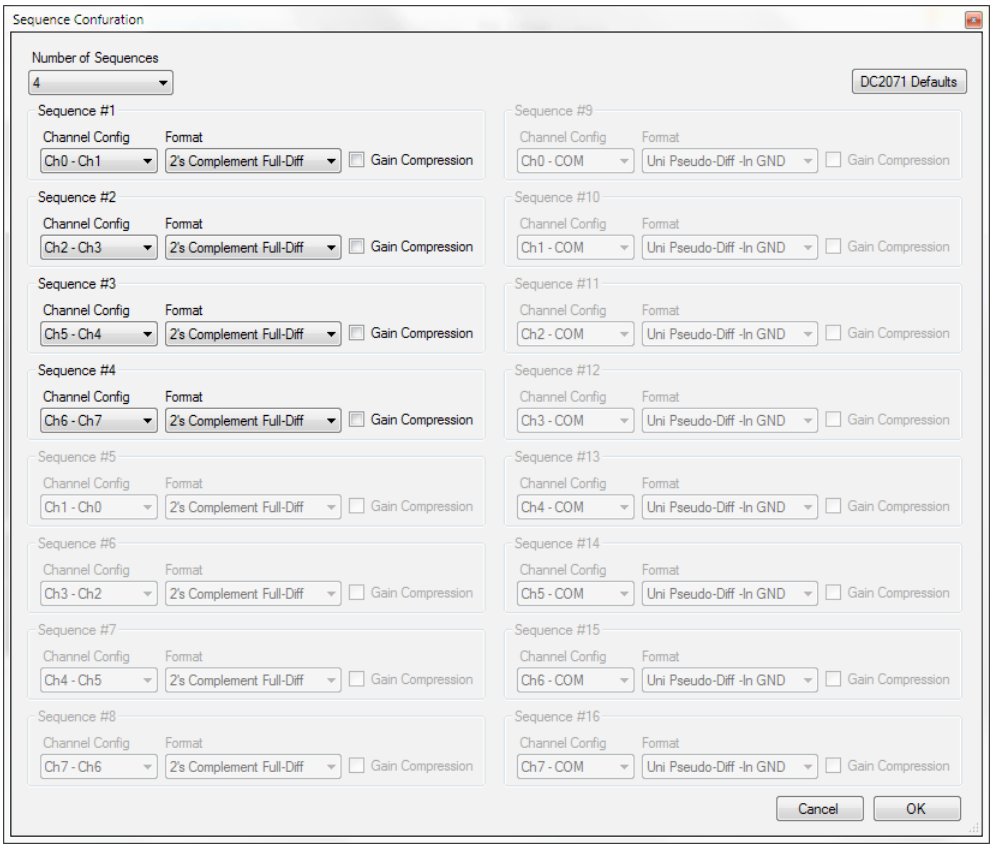

Figure 11. QuikEval Sequence Configuration Menu

DC2071A JUMPERS

Definitions

JP1: REF Selects INT or EXT reference for the ADC. The default setting is INT.

JP2: Selects the common mode voltage for the ADC. Choices are EXT, 2.5V, 2.048V or GND. The default setting is 2.048V.

JP3: VCCIO sets the output levels at J2 to either 3.3V or 2.5V. Use 2.5V to interface to the DC890 which is the default setting. Use 3.3V to interface to the DC590.

JP4: JTAG is used to program the CPLD. This is for factory use only.

JP5: EEPROM is for factory use only. The default position is WP.

JP6: +IN1 COUPLING selects AC or DC coupling of +IN1. The default setting is DC.

JP7: IN3 COUPLING selects AC or DC coupling of IN3. The default setting is DC.

JP8: –IN1 COUPLING Selects AC or DC coupling of –IN1. The default setting is DC.

JP9: COM sets the DC bias voltage for the COM pin to either CM or GND. CM is the default setting.

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