Low Power Triple and Quad Channels Digital Isolators

Check for Samples: ISO7631FM, ISO7631FC, ISO7640FC, ISO7641FC

FEATURES

- Signaling Rate: 150 Mbps (M-Grade), 25 Mbps (C-Grade)
- Robust Design with Integrated Noise Filter (C-Grade)
- Low Power Consumption, Typical I_{CC} per Channel (3.3V Supplies):
  - ISO7631FM: 2 mA at 10 Mbps
  - ISO7631FC: 1.5 mA at 10 Mbps
  - ISO7640FC: 1.1 mA at 10 Mbps
  - ISO7641FC: 1.3 mA at 10 Mbps
- Extremely low $I_{CC_disable}$(C-Grade)
- Low Propagation Delay: 7 ns Typical (M-Grade)
- Output Defaults to Low-state in Fail-safe Mode
- Wide Temperature Range: –40°C to 125°C
- 50 KV/µs Transient Immunity, Typical
- Long Life with SiO_2 Isolation barrier
- Operates From 2.7V (M-Grade), 3.3 V and 5 V Supply and Logic Levels
- Wide Body SOIC-16 Package

APPLICATIONS

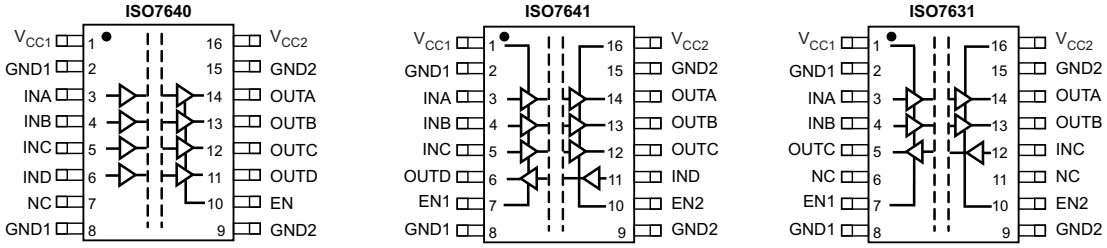
- Optocoupler Replacement in:
  - Industrial Fieldbus
    - Profibus
    - Modbus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

SAFETY AND REGULATORY APPROVALS

- 2500 V_{RMS} for 1 Minute per UL 1577 (approved)
- 4000 V_{PK} VDE Rating for DIN EN 60747-5-2 (VDE 0884 Rev. 2), 1414 V_{PK} Working Voltage (approved)
- CSA Component Acceptance Notice 5A(approved)

DESCRIPTION

ISO7631F, ISO7640F and ISO7641F provide galvanic isolation up to 4 KV_{PK} per VDE. ISO7631F has 3 channels with two forward and one reverse direction channels. ISO7640F and ISO7641F are quad channel isolators; ISO7640F has four forward and ISO7641F has three forward and one reverse direction channels. Suffix F indicates that output defaults to Low-state in fail-safe conditions (see Table 1). M-Grade devices are high speed isolators capable of 150 Mbps data rate with fast propagation delays whereas C-Grade devices can run up to 25 Mbps data rate with low power consumption and integrated filters for noise-prone applications. C-Grade devices are recommended for lower speed applications where input noise pulses of less than 6 ns duration need to be suppressed or lower power consumption is critical.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2012, Texas Instruments Incorporated

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The devices have TTL input thresholds and can operate from 2.7 V (M-Grade), 3.3 V and 5 V supplies. All inputs are 5 V tolerant when supplied from 3.3 V or 2.7 V supplies.

PIN DESCRIPTIONS

PIN				I/O	DESCRIPTION
NAME	ISO7640	ISO7641	ISO7631		
INA	3	3	3	I	Input, channel A
INB	4	4	4	I	Input, channel B
INC	5	5	12	I	Input, channel C
IND	6	11	-	I	Input, channel D
OUTA	14	14	14	O	Output, channel A
OUTB	13	13	13	O	Output, channel B
OUTC	12	12	5	O	Output, channel C
OUTD	11	6	-	O	Output, channel D
EN	10	-	-	I	Enables (when input is High or Open) or Disables (when input is Low) OUTA, OUTB, OUTC and OUTD of ISO7640
EN1	-	7	7	I	Enables (when input is High or Open) or Disables (when input is Low) OUTD of ISO7641 and OUTC of ISO7631
EN2	-	10	10	I	Enables (when input is High or Open) or Disables (when input is Low) OUTA, OUTB, and OUTC of ISO7641 Enables (when input is High or Open) or Disables (when input is Low) OUTA and OUTB of ISO7631
V_{CC1}	1	1	1	–	Power supply, V_{CC1}
V_{CC2}	16	16	16	–	Power supply, V_{CC2}
GND1	2,8	2,8	2,8	–	Ground connection for V_{CC1}
GND2	9,15	9,15	9,15	–	Ground connection for V_{CC2}
NC	7	-	6,11	-	No Connect pins are floating with no internal connection

Table 1. FUNCTION TABLE(1)

INPUT V_{CC}	OUTPUT V_{CC}	INPUT (INx)	OUTPUT ENABLE (ENx)	OUTPUT (OUTx)
PU	PU	H	H or Open	H
		L	H or Open	L
		X	L	Z
		Open	H or Open	L
PD	PU	X	H or Open	L
PD	PU	X	L	Z
PU	PD	X	X	Undetermined

(1) PU = Powered Up(V_{CC} ≥ 2.7 V); PD = Powered Down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High Level; L = Low Level; Z = High Impedance

Copyright © 2012, Texas Instruments Incorporated

AVAILABLE OPTIONS

PRODUCT	RATED ISOLATION	PACKAGE	INPUT THRESHOLD	DATA RATE and FILTER	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO7631FM	4 KV_{PK} / 2.5 KV_{RMS} (2)	DW-16	1.5 V TTL (CMOS Compatible)	150 Mbps, No Noise Filter	2 Forward, 1 Reverse	ISO7631FM	ISO7631FMDW (rail)
							ISO7631FMDWR (reel)
ISO7631FC				25 Mbps, Integrated Noise Filter	2 Forward, 1 Reverse	ISO7631FC	ISO7631FCDW (rail)
							ISO7631FCDWR (reel)
ISO7640FC (1)					4 Forward, 0 Reverse	ISO7640FC	ISO7640FCDW (rail)
							ISO7640FCDWR (reel)
ISO7641FC					3 Forward, 1 Reverse	ISO7641FC	ISO7641FCDW (rail)
							ISO7641FCDWR (reel)

(1) Product Preview
(2) See the Regulatory Information table for detailed isolation ratings.

Copyright © 2012, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS(1)

PARAMETER				VALUE		UNIT
				MIN	MAX	
Supply voltage(2)	V_{CC1}, V_{CC2}			–0.5	6	V
Voltage	INx, OUTx, ENx			–0.5	6	V
Output Current, I_O					±15	mA
Electrostatic discharge	Human Body Model	ESDA, JEDEC JS-001-2012	All pins		±4	kV
	Field-Induced Charged Device Model	JEDEC JESD22-C101E			±1.5	kV
	Machine Model	JEDEC JESD22-A115-A			±200	V
Maximum junction temperature, T_J					150	°C
Storage temperature, T_{STG}				-65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

PARAMETER			MIN	TYP	MAX	UNIT
Supply voltage	V_{CC1}, V_{CC2}	M-Grade	2.7		5.5	V
		C-Grade	3		5.5	
High-level output current	I_{OH}		-4			mA
Low-level output current	I_{OL}				4	mA
High-level input voltage	V_{IH}		2		V_{CC}	V
Low-level input voltage	V_{IL}		0		0.8	V
Input pulse duration	t_{ui}	M-Grade: ≥3V-Operation	6.67			ns
		M-Grade: <3V-Operation	10			
		C-Grade: ≥3V-Operation	40			
Signaling rate	1 / t_{ui}	M-Grade: ≥3V-Operation	0		150	Mbps
		M-Grade: <3V-Operation	0		100	
		C-Grade: ≥3V-Operation	0		25	
Junction temperature	T_J		-40		136	°C
Ambient temperature	T_A		-40	25	125	°C

THERMAL INFORMATION

THERMAL METRIC(1)			ISO76xx	UNITS
			DW (16 Pins)	
θ_{JA}	Junction-to-ambient thermal resistance		72	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance		38	
θ_{JB}	Junction-to-board thermal resistance		39	
ψ_{JT}	Junction-to-top characterization parameter		9.4	
ψ_{JB}	Junction-to-board characterization parameter		n/a	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance		n/a	
P_D	Maximum Device Power Dissipation	V_{CC1} = V_{CC2} = 5.5V, T_J = 150°C, C_L = 15pF Input a 75 MHz 50% duty cycle square wave	399	mW

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Copyright © 2012, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7640F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	V_{CCx} (1) – 0.8	4.8		V_{CCx} (1) – 0.8	4.7		V
		I_{OH} = –20 µA; see Figure 1	V_{CCx} (1) – 0.1	5		V_{CCx} (1) – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1		0.2	0.4		0.3	0.5	V
		I_{OL} = 20 µA; see Figure 1		0	0.1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			450			450		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4	25	75		25	75		kV/µs

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7640F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	3.5	7	10.5	11	17	28	ns
PWD (1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2			3	
$t_{sk(o)}$ (2)	Channel-to-channel output skew time	Same-direction Channels			2			3	
		Opposite-direction Channels			3			4	
$t_{sk(pp)}$ (3)	Part-to-part skew time				4.5			13	
t_r	Output signal rise time	See Figure 1		1.6			2.8		ns
t_f	Output signal fall time			1			2.9		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		5	16		8	20	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			5	16		7	20	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			4	16		11000	22000 (4)	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			4	16		8	20	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5			9		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

Copyright © 2012, Texas Instruments Incorporated

SUPPLY CURRENT

V_{CC1} and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			C-Grade			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.5	4		1.1	1.9	mA
I_{CC2}				3.7	5.4		1.5	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.6	4.1		1.8	2.7	
I_{CC2}				3.8	5.5		2.6	3.9	
I_{CC1}	10 Mbps			3.3	4.5		2.7	3.7	
I_{CC2}				4.9	6.6		3.9	5.3	
I_{CC1}	25 Mbps			4.5	6		4.1	5.4	
I_{CC2}				6.8	9		5.9	7.8	
I_{CC1}	150 Mbps			15	19.5	Not Applicable			
I_{CC2}				22	30				
ISO7640F						**C-Grade**			
I_{CC1}	Disable	EN = 0 V					0.6	1.2	mA
I_{CC2}							1.3	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					0.7	1.3	
I_{CC2}							3	4.6	
I_{CC1}	10 Mbps						1.3	2	
I_{CC2}							5.2	7	
I_{CC1}	25 Mbps						2.5	3.6	
I_{CC2}							8.5	11	
ISO7641F						**C-Grade**			
I_{CC1}	Disable	EN1 = EN2 = 0 V					1.2	2.1	mA
I_{CC2}							1.6	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					1.8	2.8	
I_{CC2}							3.1	4.2	
I_{CC1}	10 Mbps						3	4	
I_{CC2}							4.9	6.1	
I_{CC1}	25 Mbps						4.8	6	
I_{CC2}							7.7	9.5	

Copyright © 2012, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

V_{CC1} at 5 V ± 10% and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7640F, ISO7641F				M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.8	4.8		V_{CC1} – 0.8	4.7		V
			OUTx on V_{CC2} (3.3V) side	V_{CC2} - 0.4	3		V_{CC2} - 0.6	2.9		
		I_{OH} = –20 µA; see Figure 1	OUTx on V_{CC1} (5V) side	V_{CC1} – 0.1	5		V_{CC1} – 0.1	5		
			OUTx on V_{CC2} (3.3V) side	V_{CC2} – 0.1	3.3		V_{CC2} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1			0.2	0.4		0.3	0.5	V
		I_{OL} = 20 µA; see Figure 1			0	0.1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430			430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4		25	50		25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} at 5 V ± 10% and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7640F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	4	8	13	11	18	32	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2			3.5	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2.5			4.5	
		Opposite-direction Channels			3.5			5.5	
$t_{sk(pp)}$(3)	Part-to-part skew time				6			15	
t_r	Output signal rise time	See Figure 1		2			3.6		ns
t_f	Output signal fall time			1.2			3.3		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		6.5	17		9	20	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			6.5	17		8	20	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			5.5	17		11000	22000(4)	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			5.5	17		10	30	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5			8.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

Copyright © 2012, Texas Instruments Incorporated

SUPPLY CURRENT

V_{CC1} at 5 V ± 10% and V_{CC2} at 3.3V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			C-Grade			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		2.5	4		1.1	1.9	mA
I_{CC2}				2.7	3.7		0.7	1.3	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		2.6	4.1		1.8	2.7	
I_{CC2}				2.8	3.8		1.8	2.6	
I_{CC1}	10 Mbps			3.3	4.5		2.7	3.7	
I_{CC2}				3.5	4.6		2.6	3.5	
I_{CC1}	25 Mbps			4.5	6		4.1	5.4	
I_{CC2}				4.7	5.9		3.8	5	
I_{CC1}	150 Mbps			15	19.5	Not Applicable			
I_{CC2}				14.6	19				
ISO7640F						**C-Grade**			
I_{CC1}	Disable	EN = 0 V					0.6	1.2	mA
I_{CC2}							0.6	1.1	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					0.7	1.3	
I_{CC2}							2.1	3.2	
I_{CC1}	10 Mbps						1.3	2	
I_{CC2}							3.6	4.7	
I_{CC1}	25 Mbps						2.5	3.6	
I_{CC2}							5.7	9	
ISO7641F						**C-Grade**			
I_{CC1}	Disable	EN1 = EN2 = 0 V					1.2	2.1	mA
I_{CC2}							0.8	1.3	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					1.8	2.8	
I_{CC2}							2	2.9	
I_{CC1}	10 Mbps						3	4	
I_{CC2}							3.2	4.1	
I_{CC1}	25 Mbps						4.8	6	
I_{CC2}							5.1	7	

Copyright © 2012, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

V_{CC1} at 3.3V ± 10% and V_{CC2} at 5V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7640F, ISO7641F				M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.4	3		V_{CC1}-0.6	2.9		V
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.8	4.8		V_{CC2}–0.8	4.7		
		I_{OH} = –20 µA; see Figure 1	OUTx on V_{CC1} (3.3 V) side	V_{CC1}–0.1	3.3		V_{CC1}–0.1	3.3		
			OUTx on V_{CC2} (5 V) side	V_{CC2}–0.1	5		V_{CC2}–0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1			0.2	0.4		0.3	0.5	V
		I_{OL} = 20 µA; see Figure 1			0	0.1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				430			430		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx				10			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx		-10			-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4		25	50		25	50		kV/µs

SWITCHING CHARACTERISTICS

V_{CC1} at 3.3 V ± 10% and V_{CC2} at 5 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7640F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	4	7.5	12.5	11	18.5	32	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2			2.5	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			2.5			4.5	
		Opposite-direction Channels			3.5			5.5	
$t_{sk(pp)}$(3)	Part-to-part skew time				6			15	
t_r	Output signal rise time	See Figure 1		1.7			2.9		ns
t_f	Output signal fall time			1.1			2.9		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		5.5	17		8	20	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			5.5	17		7	20	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			4.5	17		11000	22000(4)	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			4.5	17		8	30	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.5			7.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

Copyright © 2012, Texas Instruments Incorporated

SUPPLY CURRENT

V_{CC1} at 3.3V ± 10% and V_{CC2} at 5V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			C-Grade			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.8	2.8		0.6	1.1	mA
I_{CC2}				3.7	5.4		1.5	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.9	2.9		1.2	1.8	
I_{CC2}				3.8	5.5		2.6	3.9	
I_{CC1}	10 Mbps			2.4	3.4		1.8	2.6	
I_{CC2}				4.9	6.6		3.9	5.3	
I_{CC1}	25 Mbps			3.2	4.2		2.7	3.6	
I_{CC2}				6.8	9		5.9	7.8	
I_{CC1}	150 Mbps			9.3	12.5	Not Applicable			
I_{CC2}				22	30				
ISO7640F						**C-Grade**			
I_{CC1}	Disable	EN = 0 V					0.35	0.7	mA
I_{CC2}							1.3	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					0.4	0.8	
I_{CC2}							3	4.6	
I_{CC1}	10 Mbps						0.7	1.2	
I_{CC2}							5.2	7	
I_{CC1}	25 Mbps						1.5	2.2	
I_{CC2}							8.5	11	
ISO7641F						**C-Grade**			
I_{CC1}	Disable	EN1 = EN2 = 0 V					0.7	1.1	mA
I_{CC2}							1.6	2.6	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					1.2	1.9	
I_{CC2}							3.1	4.2	
I_{CC1}	10 Mbps						2	2.8	
I_{CC2}							4.9	6.1	
I_{CC1}	25 Mbps						3.1	4	
I_{CC2}							7.7	9.5	

Copyright © 2012, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7640F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	V_{CCx}(1) – 0.4	3		V_{CCx}(1) – 0.6	2.9		V
		I_{OH} = –20 µA; see Figure 1	V_{CCx}(1) – 0.1	3.3		V_{CCx}(1) – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1		0.2	0.4		0.3	0.5	V
		I_{OL} = 20 µA; see Figure 1		0	0.1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			425			425		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4	25	50		25	50		kV/µs

(1) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F, ISO7640F, ISO7641F			M-Grade			C-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	4	8.5	14	12	23	35	ns
PWD(1)	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2			3	
$t_{sk(o)}$(2)	Channel-to-channel output skew time	Same-direction Channels			3			5	
		Opposite-direction Channels			4			6	
$t_{sk(pp)}$(3)	Part-to-part skew time				6.5			16	
t_r	Output signal rise time	See Figure 1		2			3.7		ns
t_f	Output signal fall time			1.3			3.4		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		6.5	17		9	20	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			6.5	17		8	20	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			5.5	17		11000	22000(4)	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			5.5	17		10	30	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		9.2			7.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.
(4) The enable signal rate for C-grade devices should be ≤ 45 Kbps.

Copyright © 2012, Texas Instruments Incorporated

SUPPLY CURRENT

V_{CC1} and V_{CC2} at 3.3 V ± 10% (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			C-Grade			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.8	2.8		0.6	1.1	mA
I_{CC2}				2.7	3.7		0.7	1.3	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.9	2.9		1.2	1.8	
I_{CC2}				2.8	3.8		1.8	2.6	
I_{CC1}	10 Mbps			2.4	3.4		1.8	2.6	
I_{CC2}				3.5	4.6		2.6	3.5	
I_{CC1}	25 Mbps			3.2	4.2		2.7	3.6	
I_{CC2}				4.7	5.9		3.8	5	
I_{CC1}	150 Mbps			9.3	12.5	Not Applicable			
I_{CC2}				14.6	19				
ISO7640F						**C-Grade**			
I_{CC1}	Disable	EN = 0 V					0.35	0.7	mA
I_{CC2}							0.6	1.1	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					0.4	0.8	
I_{CC2}							2.1	3.2	
I_{CC1}	10 Mbps						0.7	1.2	
I_{CC2}							3.6	4.7	
I_{CC1}	25 Mbps						1.5	2.2	
I_{CC2}							5.7	9	
ISO7641F						**C-Grade**			
I_{CC1}	Disable	EN1 = EN2 = 0 V					0.7	1.1	mA
I_{CC2}							0.8	1.3	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V, AC Signal: All channels switching with square wave clock input; C_L = 15 pF					1.2	1.9	
I_{CC2}							2	2.9	
I_{CC1}	10 Mbps						2	2.8	
I_{CC2}							3.2	4.1	
I_{CC1}	25 Mbps						3.1	4	
I_{CC2}							5.1	7	

Copyright © 2012, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 2.7 V[1] (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1	V_{CC}[2] – 0.5	2.4		V
		I_{OH} = –20 µA; see Figure 1	V_{CC}[2] – 0.1	2.7		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1		0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1		0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis			350		mV
I_{IH}	High-level input current	V_{IH} = V_{CC} at INx or ENx			10	µA
I_{IL}	Low-level input current	V_{IL} = 0 V at INx or ENx	-10			
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 4	25	50		kV/µs

(1) Only M-Grade devices are recommended for operation down to 2.7 V supplies. For 2.7 V-operation, max data rate is 100 Mbps.
(2) V_{CCx} is the supply voltage, V_{CC1} or V_{CC2}, for the output channel that is being measured.

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1	5	8	16	ns
PWD[1]	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$				2.5	
$t_{sk(o)}$[2]	Channel-to-channel output skew time	Same-direction Channels			4	
		Opposite-direction Channels			5	
$t_{sk(pp)}$[3]	Part-to-part skew time				8	
t_r	Output signal rise time	See Figure 1		2.3		ns
t_f	Output signal fall time			1.8		
t_{PHZ}	Disable Propagation Delay, high-to-high impedance output	See Figure 2		8	18	ns
t_{PLZ}	Disable Propagation Delay, low-to-high impedance output			8	18	
t_{PZH}	Enable Propagation Delay, high impedance-to-high output			7	18	
t_{PZL}	Enable Propagation Delay, high impedance-to-low output			7	18	
t_{fs}	Fail-safe output delay time from input data or power loss	See Figure 3		8.5		µs

(1) Also known as Pulse Skew.
(2) $t_{sk(o)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

Copyright © 2012, Texas Instruments Incorporated

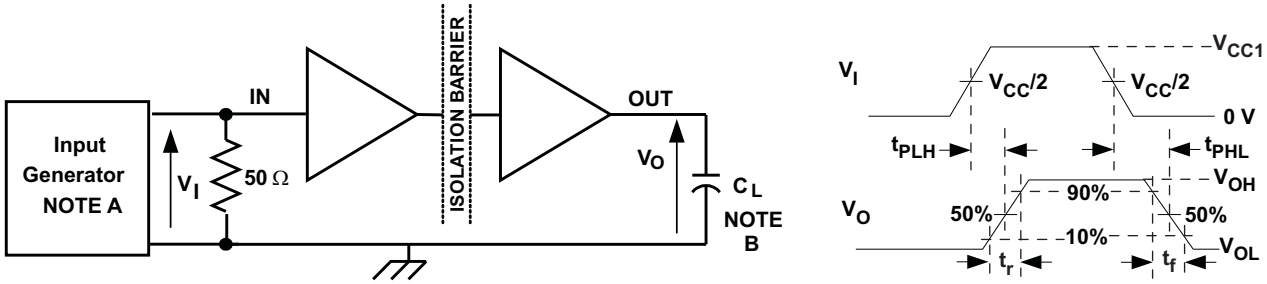
SUPPLY CURRENT

V_{CC1} and V_{CC2} at 2.7 V (over recommended operating conditions unless otherwise noted)

ISO7631F			M-Grade			
PARAMETER	**TEST CONDITIONS**		**MIN**	**TYP**	**MAX**	**UNIT**
I_{CC1}	Disable	EN1 = EN2 = 0 V		1.5	2.4	mA
I_{CC2}				2.2	3.2	
I_{CC1}	DC to 1 Mbps	DC Signal: $V_I = V_{CC}$ or 0 V AC Signal: All channels switching with square wave clock input; C_L = 15 pF		1.6	2.5	
I_{CC2}				2.3	3.2	
I_{CC1}	10 Mbps			2	2.9	
I_{CC2}				3	3.9	
I_{CC1}	25 Mbps			2.7	3.7	
I_{CC2}				3.9	4.9	
I_{CC1}	100 Mbps			5.7	6.8	
I_{CC2}				8.6	12	

Copyright © 2012, Texas Instruments Incorporated

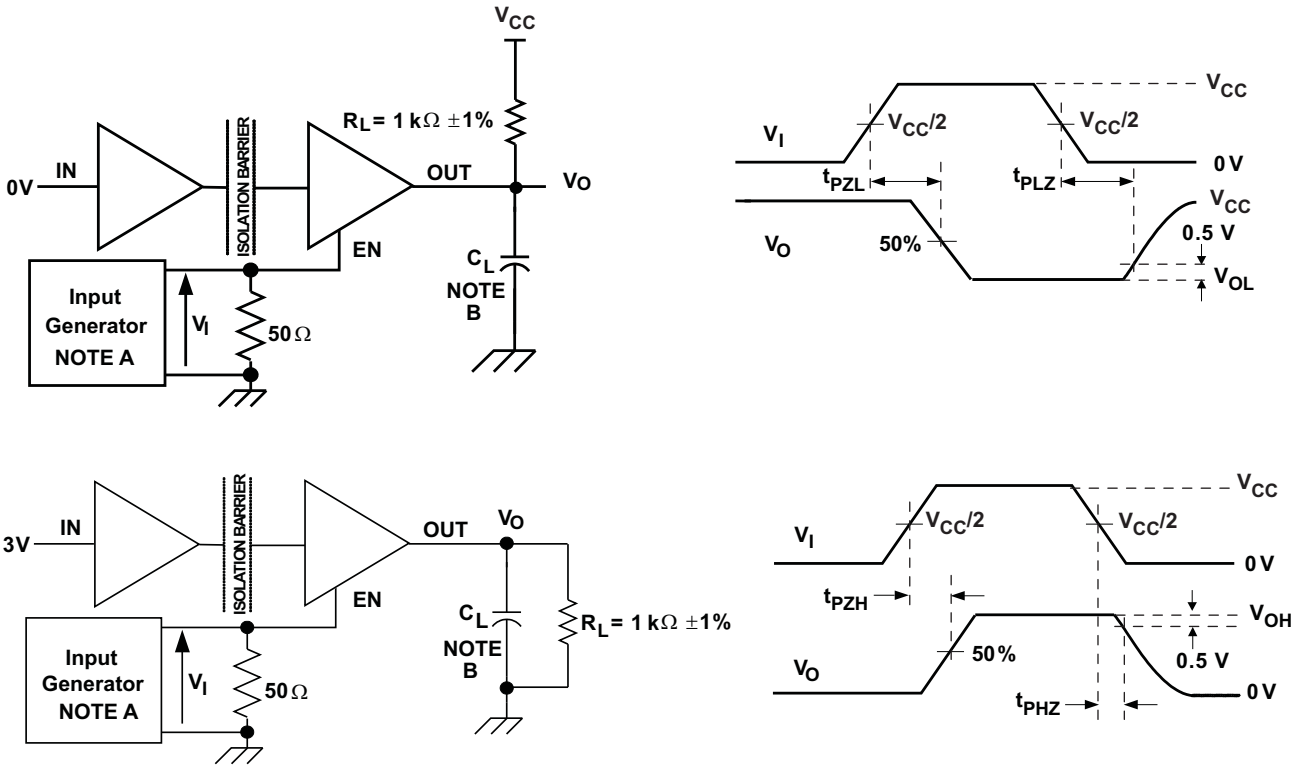
PARAMETER MEASUREMENT INFORMATION



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3ns, Z_O = 50 Ω. At the input, 50 Ω resistor is required to terminate Input Generator signal. It is not needed in actual application.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristics Test Circuit and Voltage Waveforms

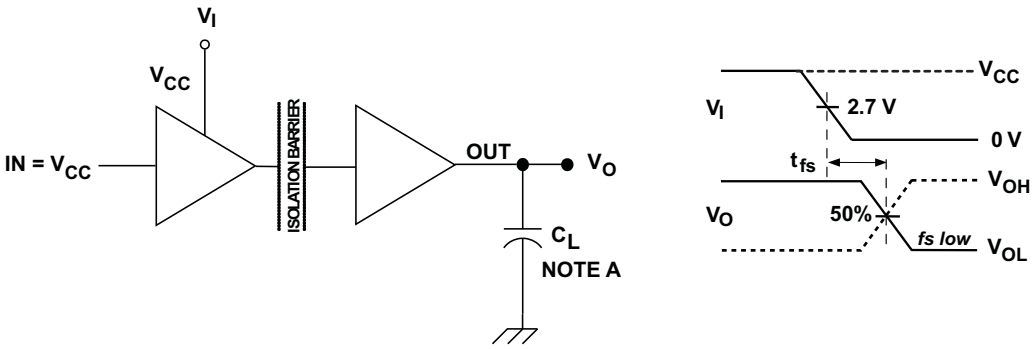


A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 10 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

B. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

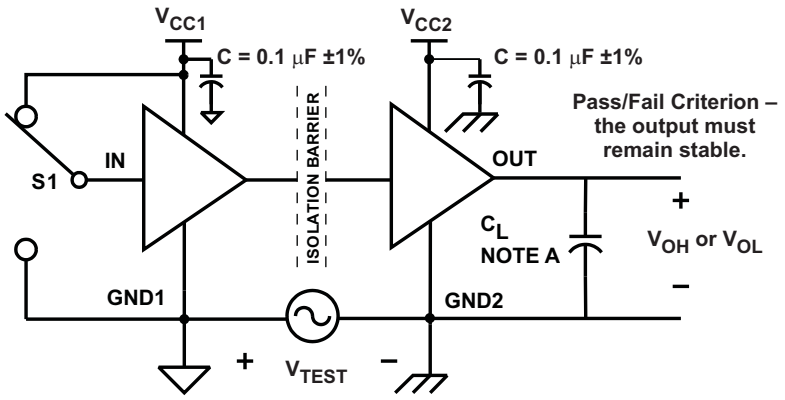
Figure 2. Enable/Disable Propagation Delay Time Test Circuit and Waveform

PARAMETER MEASUREMENT INFORMATION (continued)



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Failsafe Delay Time Test Circuit and Voltage Waveforms



A. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 4. Common-Mode Transient Immunity Test Circuit

Copyright © 2012, Texas Instruments Incorporated

DEVICE INFORMATION

IEC INSULATION AND SAFETY-RELATED SPECIFICATIONS FOR DW-16 PACKAGE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal to terminal distance through air	8.3			mm
L(I02) (1)	Minimum external tracking (Creepage)	Shortest terminal to terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
	Minimum Internal Gap (Internal Clearance)	Distance through the insulation	0.014			mm
R_{IO} (2)	Isolation resistance, Input to Output	V_{IO} = 500 V, T_A < 100°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		$>10^{11}$		
C_{IO} (2)	Barrier capacitance, Input to Output	V_I = 0.4 sin (2πft), f = 1MHz		2		pF
C_I (3)	Input capacitance	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1MHz, V_{CC} = 5 V		2		pF

(1) Per JEDEC package dimensions.
(2) All pins on each side of the barrier tied together creating a two-terminal device.
(3) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.

Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

Table 2. DIN EN 60747-5-2 (VDE 0884 TEIL 2) INSULATION CHARACTERISTICS (1) over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		1414	V_{PEAK}
V_{PR}	Input-to-output test voltage	After Input/Output safety test subgroup 2/3, $V_{PR} = V_{IORM}$ x 1.2, t = 10 s, Partial discharge < 5 pC	1697	V_{PEAK}
		Method a, After environmental tests subgroup 1, $V_{PR} = V_{IORM}$ x 1.6, t = 10 s, Partial Discharge < 5 pC	2262	
		Method b1, 100% Production test $V_{PR} = V_{IORM}$ x 1.875, t = 1 s Partial discharge < 5 pC	2652	
V_{IOTM}	Maximum transient overvoltage	$V_{TEST} = V_{IOTM}$ t = 60 sec (Qualification) t = 1 sec (100% Production)	4000	V_{PEAK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Copyright © 2012, Texas Instruments Incorporated

Table 3. IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation classification	Rated mains voltage ≤ 300 V_{RMS}	I–IV
	Rated mains voltage ≤ 600 V_{RMS}	I–III
	Rated mains voltage ≤ 1000 V_{RMS}	I–II

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to DIN EN 60747-5-2	Approved under CSA Component Acceptance Notice #5A	Recognized under 1577 Component Recognition Program
Basic Insulation Maximum Transient Overvoltage, 4000 V_{PK} Maximum Working Voltage, 1414 V_{PK}	4000 V_{PK} Insulation	Single Protection, 2500 V_{RMS} (1)
File Number: 40016131	File Number: 220991	File Number: E181974

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the IO can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	θ_{JA} = 72 °C/W, V_I = 5.5V, T_J = 150°C, T_A = 25°C			316	mA
			θ_{JA} = 72 °C/W, V_I = 3.6V, T_J = 150°C, T_A = 25°C			482	
			θ_{JA} = 72 °C/W, V_I = 2.7V, T_J = 150°C, T_A = 25°C			643	
T_S	Maximum case temperature					150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in the absolute maximum ratings table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a High-K Test Board for Leaded Surface Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

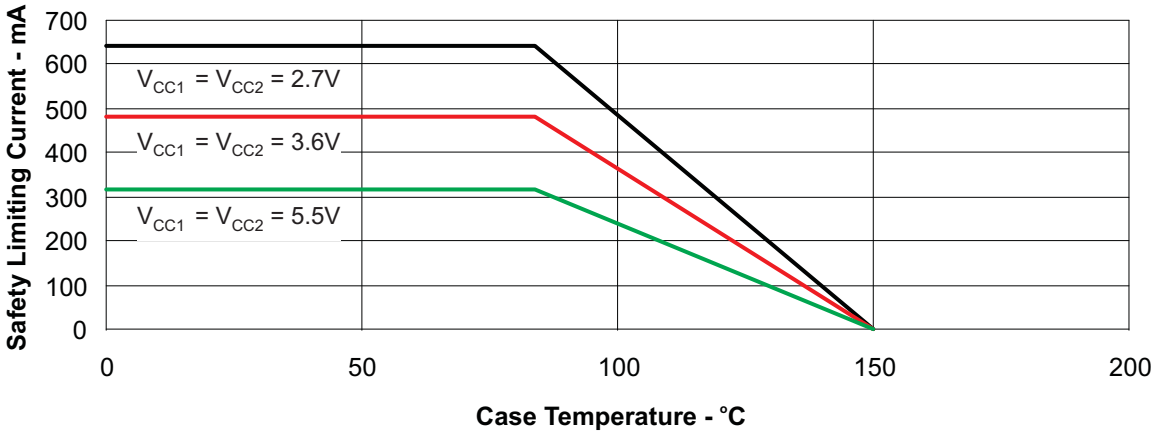


Figure 5. DW-16 θ_{JC} Thermal Derating Curve per IEC 60747-5-2

Copyright © 2012, Texas Instruments Incorporated

APPLICATION INFORMATION

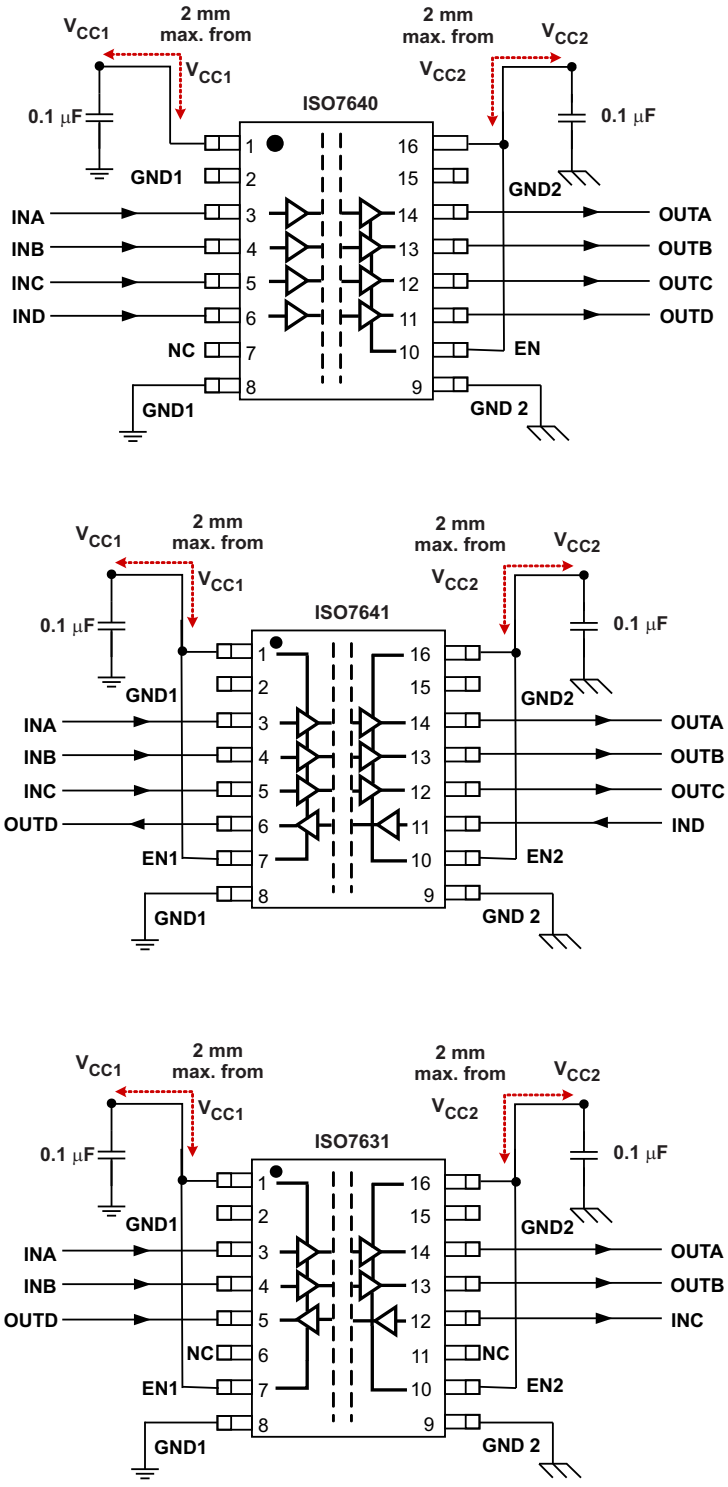


Figure 6. Typical ISO7640, ISO7641 and ISO7631 Application Circuit

Note: For detailed layout recommendations, see Application Note SLLA284, *Digital Isolator Design Guide*.

TYPICAL SUPPLY CURRENT EQUATIONS

(Calculated based on room temperature and typical Silicon process)

ISO7631FM:

At $V_{CC1} = V_{CC2} = 3.3V$

$I_{CC1} = 1.8072 + 0.0244 \times f + 0.0016 \times f \times C_L$

$I_{CC2} = 2.4625 + 0.0252 \times f + 0.0033 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 5V$

$I_{CC1} = 2.3183 + 0.04 \times f + 0.0025 \times f \times C_L$

$I_{CC2} = 3.2582 + 0.0403 \times f + 0.0049 \times f \times C_L$

ISO7631FC:

At $V_{CC1} = V_{CC2} = 3.3V$

$I_{CC1} = 1.1762 + 0.0325 \times f + 0.0017 \times f \times C_L$

$I_{CC2} = 1.5285 + 0.0299 \times f + 0.0033 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 5V$

$I_{CC1} = 1.6001 + 0.0528 \times f + 0.0025 \times f \times C_L$

$I_{CC2} = 2.2032 + 0.0475 \times f + 0.005 \times f \times C_L$

ISO7640FC:

At $V_{CC1} = V_{CC2} = 3.3V$

$I_{CC1} = 0.3209 + 0.0488 \times f$

$I_{CC2} = 1.9699 + 0.0385 \times f + 0.0066 \times f \times C_L$

At VCC1 = VCC2 = 5V

$I_{CC1} = 0.5038 + 0.0812 \times f$

$I_{CC2} = 2.6117 + 0.0603 \times f + 0.0101 \times f \times C_L$

ISO7641FC:

At $V_{CC1} = V_{CC2} = 3.3V$

$I_{CC1} = 1.2162 + 0.0462 \times f + 0.0017 \times f \times C_L$

$I_{CC2} = 1.8054 + 0.0411 \times f + 0.005 \times f \times C_L$

At $V_{CC1} = V_{CC2} = 5V$

$I_{CC1} = 1.6583 + 0.0757 \times f + 0.0025 \times f \times C_L$

$I_{CC2} = 2.5008 + 0.0655 \times f + 0.0076 \times f \times C_L$

I_{CC1} and I_{CC2} are typical supply currents measured in mA; f is data rate measured in Mbps; C_L is the capacitive load on each channel measured in pF.

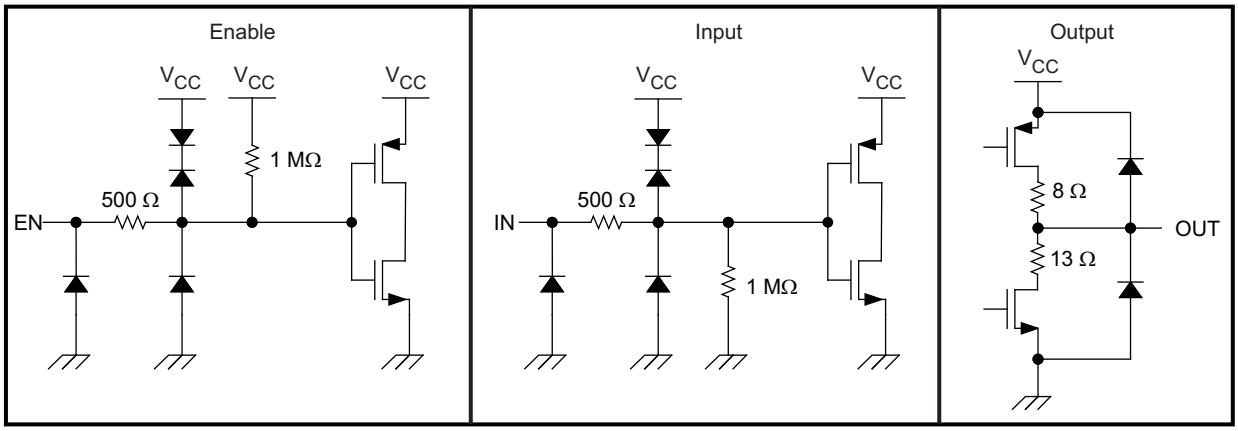


Figure 7. Device I/O Schematics

Copyright © 2012, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS

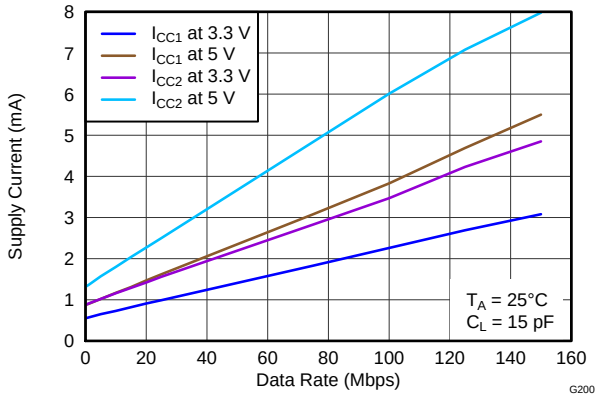


Figure 8. ISO7631FM Supply Current Per Channel vs Data Rate

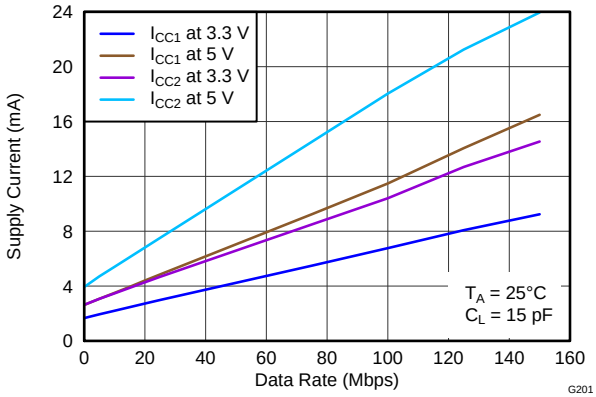


Figure 9. ISO7631FM Supply Current For All Channels vs Data Rate

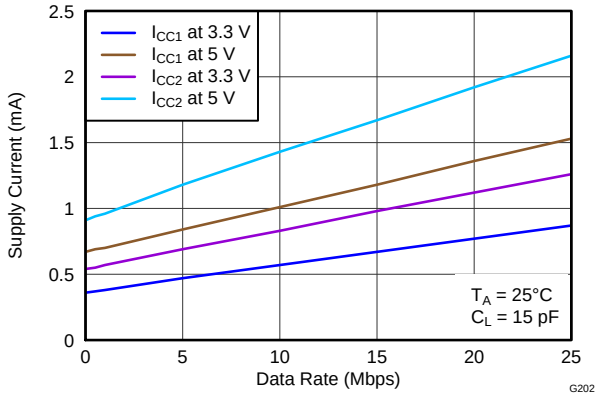


Figure 10. ISO7631FC Supply Current Per Channel vs Data Rate

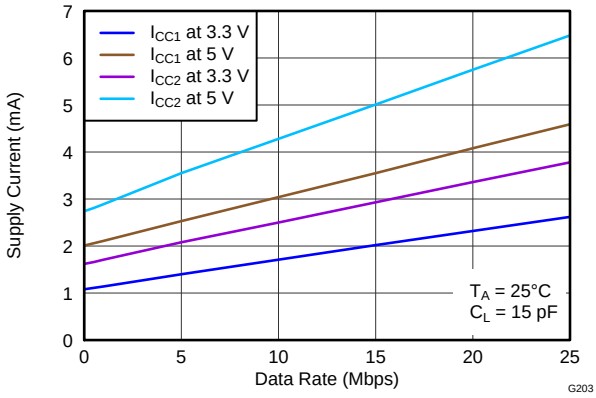


Figure 11. ISO7631FC Supply Current For All Channels vs Data Rate

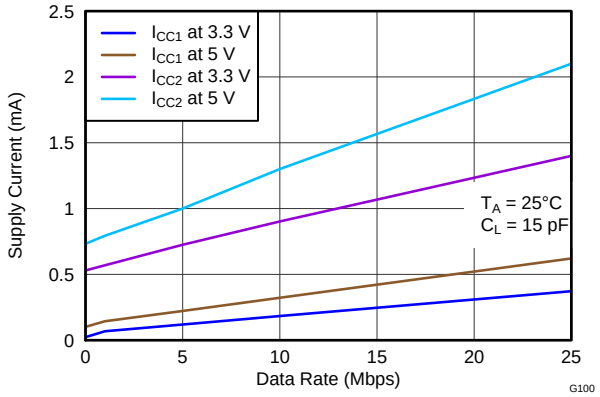


Figure 12. ISO7640FC Supply Current Per Channel vs Data Rate

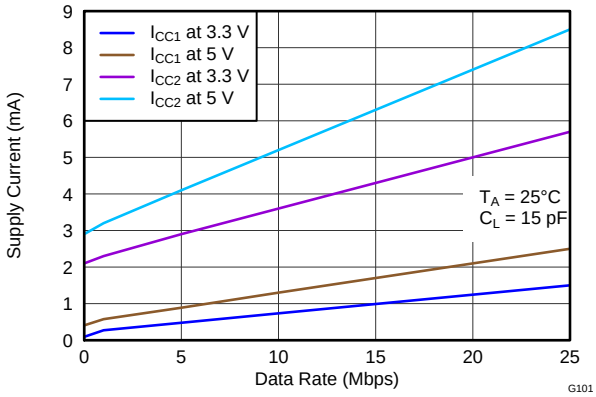


Figure 13. ISO7640FC Supply Current For All Channels vs Data Rate

Copyright © 2012, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

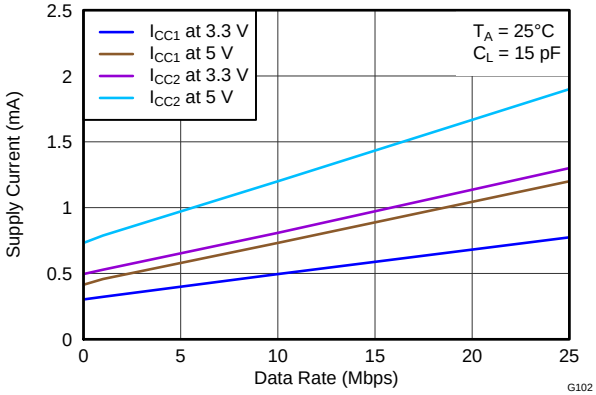


Figure 14. ISO7641FC Supply Current Per Channel vs Data Rate

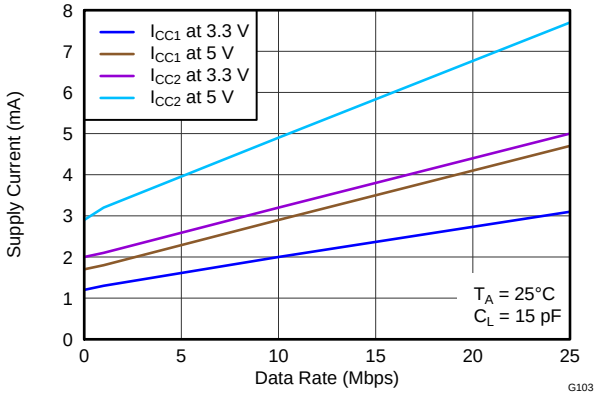


Figure 15. ISO7641FC Supply Current For All Channels vs Data Rate

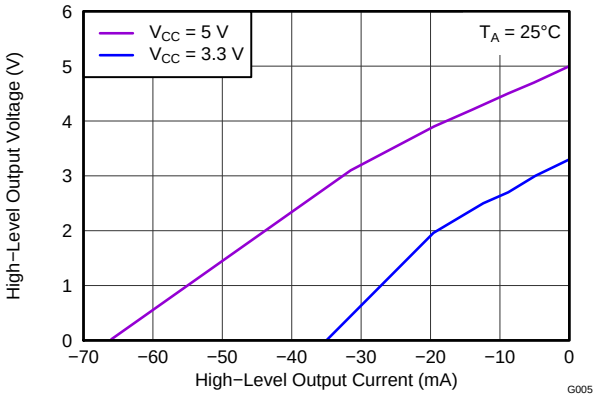


Figure 16. M-Grade High-Level Output Voltage vs High-Level Output Current

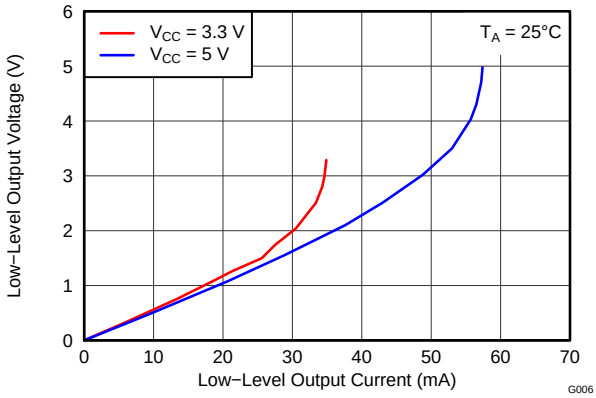


Figure 17. M-Grade Low-Level Output Voltage vs Low-Level Output Current

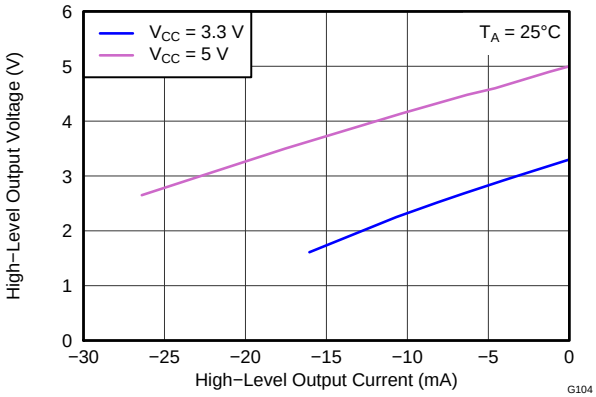


Figure 18. C-Grade High-Level Output Voltage vs High-Level Output Current

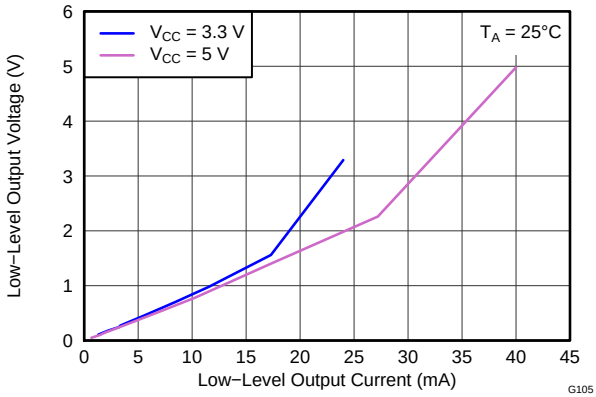


Figure 19. C-Grade Low-Level Output Voltage vs Low-Level Output Current

Copyright © 2012, Texas Instruments Incorporated

TYPICAL CHARACTERISTICS (continued)

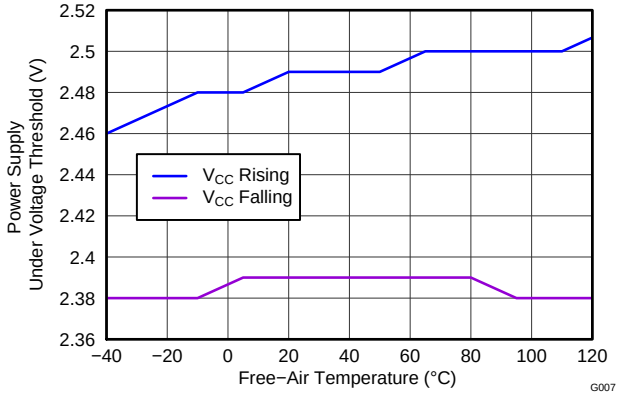


Figure 20. V_{CC} Undervoltage Threshold vs Free Air Temperature

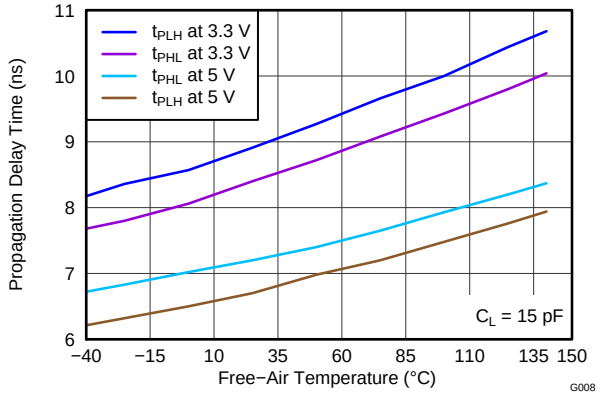


Figure 21. M-Grade Propagation Delay Time vs Free Air Temperature

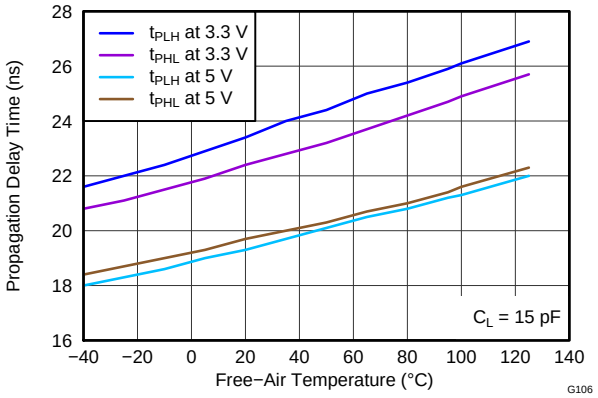


Figure 22. C-Grade Propagation Delay Time vs Free Air Temperature

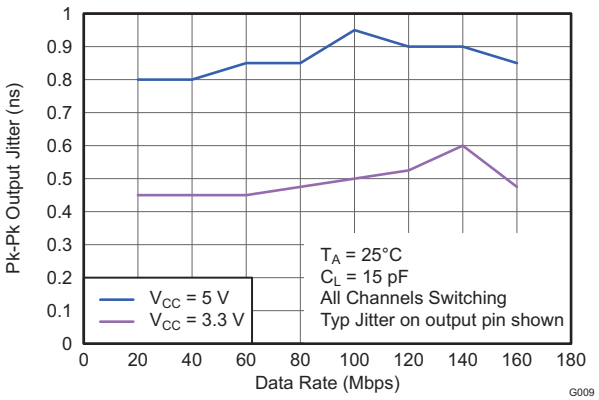


Figure 23. M-Grade Output Jitter vs Data Rate

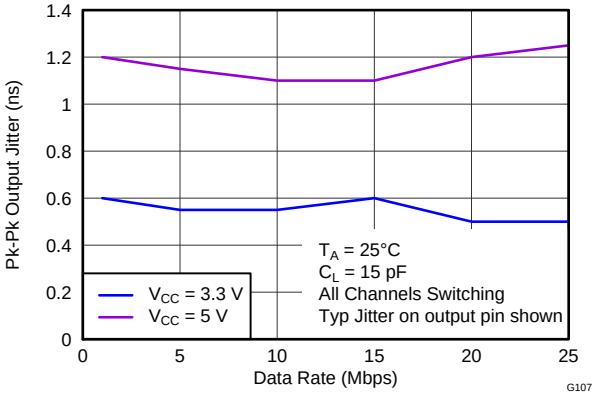


Figure 24. C-Grade Output Jitter vs Data Rate

TYPICAL CHARACTERISTICS (continued)

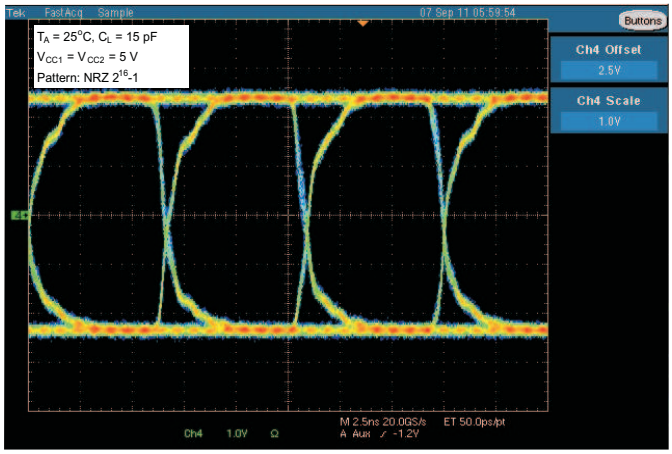


Figure 25. M-Grade Typical Eye Diagram at 150 Mbps, 5 V Operation

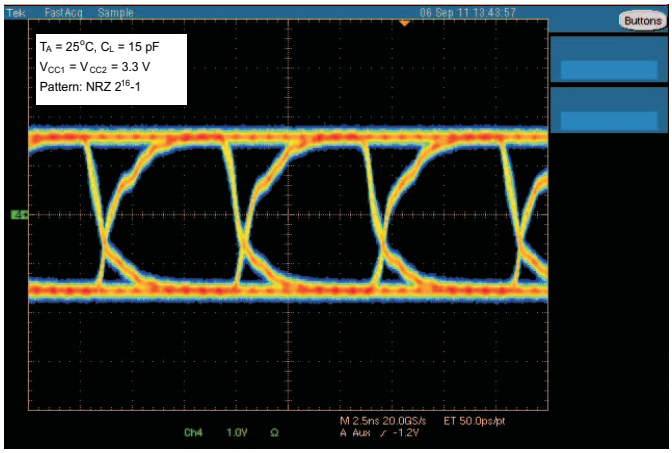


Figure 26. M-Grade Typical Eye Diagram at 150 Mbps, 3.3 V Operation

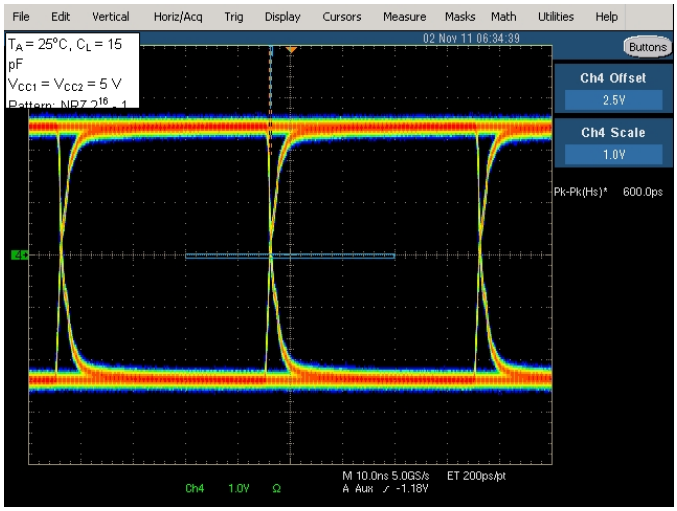


Figure 27. C-Grade Typical Eye Diagram at 25 Mbps, 5 V Operation

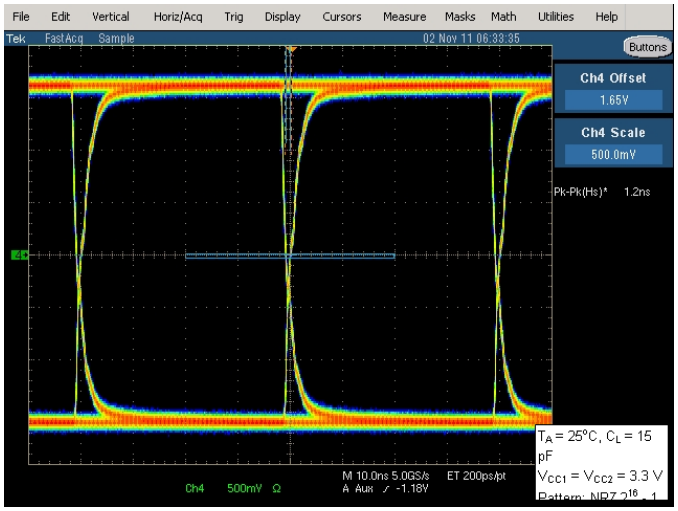


Figure 28. C-Grade Typical Eye Diagram at 25 Mbps, 3.3 V Operation

REVISION HISTORY

Changes from Original (September 2012) to Revision A **Page**

- Changed Description text From: "applications where input noise pulses of less than 10 ns duration..." To:"applications where input noise pulses of less than 6 ns duration..." 1
- Changed Input PU in the Function table From: Z To: 'Undetermined 2
- Added note "Product Preview" to ISO7640FC 3

Copyright © 2012, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ISO7631FCDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7631FCDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7631FMDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7631FMDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7641FCDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
ISO7641FCDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

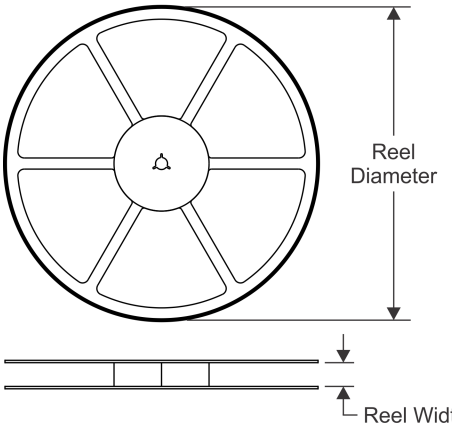
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

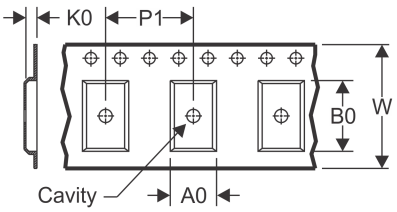
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

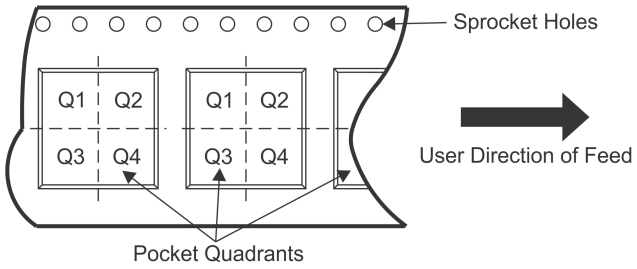


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

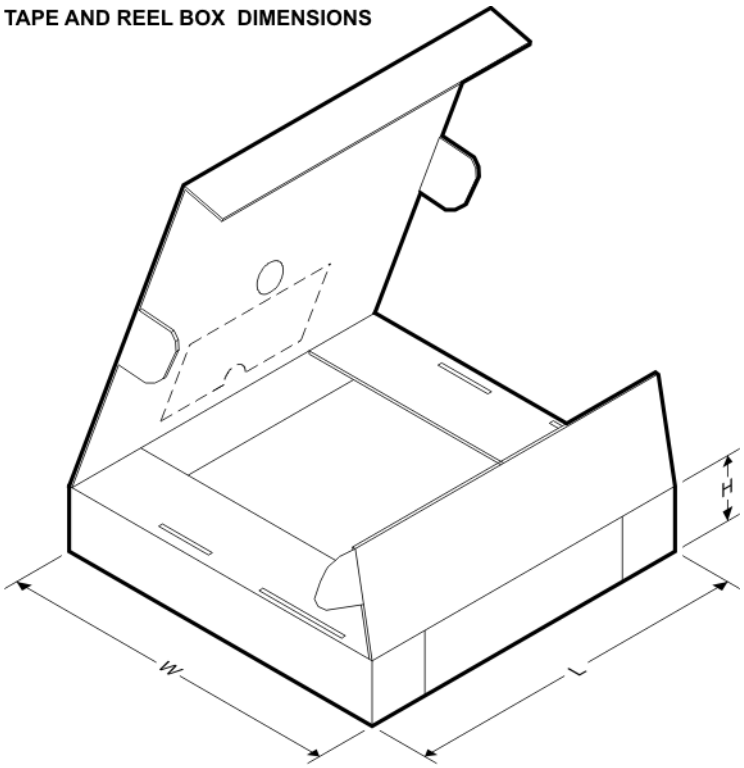
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7631FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7631FMDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7641FCDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

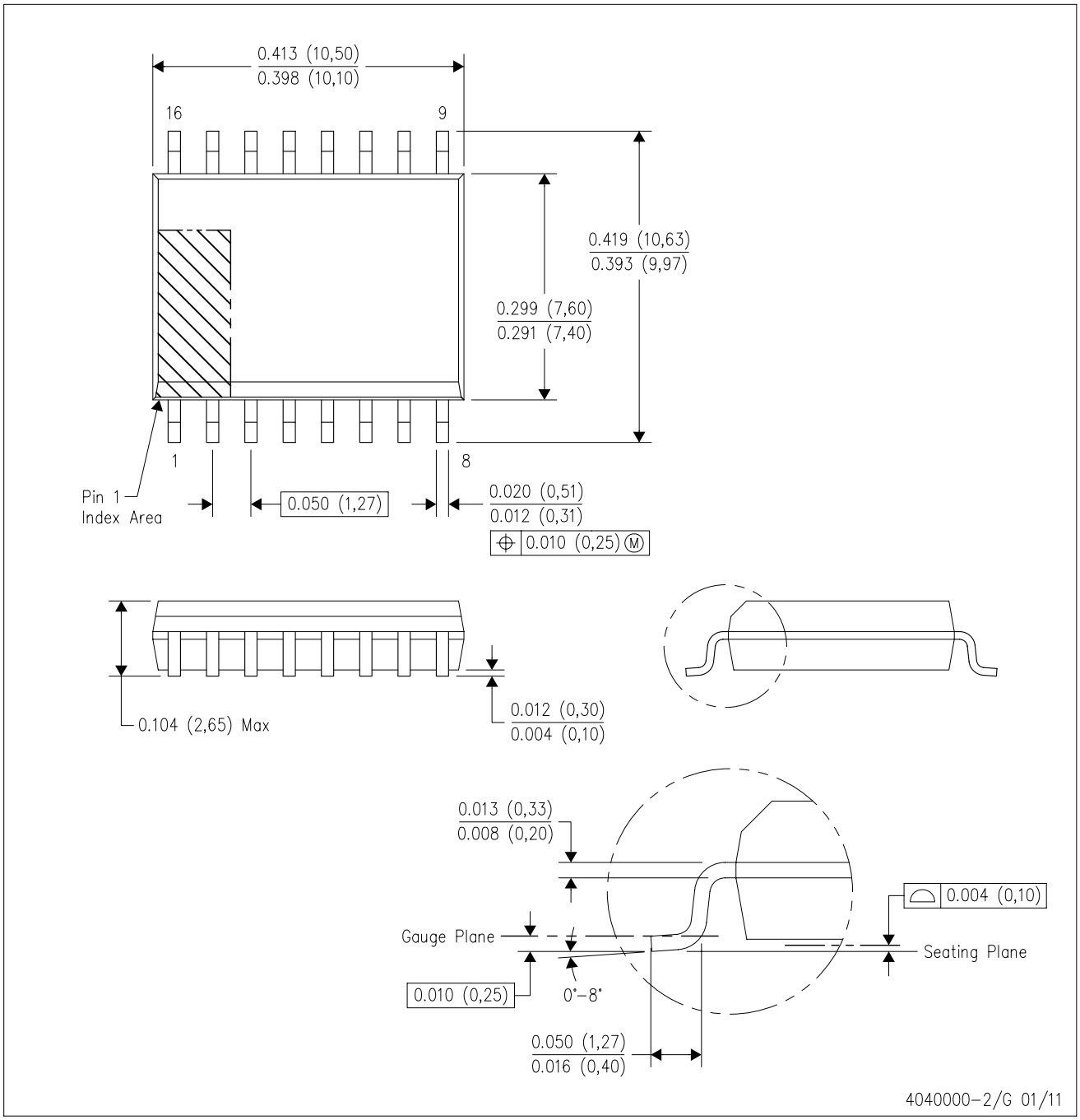
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

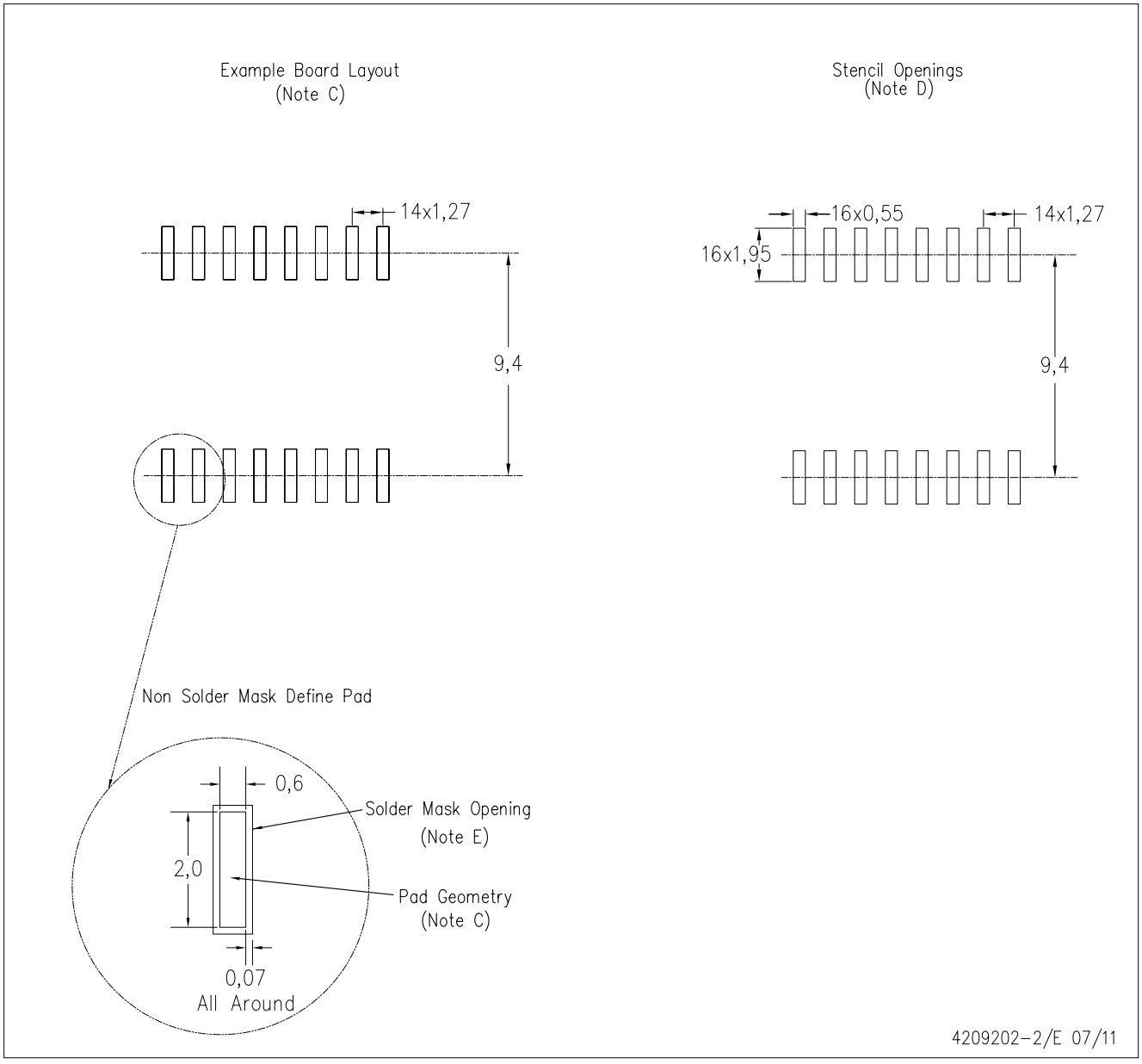
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7631FCDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7631FMDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ISO7641FCDWR	SOIC	DW	16	2000	367.0	367.0	38.0

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AA.

DW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated