FAIRCHILD SEMICONDUCTOR®

October 2009

FSQ500N
Green Mode Fairchild Power Switch (FPS™)

Features

- Single-Chip 700V SenseFET Power Switch
- Precision Fixed Operating Frequency: 130kHz
- No-Load Consumption 250mW at 265V_{AC} with Burst Mode
- Internal Startup Switch
- Soft-Start Time Tuned by External Capacitor
- Under-Voltage Lockout (UVLO) with Hysteresis
- Pulse-by-Pulse Current Limit
- Overload Protection (OLP) and Internal Thermal Shutdown Function (TSD) with Hysteresis
- Auto-Restart Mode
- No Need for Auxiliary Bias Winding

Applications

- STB and DSL Power Supply
- Home Appliance, IH Cooker, Auxiliary Power Supply

Related Resources

- *AN-4137-Design Guidelines for Off-line Flyback Converters using FPS*
- *AN-4141-Troubleshooting and Design Tips for Fairchild Power Switch (FPStm) Flyback Applications*
- *AN-4147-Design Guidelines for RCD Snubber of Flyback*
- *AN6075- (Flyback) -AN-6075-Compact Green-Mode Adapter Using FSQ500L for Low Cost*

Description

The FSQ500N is specially designed for low cost, small set-top box, DSL, home appliance auxiliary power supplies. This device combines a current-mode Pulse Width Modulator (PWM) with a SenseFET. The integrated PWM controller features include: a fixed oscillator, Under-Voltage Lockout (UVLO) protection, Overload Protection (OLP), Leading-Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection with hysteresis, and temperature-compensated precision-current sources for loop compensation. When compared to a linear power supply, the FSQ500N reduces total size and weight, while increasing efficiency, productivity, and system reliability. This device provides a basic platform for cost-effective flyback converters.



Maximum Output Power(1)			
230V_{AC} ± 15%(2)		85-265V_{AC}	
Adapter(3)	Open Frame(4)	Adapter(3)	Open Frame(4)
4.0W	6.5W	3.5W	5.5W

Notes:
1. The junction temperature can limit the maximum output power.
2. 230V_{AC} or 100/115V_{AC} with doubler.
3. Typical continuous power in a non-ventilated enclosed adapter measured at 50°C ambient.
4. Maximum practical continuous power in an open frame design at 50°C ambient.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FSQ500N	-40°C to +85°C	RoHS	8-Lead, Molded Dual Inline Package (MDIP), JEDEC MS-001, .300 Inch Wide	Rail

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

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Application Circuit Diagram

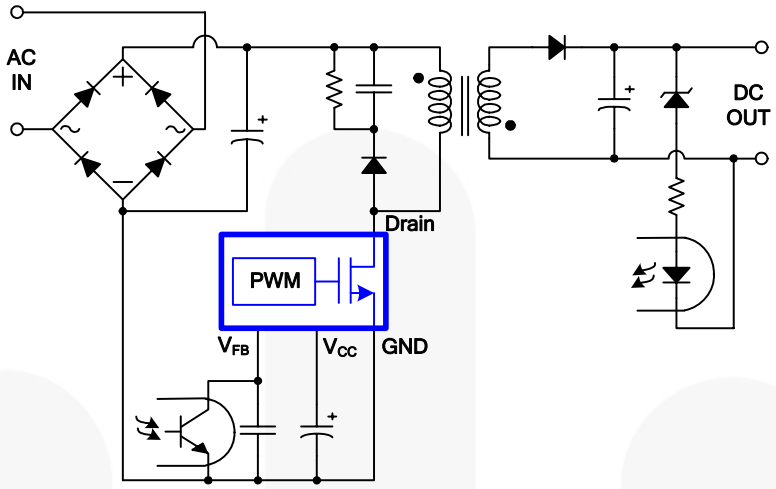


Figure 1. Typical Application Circuit

Internal Block Diagram

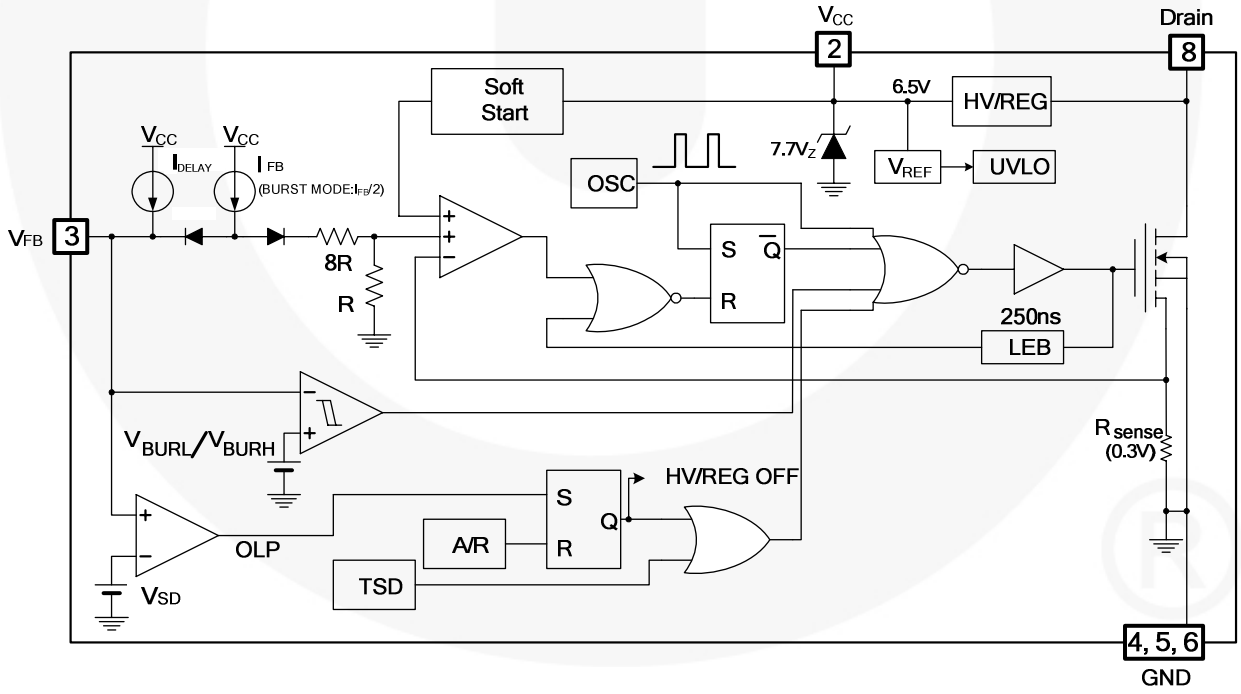


Figure 2. Internal Block Diagram

Pin Configuration

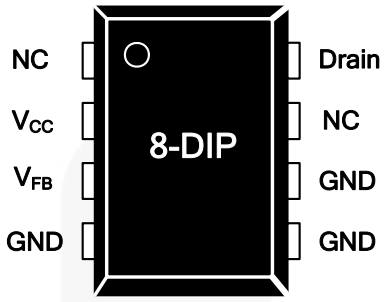


Figure 3. Package / Pin Diagram

Pin Definitions

Pin #	Name	Description
1	NC	No connection
2	V_{CC}	This pin is connected to a storage capacitor. A high-voltage regulator connected between pin 8 (V_{STR}) and this pin provides the supply voltage to the FSQ500N at startup and when switching during normal operation. The FSQ500N eliminates the need for auxiliary bias winding and associated external components.
3	V_{FB}	This pin is internally connected to the non-inverting input of the PWM comparator. The collector of an opto-coupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 4.5V, the overload protection triggers, which shuts down the FPS.
4, 5, 6	GND	This pin is the control ground and the SenseFET source.
7	NC	No connection
8	Drain	High-voltage power SenseFET drain connection

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{DS}	Drain Pin Voltage[5]	700		V
V_{CC}	Supply Voltage		10	V
V_{FB}	Feedback Voltage Range	-0.3	V_{CC}	V
P_D	Total Power Dissipation		1.42	W
I_{DM}	Drain Current Pulsed[6]		0.41	A
T_J	Operating Junction Temperature	-40	+150	°C
T_{STG}	Storage Temperature	-55	+150	°C
ESD[7]	Human Body Model, JESD22-A114		2.5	KV
	Charged Device Model, JESD22-C101		2	

Notes:
5. LDMOS available drain voltage is -0.3V ~ 700V.
6. Repetitive rating: pulse width is limited by maximum junction temperature.
7. Meet JEDEC Standards JESD 22-A114 and JESD 22-C101

Thermal Impedance

Symbol	Parameter	Value	Unit
θ_{JA}[8][9]	Junction-to-Ambient Thermal Resistance	88	°C/W
θ_{JC}[8][10]	Junction-to-Case Thermal Resistance	19	°C/W

Note:
8. All items are tested with the standards JESD 51-2 and JESD 51-10 (DIP Package).
9. θ_{JA} Free-standing, with no heat-sink, under natural convection.
10. θ_{JC}, Junction to lead thermal characteristics under Θ_{JA} test condition. T_C is measured on the source #7 pin closed to plastic interface for Θ_{JA} thermo couple is mounted on soldering.

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Electrical Characteristics

T_J = 25°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
SenseFET Section						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{CC} = 6.5V, V_{FB} = 0V, I_D = 150μA	700			V
I_{DSS}	Zero-Gate-Voltage Drain Current	V_{CC} = 6.5V, V_{FB} = 0V, V_{DS} = 700V			150	μA
$R_{DS(ON)}$	Drain-Source On-State Resistance	T_J = 25°C, I_D = 25mA		25	29	Ω
		T_J = 100°C, I_D = 25mA		35	41	Ω
C_{ISS}	Input Capacitance[11]	V_{GS} = 6.5V		42		pF
C_{OSS}	Output Capacitance[11]	V_{DS} = 40V, f_S = 1MHz		25		pF
t_r	Rise Time[11]	V_{DS} = 350V, I_D = 25mA		100		ns
t_f	Fall Time[11]	V_{DS} = 350V, I_D = 25mA		50		ns
Control Section						
f_S	Switching Frequency	V_{CC} = 6.5V, V_{FB} = 1.0V	120	130	140	kHz
Δf_S	Switching Frequency Variation[11]	-25°C < T_J < 125°C		±5	±7	%
$I_{FB(Burst)}$	Feedback Source Current	V_{CC} = 6.5V, V_{FB} = 0V	98	110	122	μA
$I_{FB(Normal)}$		V_{CC} = 6.5V	200	225	250	μA
D_{MAX}	Maximum Duty Ratio	V_{CC} = 6.5V, V_{FB} = 4.0V	54	60	66	%
D_{MIN}	Minimum Duty Ratio	V_{CC} = 6.5V, V_{FB} = 0V			0	%
V_{START}	UVLO Threshold Voltage	V_{FB} = 0V, V_{CC} Sweep	5.5	6.0	6.5	V
V_{STOP}		After Turn-on, V_{FB} = 0V, V_{CC} Sweep	4.5	5.0	5.5	V
V_{DLY_EN}	Shutdown Delay Current Enable Voltage	V_{FB} = V_{SD}, V_{CC} Sweep from 6V	6.0	6.5	7.0	V
Burst-Mode Section						
V_{BURH}	Burst Mode Voltage	V_{CC} = 6.5V, V_{FB} Sweep	0.75	0.80	0.85	V
V_{BURL}			0.70	0.75	0.80	V
HYS			30	50	80	mV
Protection Section						
I_{LIM}	Peak Current Limit	di/dt = 150mA/μs	280	320	360	mA
V_{SD}	Shutdown Feedback Voltage	V_{CC} = 6.5V, V_{FB} Sweep	4.1	4.5	4.9	V
I_{DELAY}	Shutdown Delay Current	V_{CC} = 6.5V, V_{FB} = 4.0V	4	5	6	μA
t_{LEB}	Leading-Edge Blanking Time[11]			250		ns
t_{CLD}	Current Limit Delay Time[11]			100		ns
TSD	Thermal Shutdown Temperature[11]		130	140	150	°C
HYS				80		°C
Total Device Section						
$I_{OP-BURST}$	Operating Supply Current (Control Part Only)	V_{CC} = 6.5V, V_{FB} = 0V	360	430	500	μA
I_{OP-FB}		V_{CC} = 6.5V, V_{FB} = 4V	640	760	880	μA
I_{CH}	Startup Charging Current	V_{CC} = V_{FB} = 0V, V_{DS} = 40V	3.3			mA
V_{CCREG}	Supply Shunt Regulator	V_{DS} = 40V, V_{FB} = 0V	6.0	6.5	7.0	V
V_{CCREG_TSD}	Supply Shunt Regulator During TSD[11]		5.2	5.7	6.2	V

Note:

11. These parameters, although guaranteed, are not 100% tested in production.

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Typical Performance Characteristics

These characteristic graphs are measured at T_A = 25°C.

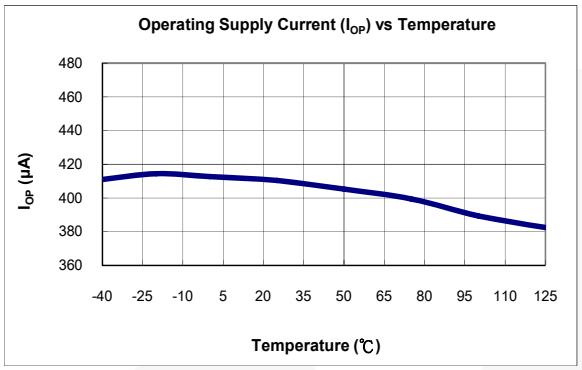


Figure 4. Operating Supply Current (I_{OP_Burst}) vs. Temperature

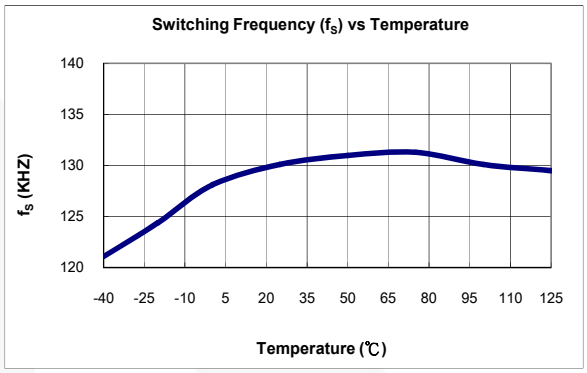


Figure 5. Switching Frequency (f_S) vs. Temperature

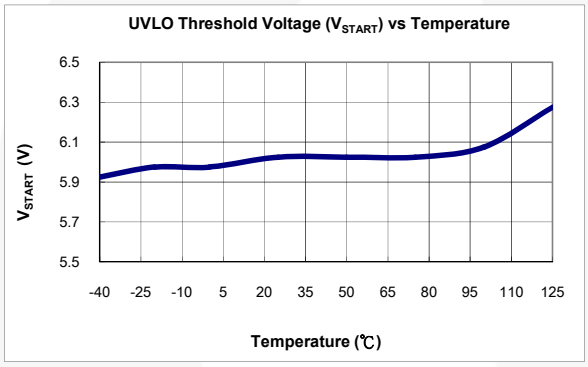


Figure 6. UVLO Threshold Voltage (V_{START}) vs. Temperature

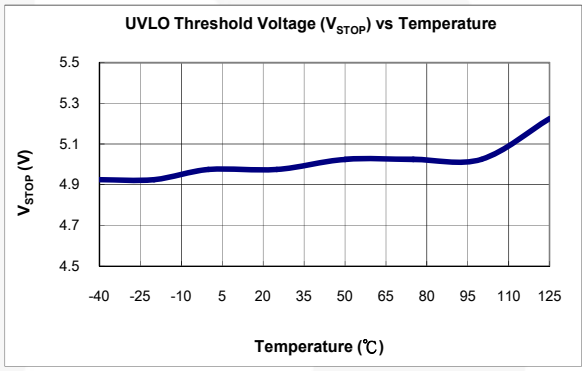


Figure 7. UVLO Threshold Voltage (V_{STOP}) vs. Temperature

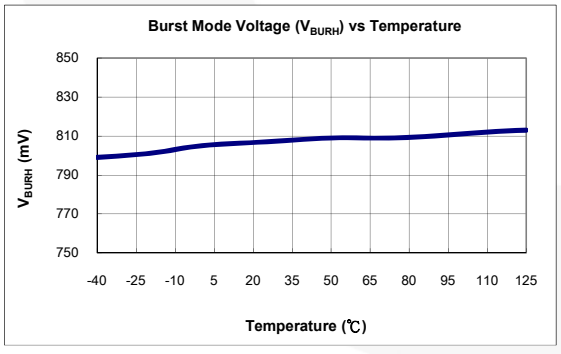


Figure 8. Burst-Mode Voltage (V_{BURH}) vs. Temperature

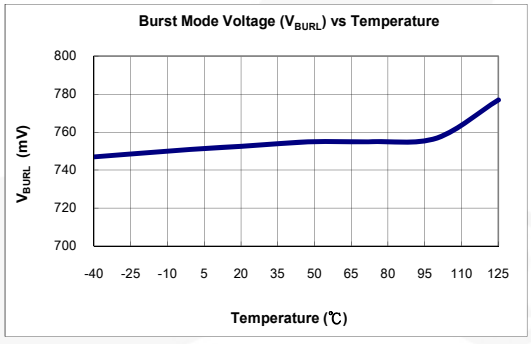


Figure 9. Burst-Mode Voltage (V_{BURL}) vs. Temperature

Typical Performance Characteristics (Continued)

These characteristic graphs are measured at T_A = 25°C.

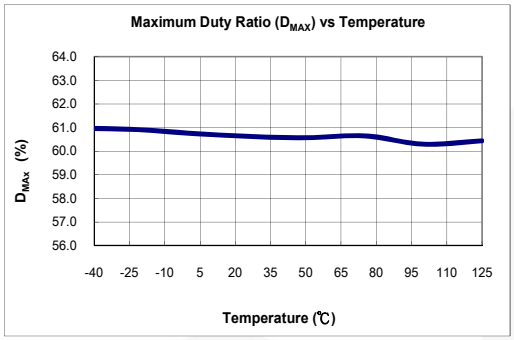


Figure 10. Maximum Duty Ratio (D_{MAX}) vs. Temperature

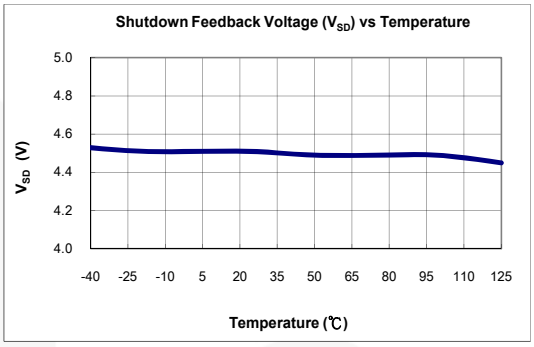


Figure 11. Shutdown Feedback Voltage (V_{SD}) vs. Temperature

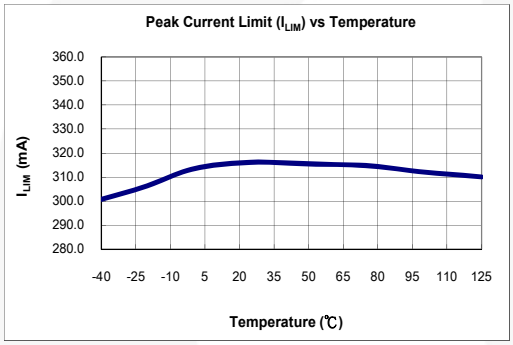


Figure 12. Peak Current Limit (I_{LIM}) vs. Temperature

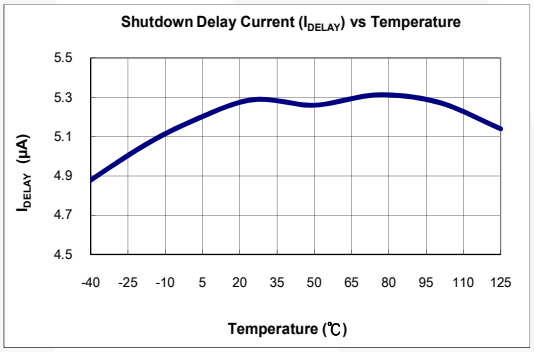


Figure 13. Shutdown Delay Current (I_{DELAY}) vs. Temperature

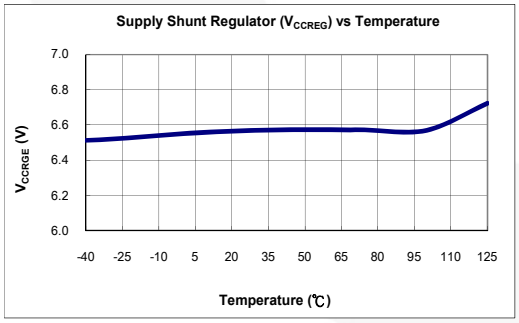


Figure 14. Supply Shunt Regulator (V_{CCREG}) vs. Temperature

Functional Description

1. Startup and V_{CC} Regulation: At startup, an internal high-voltage current source supplies the internal bias and charges the external capacitor (C_A) connected to the V_{CC} pins, as illustrated in Figure 15. An internal high-voltage regulator (HV/REG) located between the Drain and V_{CC} pins regulates the V_{CC} to 6.5V and supplies operating current. Therefore, FSQ500N needs no auxiliary bias winding.

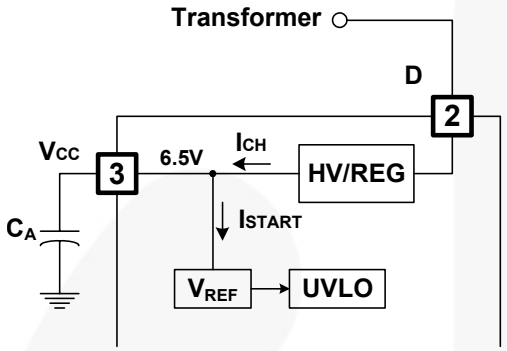


Figure 15. Startup Block

2. Feedback Control: FSQ500N employs current-mode control, as shown in Figure 16. An opto-coupler (such as the FOD817A) and shunt regulator (such as the KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{sense} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the regulator exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, pulling down the feedback voltage and reducing the duty cycle. This typically occurs when the line input voltage increases or the output load current decreases.

2.1 Pulse-by-Pulse Current Limit: Because current-mode control is employed, the peak current through the senseFET is limited by the non-inverting input of PWM comparator (V_{FB}*), as shown in Figure 16. Assuming that 225μA current source flows only through the internal resistor (8R + R = 12kΩ), the cathode voltage of diode D2 is about 2.7V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.7V, the maximum voltage of the cathode of D2 is clamped at this voltage, clamping V_{FB}*. Therefore, the peak value of the current through the senseFET is limited.

2.2 Leading-Edge Blanking (LEB): At the instant the internal senseFET is turned on, a high-current spike occurs through the senseFET, caused by primary-side capacitance and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FPS employs a leading-edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB} = 250ns) after the senseFET turns on.

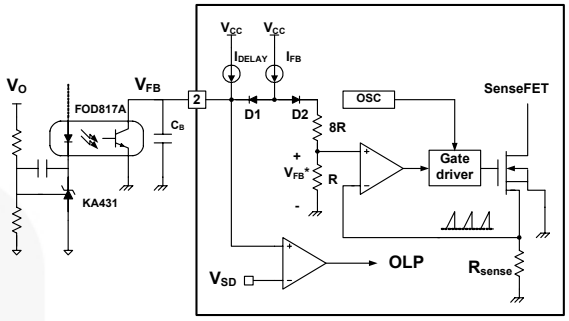


Figure 16. Pulse Width Modulation (PWM) Circuit

3. Protection Circuits: The FSQ500N has two self-protective functions: overload protection (OLP) and thermal shutdown (TSD). While OLP is implemented as auto-restart mode, there is no switching when TSD triggers. Once the overload condition is detected; switching is terminated, the senseFET remains off, and HV/REG turns off. This causes V_{CC} to fall. When V_{CC} falls below the under-voltage lockout (UVLO) stop voltage of 5.0V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When V_{CC} reaches the start voltage of 6.0V, the FSQ500N resumes its normal operation. If the fault condition is still not removed, the senseFET and HV/REG remain off and V_{CC} drops to V_{STOP} again. In this manner, the auto-restart can alternately enable and disable the switching of the power senseFET until the fault condition is eliminated, as shown in Figure 17.

Because these protection circuits are fully integrated into the IC without external components, reliability is improved without increasing cost.

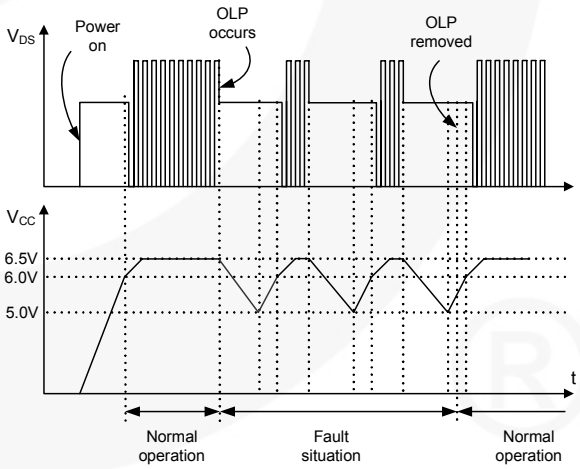


Figure 17. Auto Restart Protection Waveforms

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3.1 Overload Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during the load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger after a specified time to determine whether the situation is transient or a true overload. Because of the pulse-by-pulse current limit capability, the maximum peak current through the senseFET is limited and, therefore, the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto-coupler LED, which also reduces the opto-coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.7V, D1 is blocked and the 5μA current source starts to charge C_B slowly up to V_{CC}. In this condition, V_{FB} continues increasing until it reaches 4.5V, when the switching operation is terminated, as shown in Figure 18. The delay time for shutdown is the time required to charge C_B from 2.7V to 4.5V with 5μA. In general, a 10 ~ 50ms delay is typical for most applications. This protection is implemented in auto-restart mode.

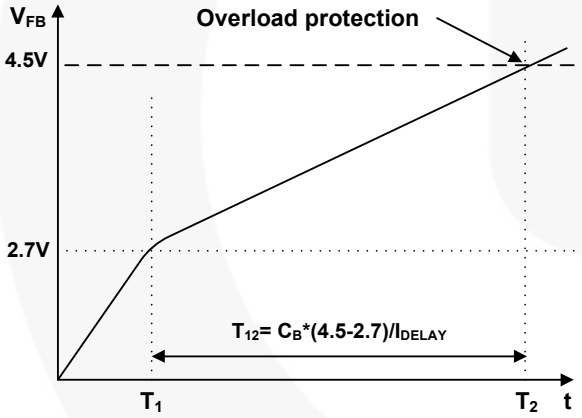


Figure 18. Overload Protection

3.2 Thermal Shutdown (TSD): The senseFET and the control IC in one package makes it easy for the control IC to detect an abnormal over temperature of the senseFET. When the temperature exceeds ~140°C, the thermal shutdown triggers. When TSD triggers, delay current is disabled, switching operation stops, and V_{CC} through the internal high-voltage current source is set to 5.7V from 6.5V, as shown in Figure 19. Since the TSD signal prohibits the senseFET from switching, there is no switching until the junction temperature decreases sufficiently. If the junction temperature is lower than 60°C typically, TSD signal is removed and V_{CC} is set to 6.5V again. While V_{CC} increases from 5.7V to 6.5V, the soft-start function makes the senseFET turn on and off with no voltage and/or current stress.

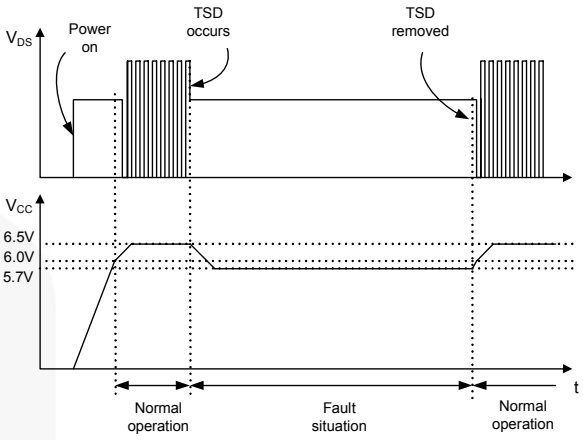


Figure 19.Over-Temperature Protection (OTP)

4. Soft-Start: The soft-start time is tuned by an external V_{CC} capacitor (C_A), which increases PWM comparator non-inverting input voltage together with the senseFET current slowly after it starts. Before V_{CC} reaches V_{START}, C_A is charged by the current I_{CH}-I_{START}, where I_{CH} and I_{START} are described in Figure 15. After V_{CC} reaches V_{START}, all internal blocks are activated, so that the current consuming inside IC becomes I_{OP}. Therefore, C_A is charged by the current I_{CH}-I_{OP}, which makes the increasing slope of V_{CC} become sluggish. V_{CC} is shifted by 6.0V negatively (it is performed in soft-start block in Figure 2), then V_{CC} -6.0V is an input of one of the input terminals of the PWM comparator. The drain current follows V_{CC} -6.0V instead of the V_{FB}* because of the low-dominant feature of the PWM comparator. The soft-start time can be made long or short by selecting C_A, as described in Figure 20. During $t_{S/S}$, I_{DELAY} is disabled to avoid unwanted OLP. Typically, $t_{S/S}$ is around 4.6ms with 27μF of C_A.

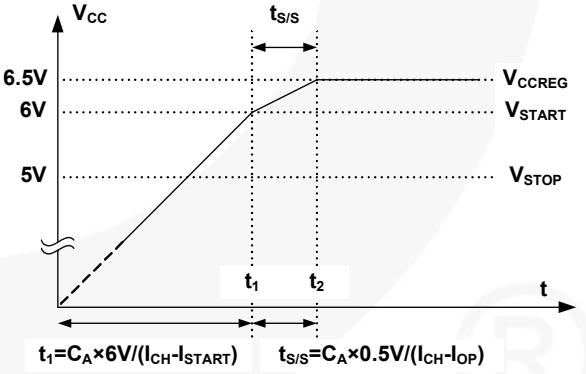


Figure 20. Soft-Start Function

The peak value of the drain current of the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce stress on the secondary diode during startup.

5. Burst Operation: To minimize power dissipation in standby mode, the FPS enters burst-mode operation. During the burst-mode operation, $I_{FB(Burst)}$ decreases half of $I_{FB(Normal)}$. As the load decreases, the feedback voltage decreases. As shown in Figure 21, the device automatically enters burst mode when the feedback voltage drops below V_{BURL} (750mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (800mV), switching resumes. The feedback voltage then falls and the process repeats. Burst mode alternately enables and disables switching of the power senseFET, reducing switching loss in standby mode.

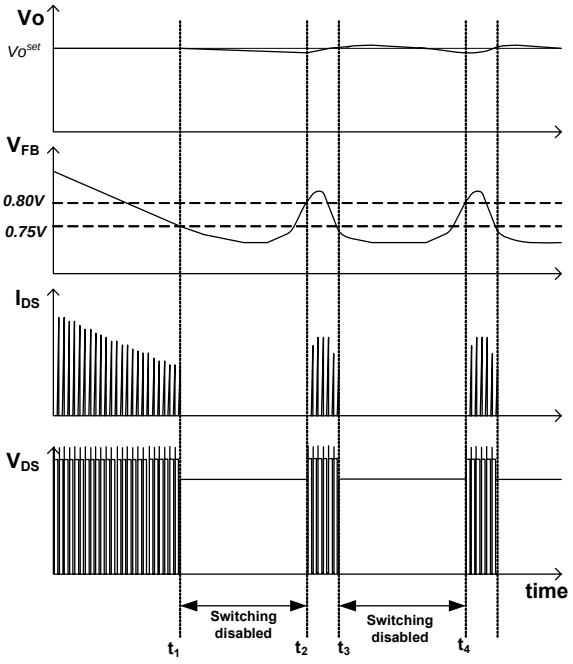
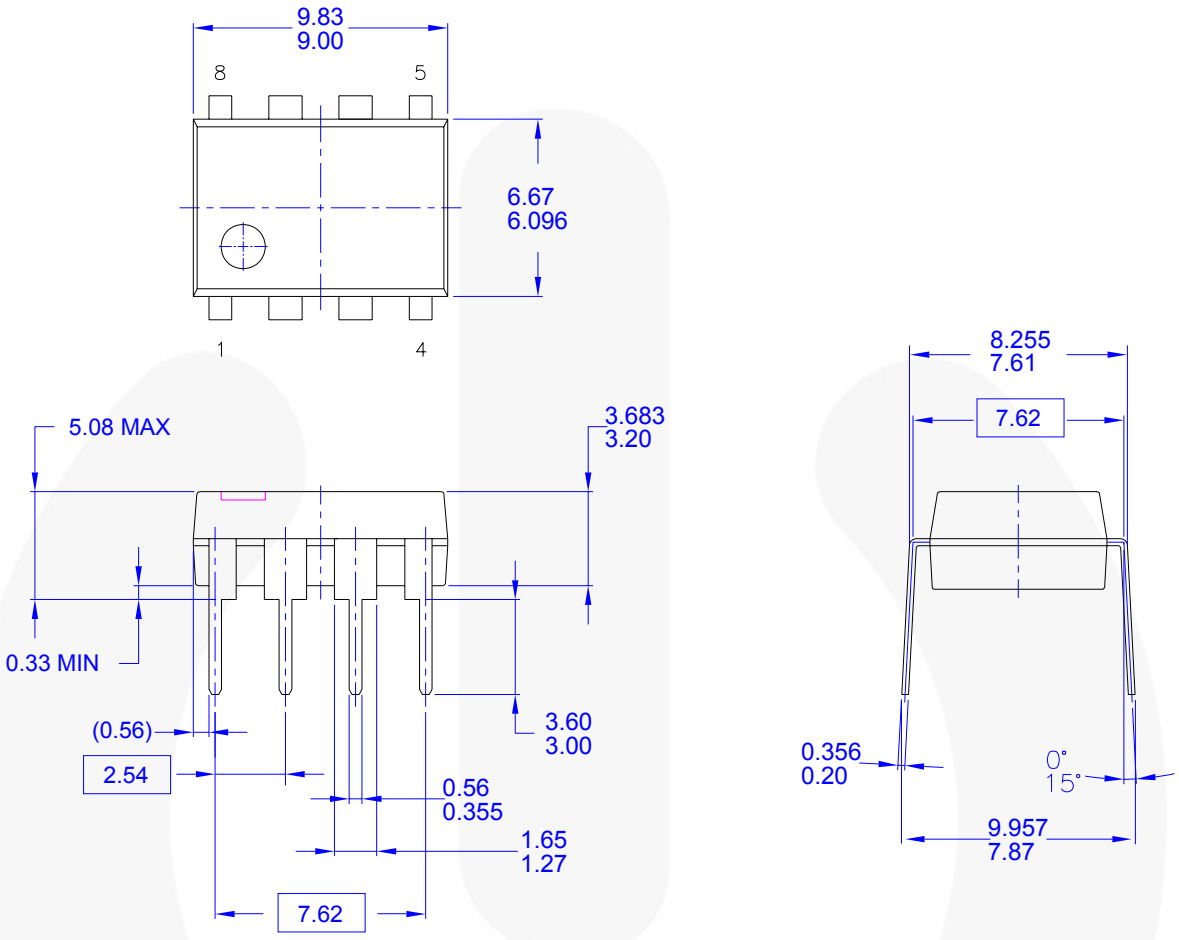


Figure 21. Burst-Mode Operation

Package Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

E) DRAWING FILENAME AND REVSION: MKT-N08FREV2.

Figure 22. 8-Lead, Molded Dual Inline Package (MDIP)

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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