International
IOR Rectifier

# IRF7351PbF

HEXFET® Power MOSFET

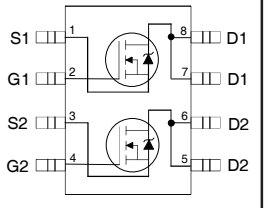
| $V_{DSS}$ | $R_{DS(on)}$ max | Qg (typ.) |
|---|---|---|
| 60V | 17.8mΩ@$V_{GS}$ = 10V | 24nC |

## Applications

- Synchronous Rectifier MOSFET for Isolated DC-DC Converters
- Low Power Motor Drive Systems

## Benefits

- Ultra-Low Gate Impedance
- Fully Characterized Avalanche Voltage and Current
- 20V $V_{GS}$ Max. Gate Rating



Top View


SO-8

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 60 | V |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | |
| $I_D$ @ $T_A$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V | 8.0 | A |
| $I_D$ @ $T_A$ = 70°C | Continuous Drain Current, $V_{GS}$ @ 10V | 6.4 | |
| $I_{DM}$ | Pulsed Drain Current ① | 64 | |
| $P_D$ @$T_A$ = 25°C | Power Dissipation ④ | 2.0 | W |
| $P_D$ @$T_A$ = 70°C | Power Dissipation ④ | 1.28 | |
| | Linear Derating Factor | 0.016 | W/°C |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 150 | °C |

## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JL}$ | Junction-to-Drain Lead ⑤ | ––– | 20 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient ④ ⑤ | ––– | 62.5 | |

Notes ① through ⑤ are on page 10

## Static @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-to-Source Breakdown Voltage | 60 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| $\Delta BV_{DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.068 | — | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | 13.7 | 17.8 | mΩ | $V_{GS}$ = 10V, $I_D$ = 8.0A ③ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 50µA |
| $\Delta V_{GS(th)}$ | Gate Threshold Voltage Coefficient | — | -8.2 | — | mV/°C | |
| $I_{DSS}$ | Drain-to-Source Leakage Current | — | — | 20 | µA | $V_{DS}$ = 60V, $V_{GS}$ = 0V |
| | | — | — | 250 | | $V_{DS}$ = 60V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | $V_{GS}$ = -20V |
| gfs | Forward Transconductance | 18 | — | — | S | $V_{DS}$ = 25V, $I_D$ = 6.4A |
| $Q_g$ | Total Gate Charge | — | 24 | 36 | | |
| $Q_{gs1}$ | Pre-Vth Gate-to-Source Charge | — | 3.8 | — | | $V_{DS}$ = 30V |
| $Q_{gs2}$ | Post-Vth Gate-to-Source Charge | — | 1.2 | — | nC | $V_{GS}$ = 10V |
| $Q_{gd}$ | Gate-to-Drain Charge | — | 7.2 | — | | $I_D$ = 6.4A |
| $Q_{godr}$ | Gate Charge Overdrive | — | 11.8 | — | | See Fig. 17 |
| $Q_{sw}$ | Switch Charge ($Q_{gs2}$ + $Q_{gd}$) | — | 8.4 | — | | |
| $Q_{oss}$ | Output Charge | — | 7.5 | — | nC | $V_{DS}$ = 16V, $V_{GS}$ = 0V |
| $t_{d(on)}$ | Turn-On Delay Time | — | 5.1 | — | | $V_{DD}$ = 30V, $V_{GS}$ = 10V ③ |
| $t_r$ | Rise Time | — | 5.9 | — | ns | $I_D$ = 6.4A |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 17 | — | | $R_G$ = 1.8Ω |
| $t_f$ | Fall Time | — | 6.7 | — | | |
| $C_{iss}$ | Input Capacitance | — | 1330 | — | | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | — | 190 | — | pF | $V_{DS}$ = 30V |
| $C_{rss}$ | Reverse Transfer Capacitance | — | 92 | — | | $f$ = 1.0MHz |

## Avalanche Characteristics

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $E_{AS}$ | Single Pulse Avalanche Energy ② | — | 325 | mJ |
| $I_{AR}$ | Avalanche Current ① | — | 6.4 | A |

## Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | — | — | 1.8 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | — | — | 64 | | |
| $V_{SD}$ | Diode Forward Voltage | — | — | 1.3 | V | $T_J$ = 25°C, $I_S$ = 6.4A, $V_{GS}$ = 0V ③ |
| $t_{rr}$ | Reverse Recovery Time | — | 20 | 30 | ns | $T_J$ = 25°C, $I_F$ = 6.4A, $V_{DD}$ = 30V |
| $Q_{rr}$ | Reverse Recovery Charge | — | 61 | 92 | nC | di/dt = 300A/µs ③ |

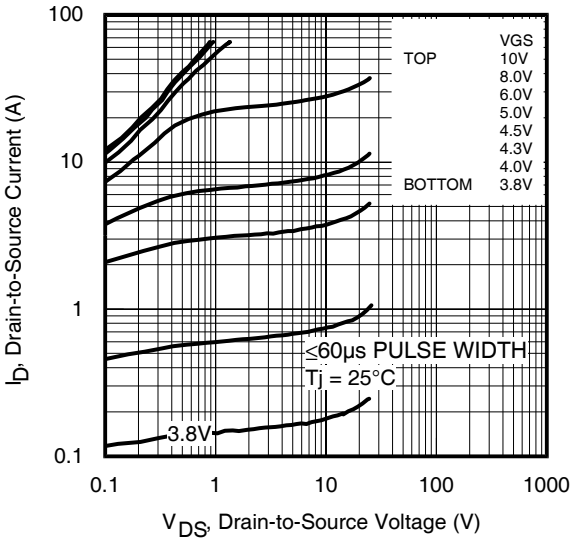



**Fig 1.** Typical Output Characteristics

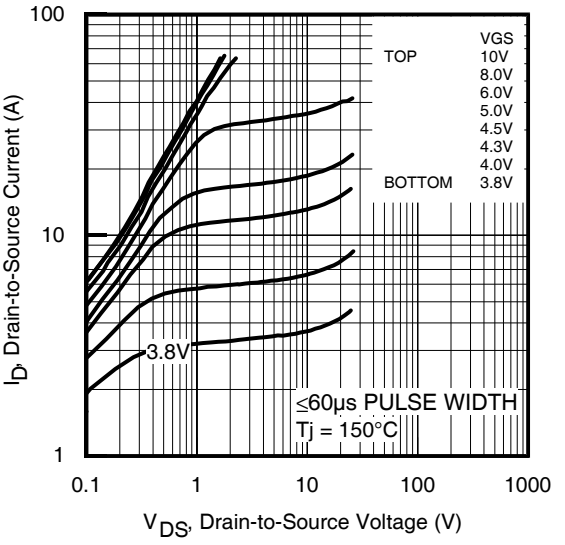



**Fig 2.** Typical Output Characteristics

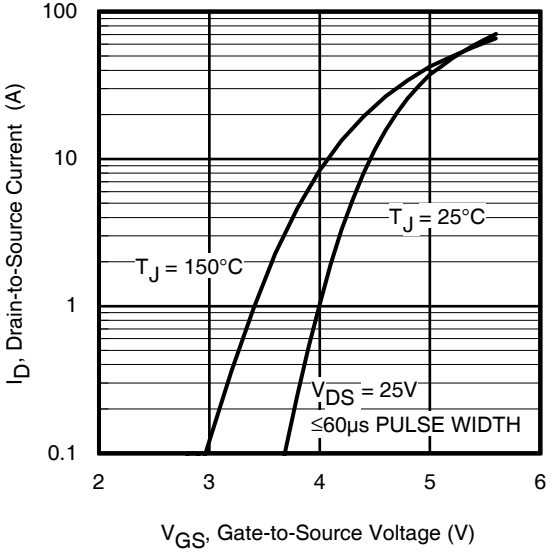



**Fig 3.** Typical Transfer Characteristics

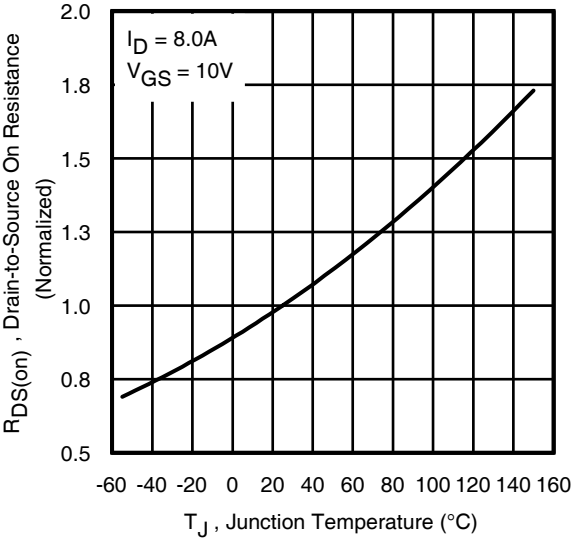



**Fig 4.** Normalized On-Resistance vs. Temperature

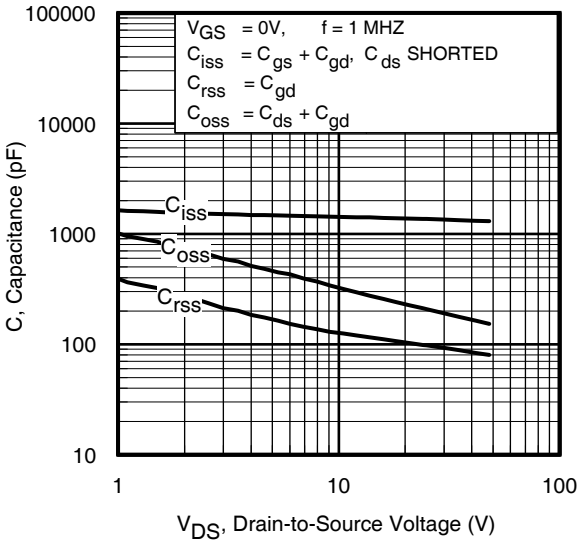



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

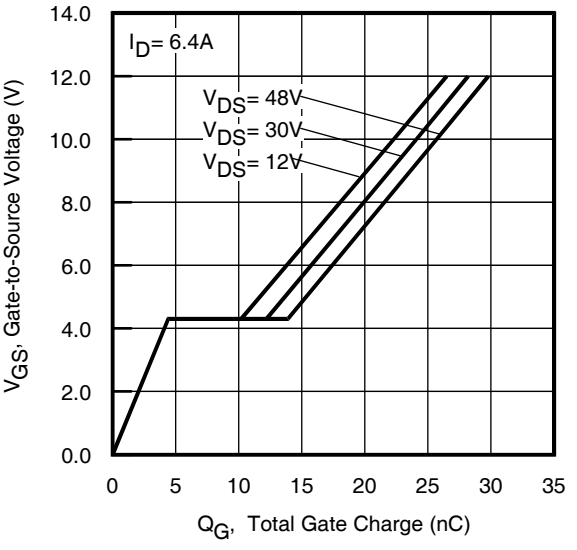



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

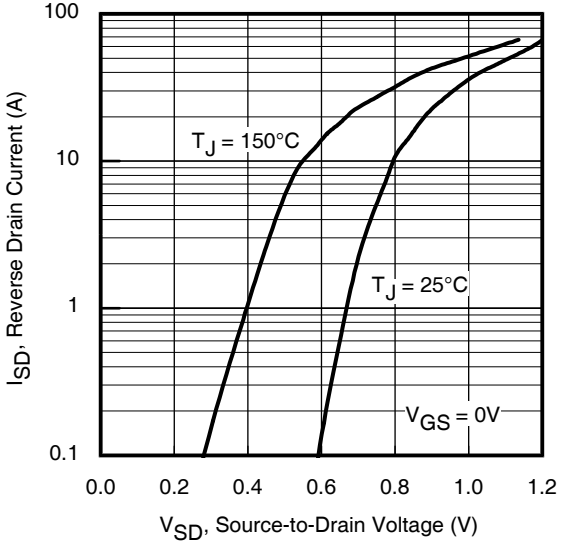



**Fig 7.** Typical Source-Drain Diode Forward Voltage

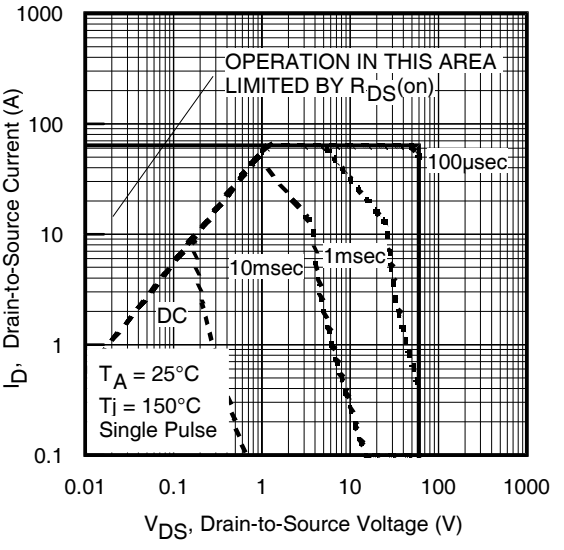



**Fig 8.** Maximum Safe Operating Area

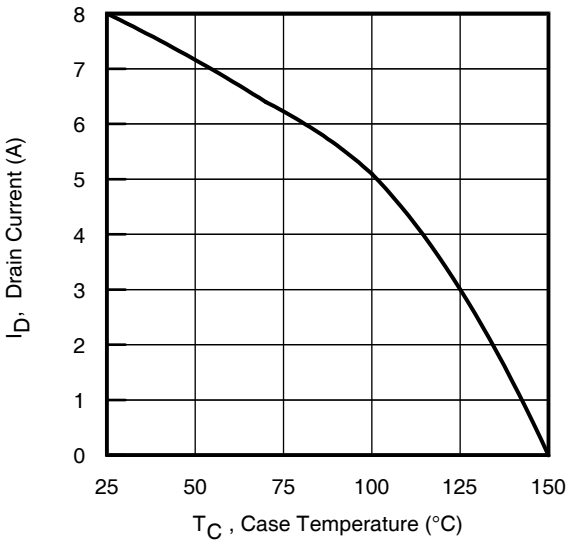



**Fig 9.** Maximum Drain Current vs. Case Temperature

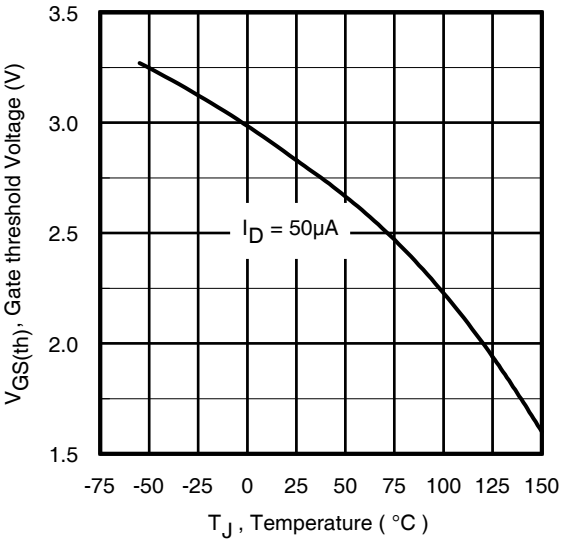
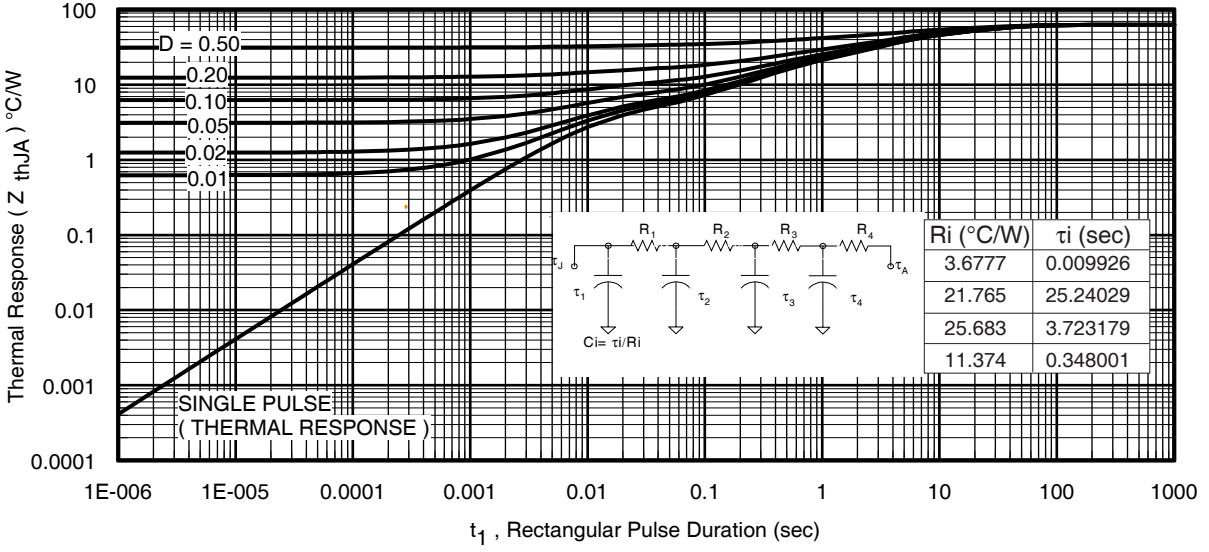



**Fig 10.** Threshold Voltage vs. Temperature




| Ri (°C/W) | τi (sec) |
|---|---|
| 3.6777 | 0.009926 |
| 21.765 | 25.24029 |
| 25.683 | 3.723179 |
| 11.374 | 0.348001 |

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

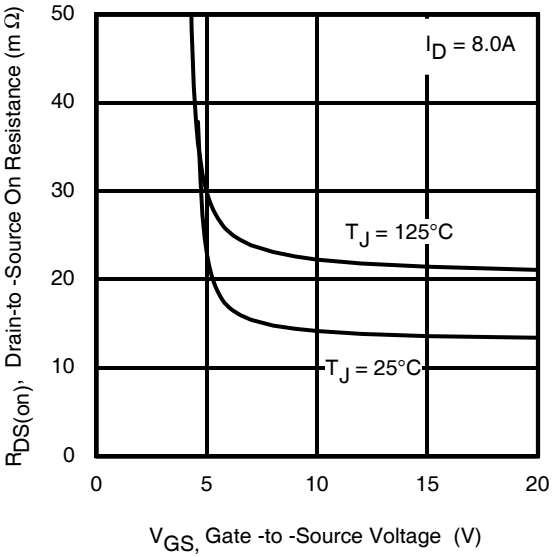



**Fig 12.** On-Resistance vs. Gate Voltage

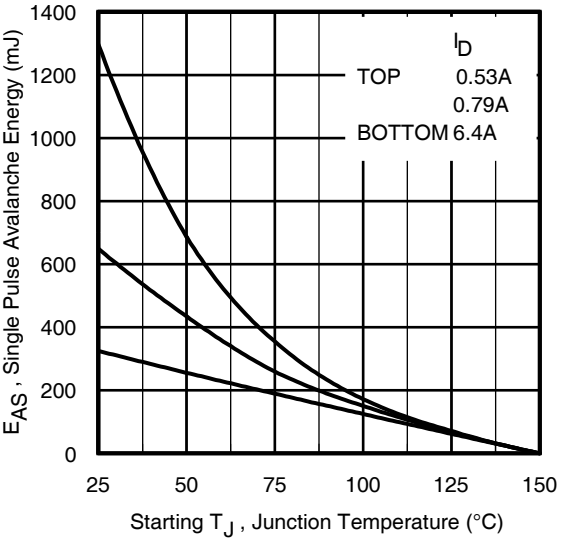



**Fig 13.** Maximum Avalanche Energy vs. Drain Current

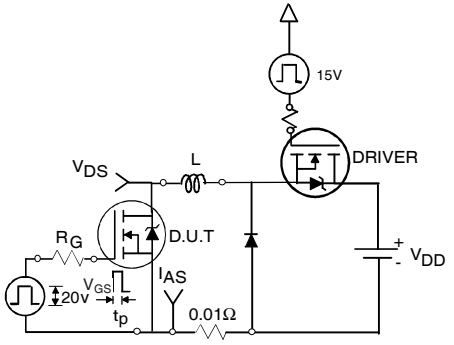



**Fig 14a.** Unclamped Inductive Test Circuit

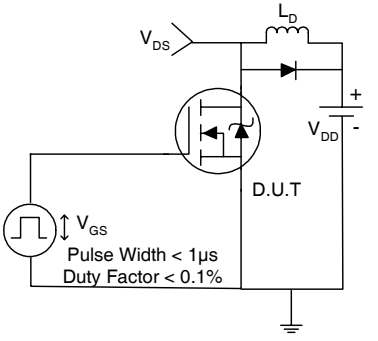



**Fig 15a.** Switching Time Test Circuit

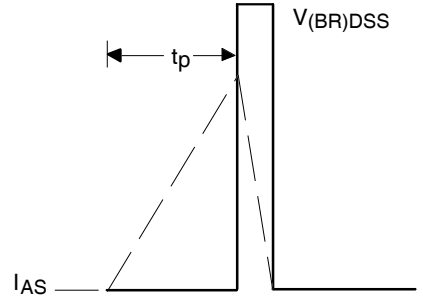



**Fig 14b.** Unclamped Inductive Waveforms

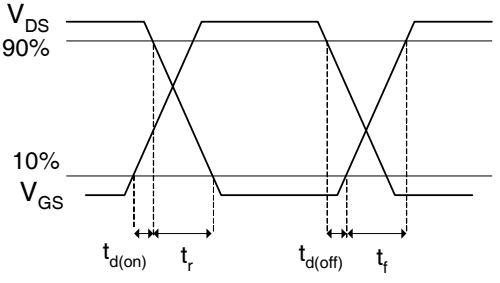



**Fig 15b.** Switching Time Waveforms

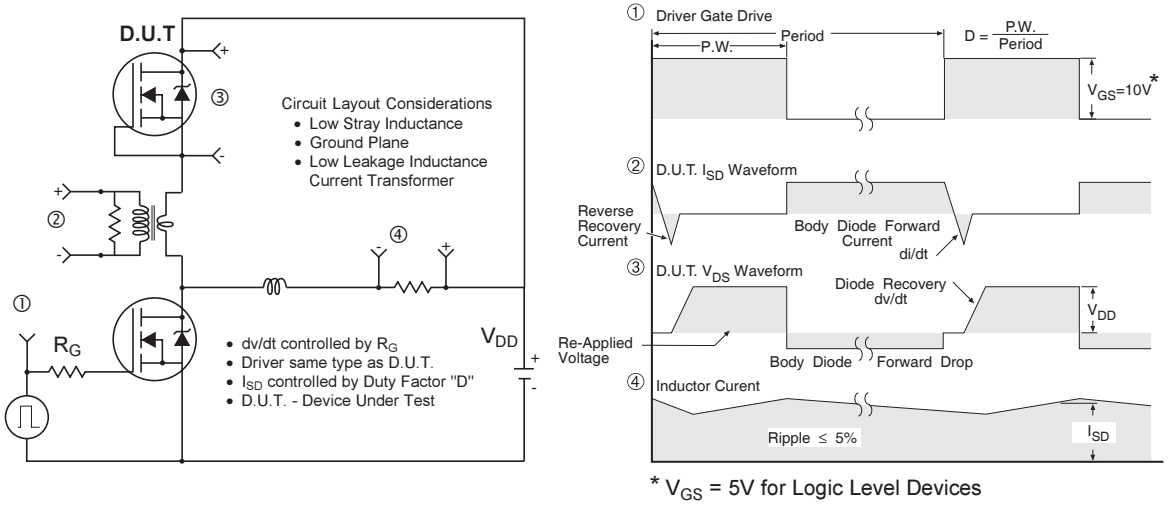



**Fig 16.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

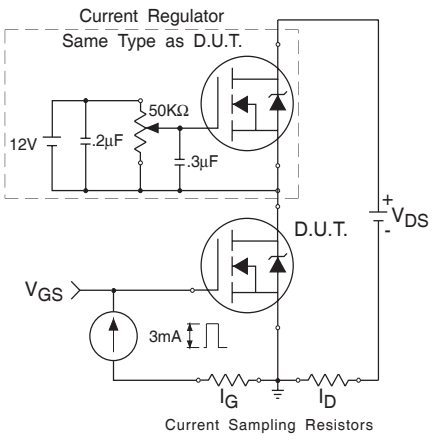



**Fig 17a.** Gate Charge Test Circuit

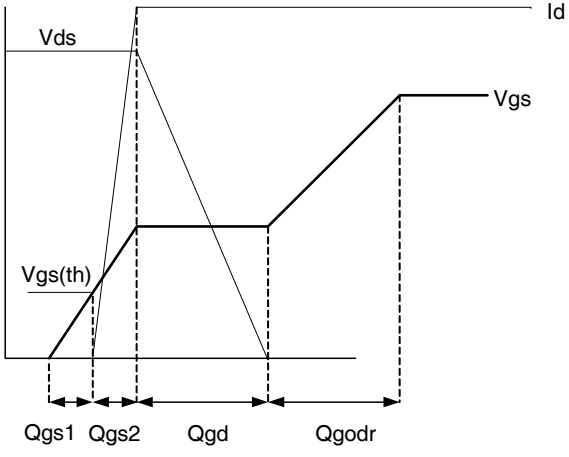



**Fig 17b.** Gate Charge Waveform

## Power MOSFET Selection for Non-Isolated DC/DC Converters

### Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms $Q_{gs2}$ and $Q_{oss}$ which are new to Power MOSFET data sheets.

$Q_{gs2}$ is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, $Q_{gs1}$ and $Q_{gs2}$, can be seen from Fig 16.

$Q_{gs2}$ indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached and the time the drain current rises to $I_{dmax}$ at which time the drain voltage begins to change. Minimizing $Q_{gs2}$ is a critical factor in reducing switching losses in Q1.

$Q_{oss}$ is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure A shows how $Q_{oss}$ is formed by the parallel combination of the voltage dependant (non-linear) capacitance's $C_{ds}$ and $C_{dg}$ when multiplied by the power supply input buss voltage.

### Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P^*_{output}$$

$$P_{loss} = \left(I_{rms}{}^2 \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge $Q_{oss}$ and reverse recovery charge $Q_{rr}$ both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and $V_{in}$. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of $Q_{gd}/Q_{gs1}$ must be minimized to reduce the potential for Cdv/dt turn on.

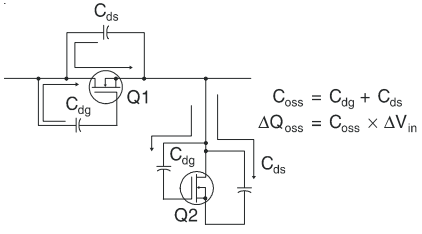
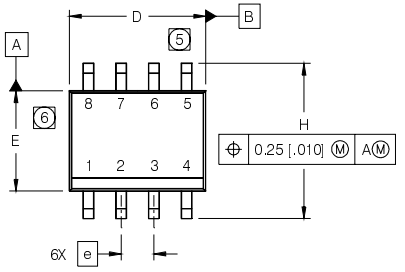


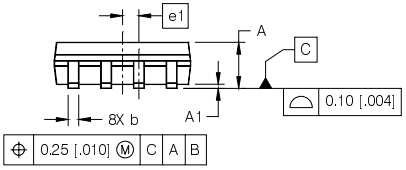

Figure A: $Q_{oss}$ Characteristic

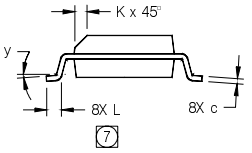
## SO-8 Package Outline (Mosfet & Fetky)

Dimensions are shown in milimeters (inches)




| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |



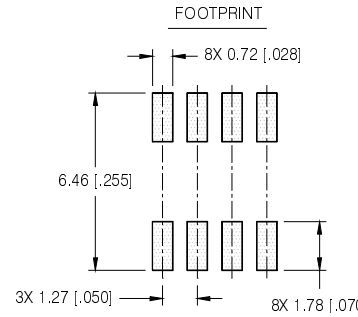

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].

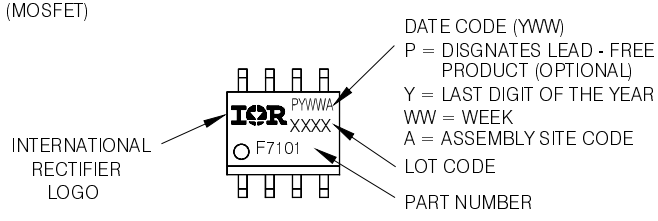
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



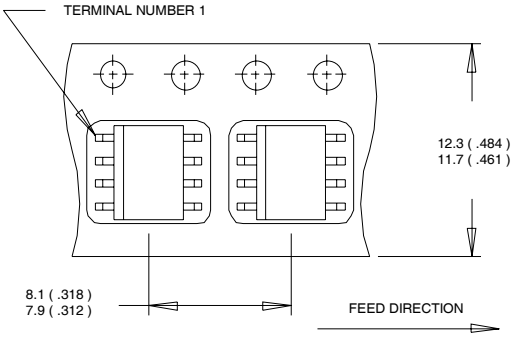

## SO-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

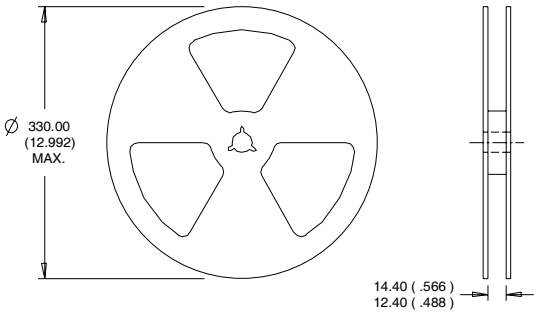



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

## SO-8 Tape and Reel




NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.




NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J$ = 25°C, L = 16mH
$R_G$ = 25Ω, $I_{AS}$ = 6.4A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ When mounted on 1 inch square copper board.

⑤ $R_\theta$ is measured at $T_J$ approximately 90°C.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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Visit us at www.irf.com for sales contact information. 11/09