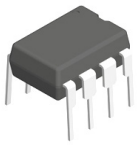
FEATURES

- Output Switch Current In Excess of 1.5A
- 2% Reference Accuracy
- Low Quiescent Current : 2.5mA(Typ.)
- Operating From 3V to 40V
- Frequency Operation to 100KHz
- Active Current Limiting
- Moisture Sensitivity Level 3D
- MC34063AG is Halogen Free Products

SOP-8 PKG



DIP-8 PKG



APPLICATION

- Battery Chargers
- NICs / Switches / Hubs
- ADSL Modems
- Negative Voltage Power Supplies

ORDERING INFORMATION

Device	Package
MC34063AD	SOP-8
MC34063AGD	
MC34063BD	
MC34063AN	DIP-8

DESCRIPTION

The MC34063A/B series is a monolithic control circuit delivering the main functions for DC-DC voltage converting. The device contains an internal temperature compensated reference, comparator, duty cycle controlled oscillator with an active current limit circuit driver and high current output switch.

Output voltage is adjustable through two external resistors with a 2% reference accuracy.

Employing a minimum number of external components the MC34063A/B devices series is designed for Step-Down, Step-Up and Voltage-Inverting applications.

Absolute Maximum Ratings (Note 1)

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Power Supply Voltage	V_{CC}	-	50	V
Comparator Input Voltage Range	V_{IR}	-0.3	40	V
Switch Collector Voltage	V_{SWC}		40	V
Switch Emitter Voltage(V_{SWC}=40V)	V_{SWE}		40	V
Switch Collector to Emitter Voltage	V_{CE}		40	V
Driver Collector Voltage	V_{dc}	-	40	V
Driver Collector Current (Note 2)	I_{dc}	-	100	mA
Switch Current	I_{SW}	-	1.5	A

Absolute Maximum Ratings (Continued)

CHARACTERISTIC		SYMBOL	MIN.	MAX.	UNIT
Power Dissipation (at T_A = 25°C)	SOP-8	PD_{MAX_SOP-8}		1.250	W
	DIP-8	PD_{MAX_DIP-8}		0.625	W
Thermal Resistance	SOP-8	$\theta_{JA-SOP-8}$		100	°C/W
	DIP-8	$\theta_{JA-DIP-8}$		160	°C/W
Operating Junction Temperature Range		T_J	-40	150	°C
Operating Ambient Temperature Range	MC34063A	T_{AOPR}	0	75	°C
	MC34063B		-40	85	°C
Storage Temperature Range		T_{STG}	-65	150	°C

Note 1. Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

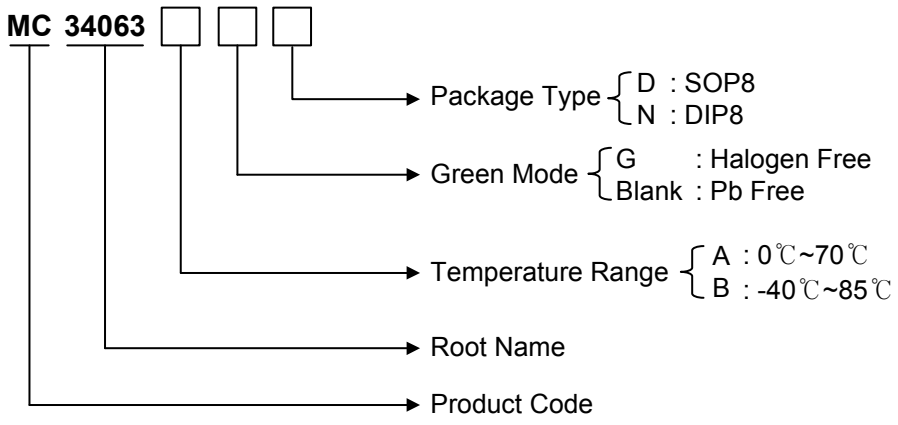
THERMAL DATA

SYMBOL	PARAMETER	DIP-8	SOP-8	UNIT
$R_{THJ-AMB}$	Thermal Resistance Junction-Ambient(*) Max	100	160	℃/W

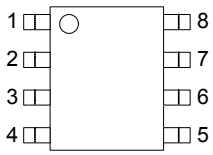
(*) This value depends from thermal design of PCB on which the device is mounted.

Ordering Information

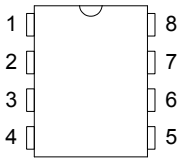
Operating Ambient Temperature(T_{AOPR}) Range	Package	Order No.	Supplied As	Status
0℃~70℃	SOP8	MC34063AD	Reel	Active
0℃~70℃		MC34063AGD	Reel	Contact us
-40℃~85℃		MC34063BD	Reel	Active
0℃~70℃	DIP8	MC34063AN	Tube	Active
-40℃~85℃		MC34063BN	Tube	Active



PIN CONFIGURATION



SOP-8

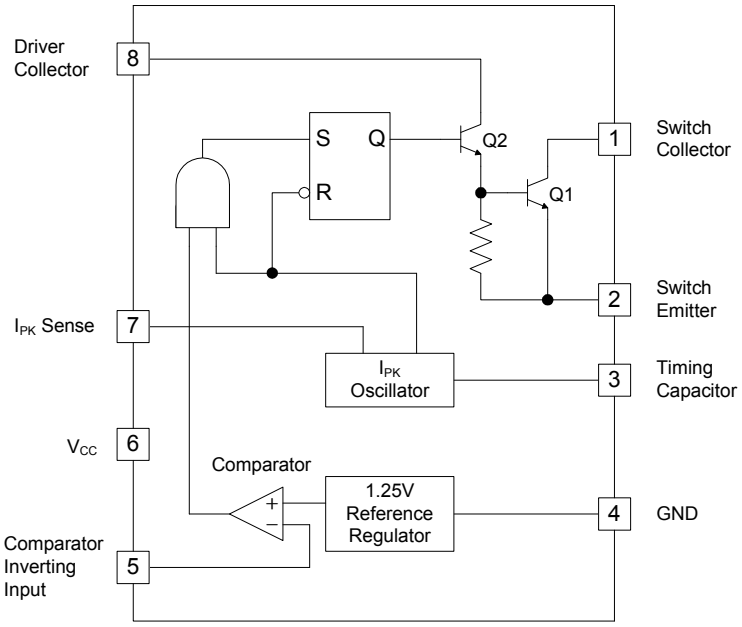


DIP-8

PIN DESCRIPTION

Pin No.	SOP-8 / DIP-8 PKG	
	Name	Function
1	Switch Collector	Internal switch transistor collector
2	Switch Emitter	Internal switch transistor emitter
3	Timing Capacitor	Timing Capacitor to control the switching frequency
4	GND	Ground pin for all internal circuits
5	Comparator Inverting Input	Inverting input pin for internal comparator
6	V_{CC}	Voltage supply
7	I_{PK} Sense	Peak Current Sense Input by monitoring the voltage drop across an external I sense resistor to limit the peak current through the switch
8	Driver Collector	Voltage driver collector

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

(Refer to the test circuits, V_{CC}=5V, T_A=T_{LOW} to T_{HIGH}, unless otherwise specified, see note 2)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
OSCILLATOR						
F_{OSC}	Frequency	V_{PIN5}=0V, C_T=1nF, T_A=25℃	24	33	42	KHz
I_{CHG}	Charge Current	V_{CC}=5 to 40V, T_A=25℃	24	35	42	μA
I_{DISCHG}	Discharge Current	V_{CC}=5 to 40V, T_A=25℃	140	220	260	μA
I_{DISCHG}/I_{CHG}	Discharge to Charge Current Ratio	Pin 7= V_{CC}, T_A=25℃	5.2	6.5	7.5	
$V_{IPK(SENSE)}$	Current Limit Sense Voltage	I_{CHG}=I_{DISCHG}, T_A=25℃	250	300	350	mV
OUTPUT SWITCH						
$V_{CE(SAT)}$	Saturation Voltage, Darlington connection	I_{SW}=1A, Pins 1,8 connected		1.0	1.3	V
$V_{CE(SAT)}$	Saturation Voltage	I_{SW}=1A, R_{PIN8}=82Ω to V_{CC}, Forced β ~ 20		0.45	0.7	V
h_{FE}	DC Current Gain	I_{SW}=1A, V_{CE}=5V, T_A=25℃	50	75		
$I_{C(OFF)}$	Collector Off-State Current	V_{CE}= 40V		0.01	100	μA
COMPARATOR						
V_{TH}	Threshold Voltage	T_A=25℃	1.225	1.25	1.275	V
		T_A=T_{LOW} to T_{HIGH}	1.21		1.29	V
REG_{LINE}	Threshold Voltage Line Regulation	V_{CC}= 3 to 40V		1	5	mV
I_{IB}	Input Bias Current	V_{IN}= 0V		-5	-400	nA
TOTAL DEVICE						
I_{CC}	Supply Current	V_{CC}= 5 to 40V, C_T=1nF Pin7= V_{CC}, V_{PIN5}>V_{TH}, Pin2=GND Remaining pins open for MC34063A/B		1.4	4	mA

Note 1. Maximum package power dissipation limit must be observed.

Note 2. T_{LOW}= '-30℃, T_{HIGH}= '+125℃

Note 3. If Darlington configuration is not used, care must be taken to avoid deep saturation of output switch.
The resulting switch-off time may be adversely affected.
In a Darlington configuration the following output driver condition is suggested:

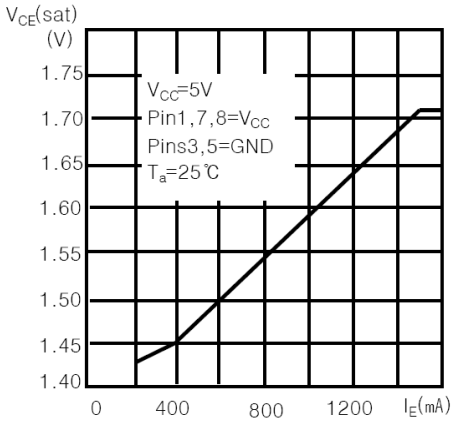
Forced β of output switch : $\frac{I_{C(OUTPUT)}}{I_{C(DRIVER)} - 7.0mA^{*}} \geq 10$

* Currentless due to a built in 1KΩ anti-leakage resistor

TYPICAL ELECTRICAL CHARACTERISTICS

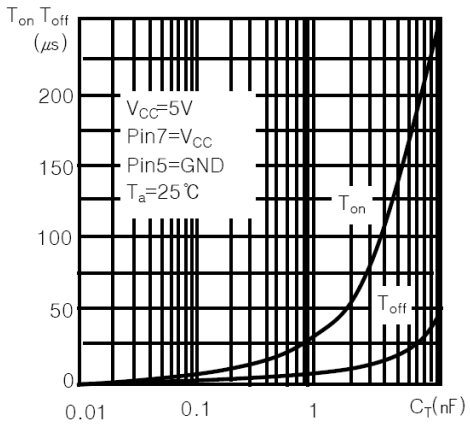
Emitter Follower Configuration Output

Saturation Voltage vs. Emitter Current



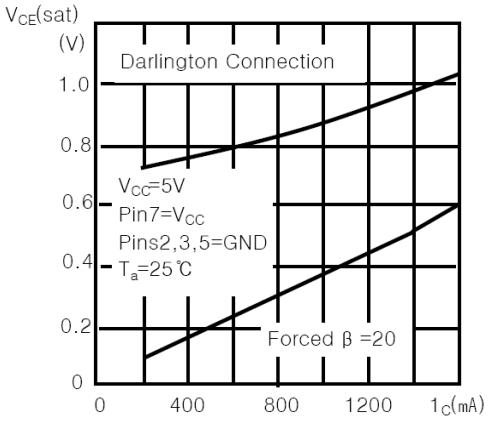
Output Switch ON-OFF Time

vs. Oscillator Timing Capacitor



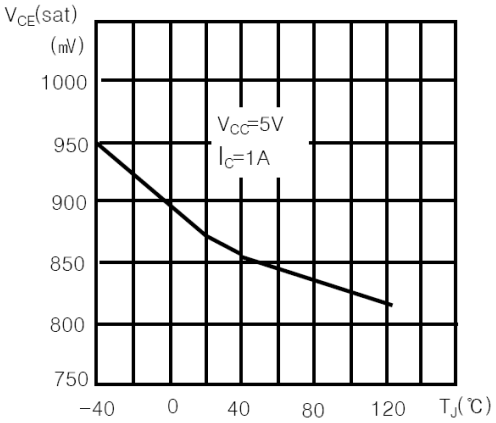
Common Emitter Configuration Output Switch

Saturation Voltage vs. Collector Current



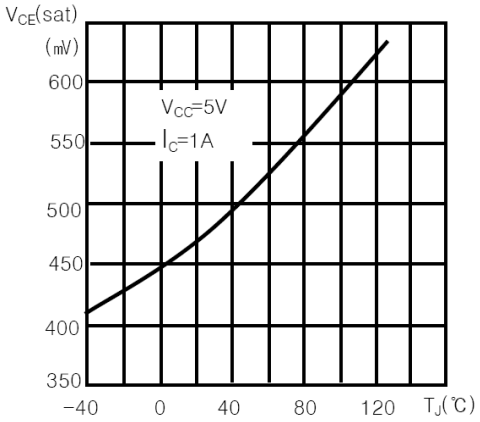
Darlington Configuration Collector Emitter

Saturation Voltage ($V_{CE(SAT)}$) vs. Temperature



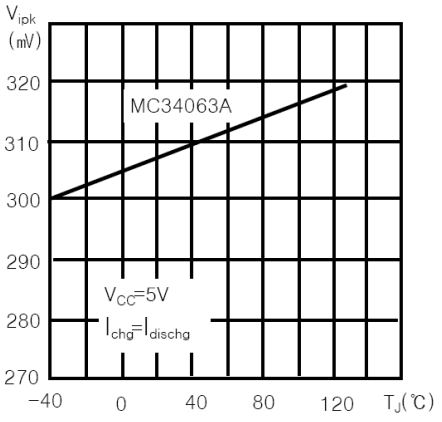
Power Collector Emitter Saturation

Voltage ($V_{CE(SAT)}$) vs, Temperature



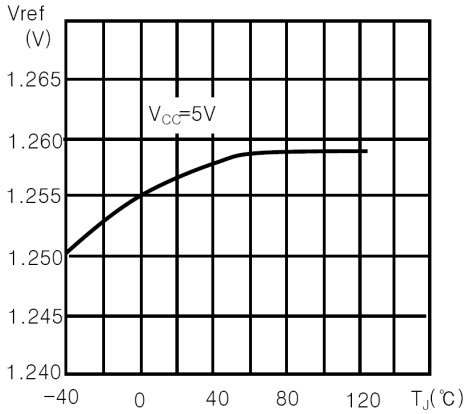
Current Limit Sense Voltage (V_{IPK})

vs. Temperature

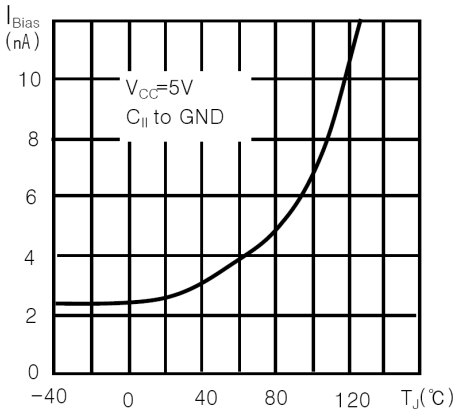


TYPICAL ELECTRICAL CHARACTERISTICS (Continued)

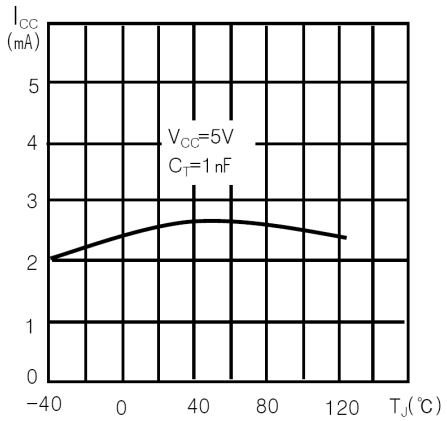
Reference Voltage vs. Temperature



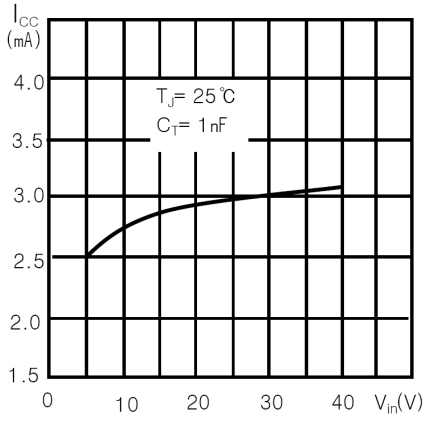
Bias Current vs. Temperature



Supply Current vs. Temperature

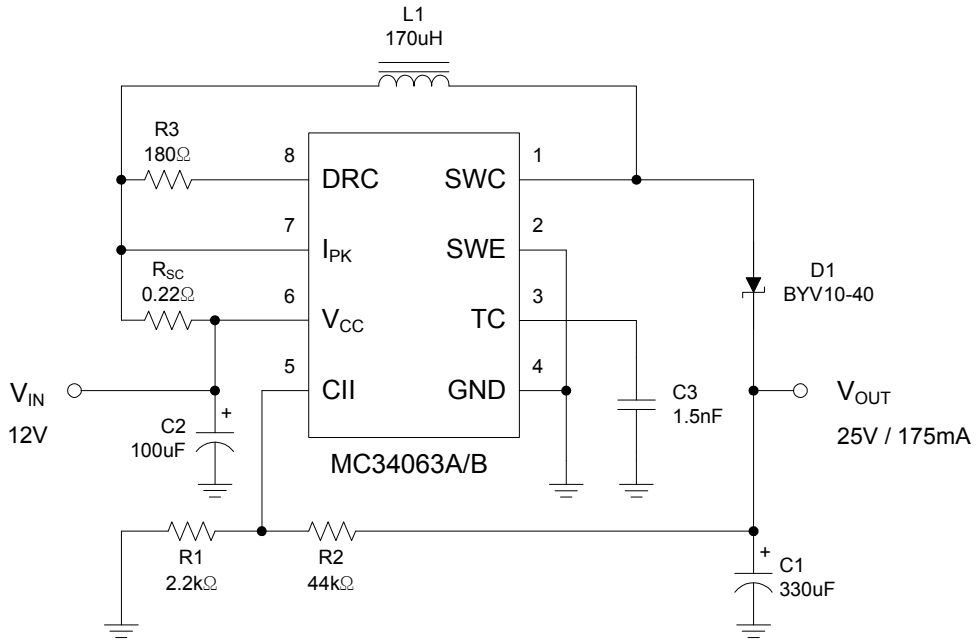


Supply Current vs. Input Voltage

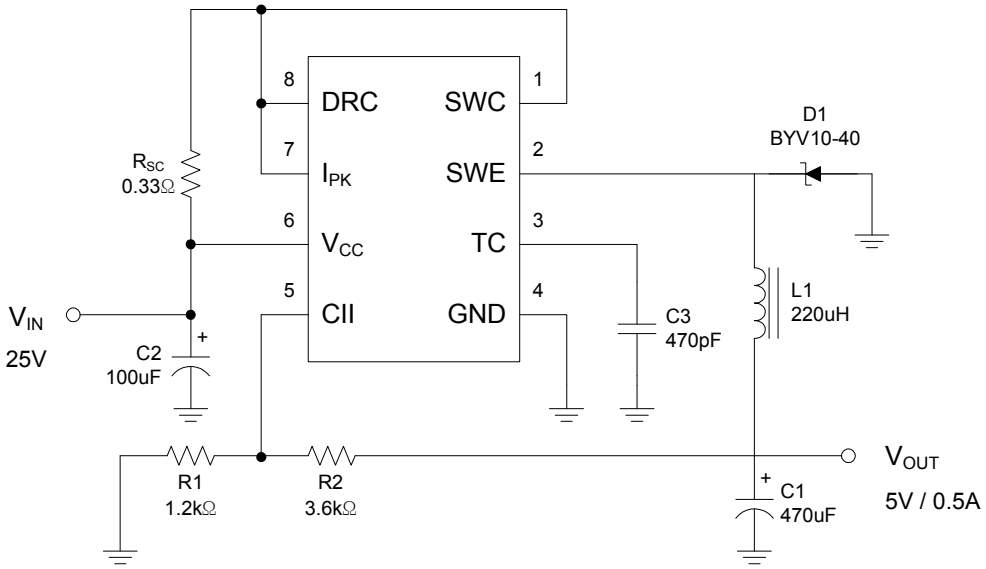


TYPICAL APPLICATION CIRCUIT

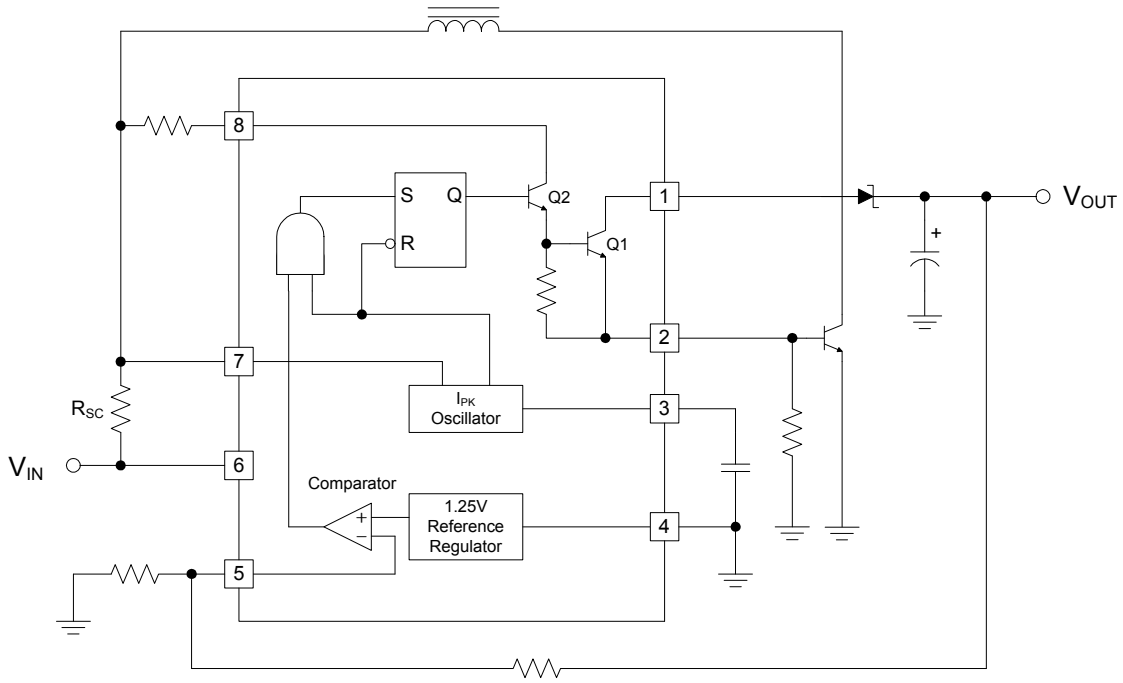
Step-Up Converter



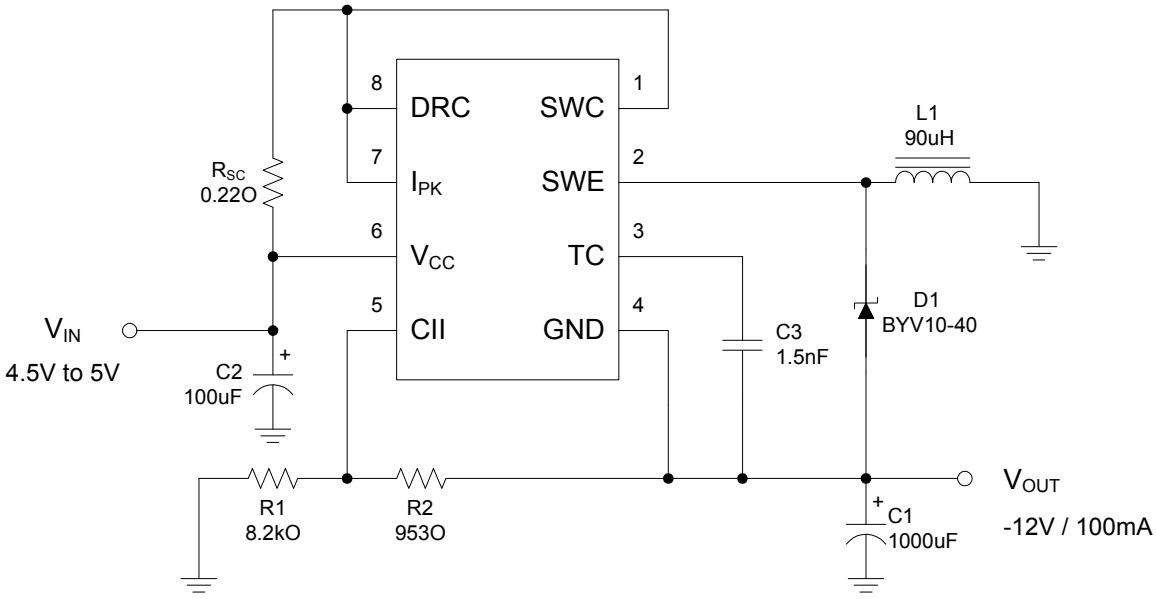
Step-Down Converter



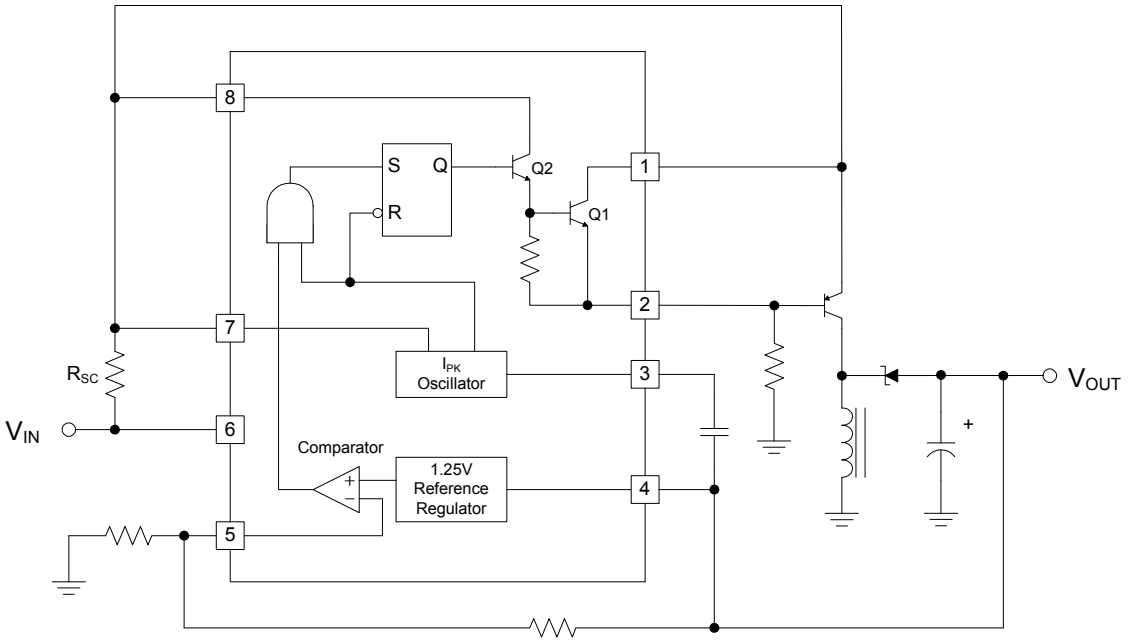
Step-Up with External NPN Switch



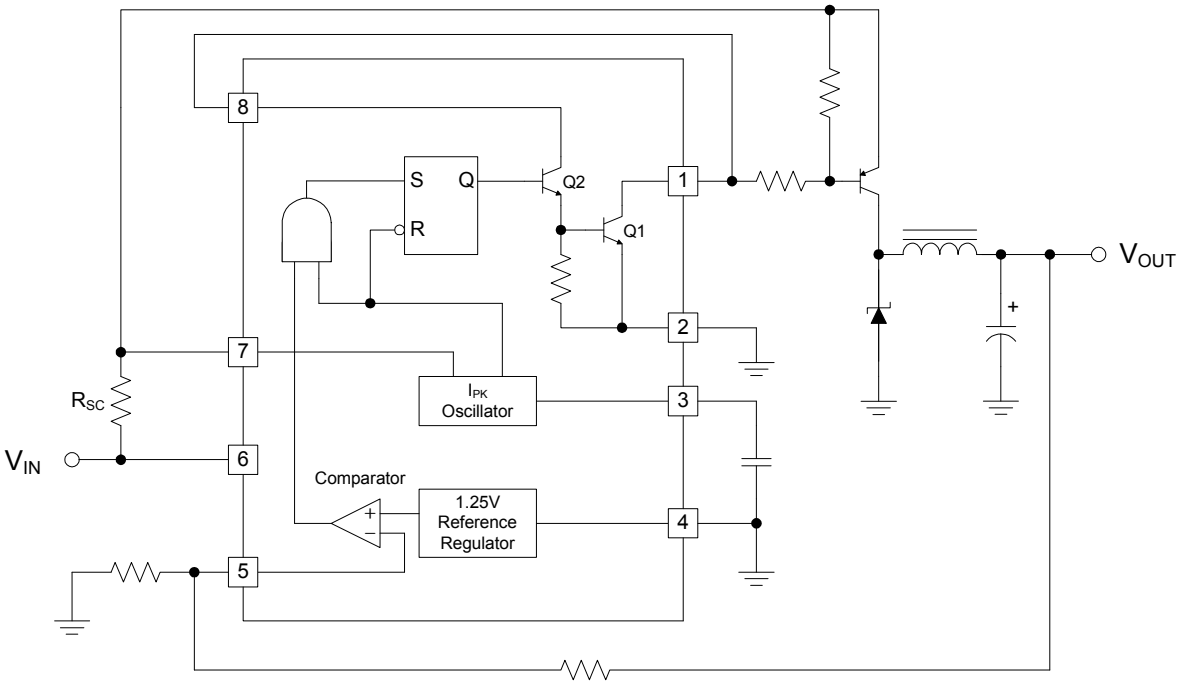
Voltage Inverting Converter



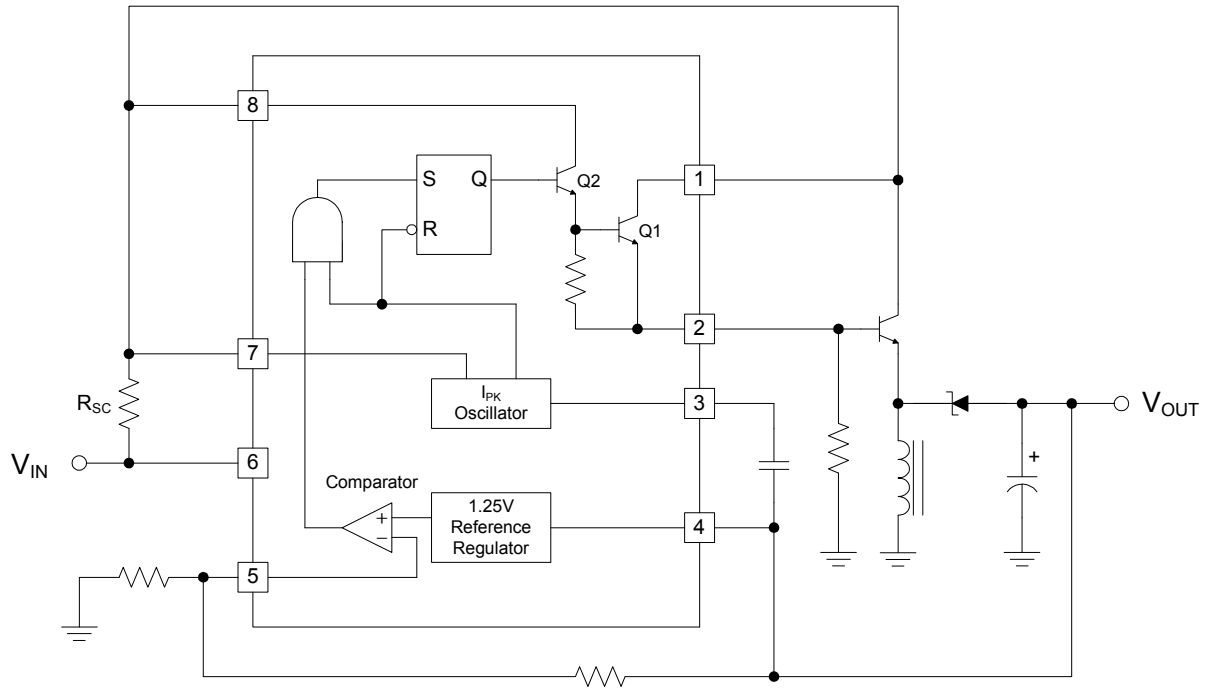
Step-Down with External NPN Switch



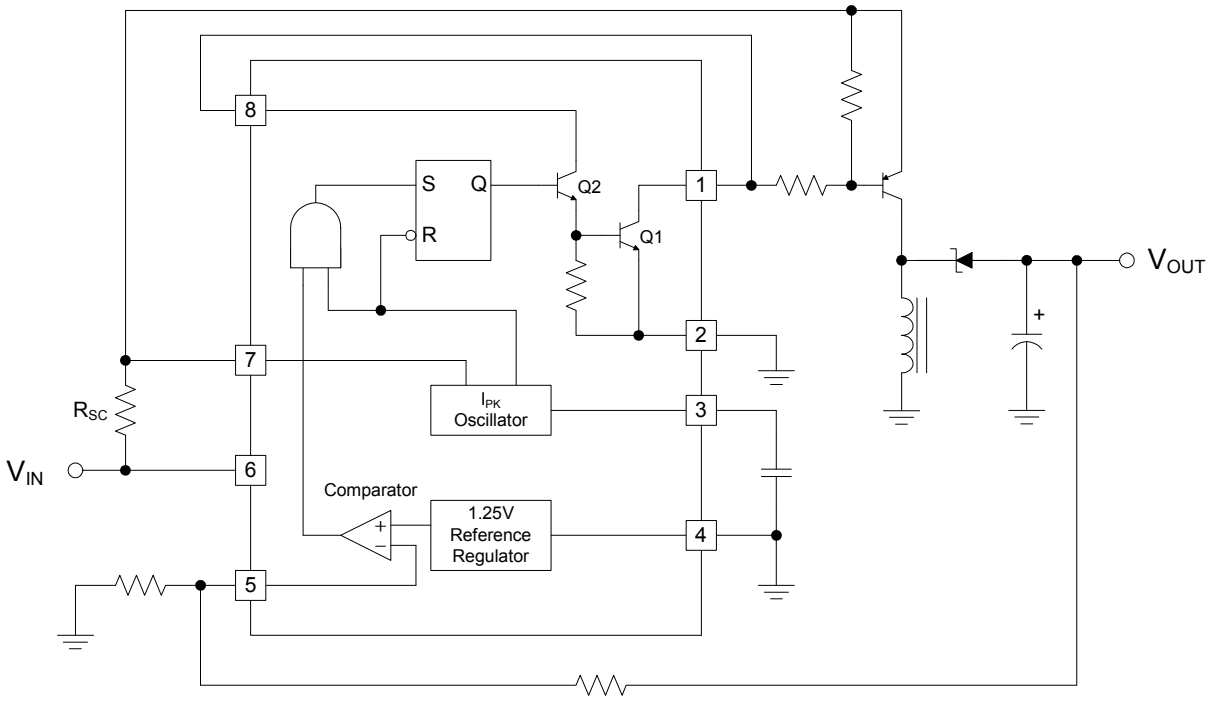
Step-Down with External PNP Switch



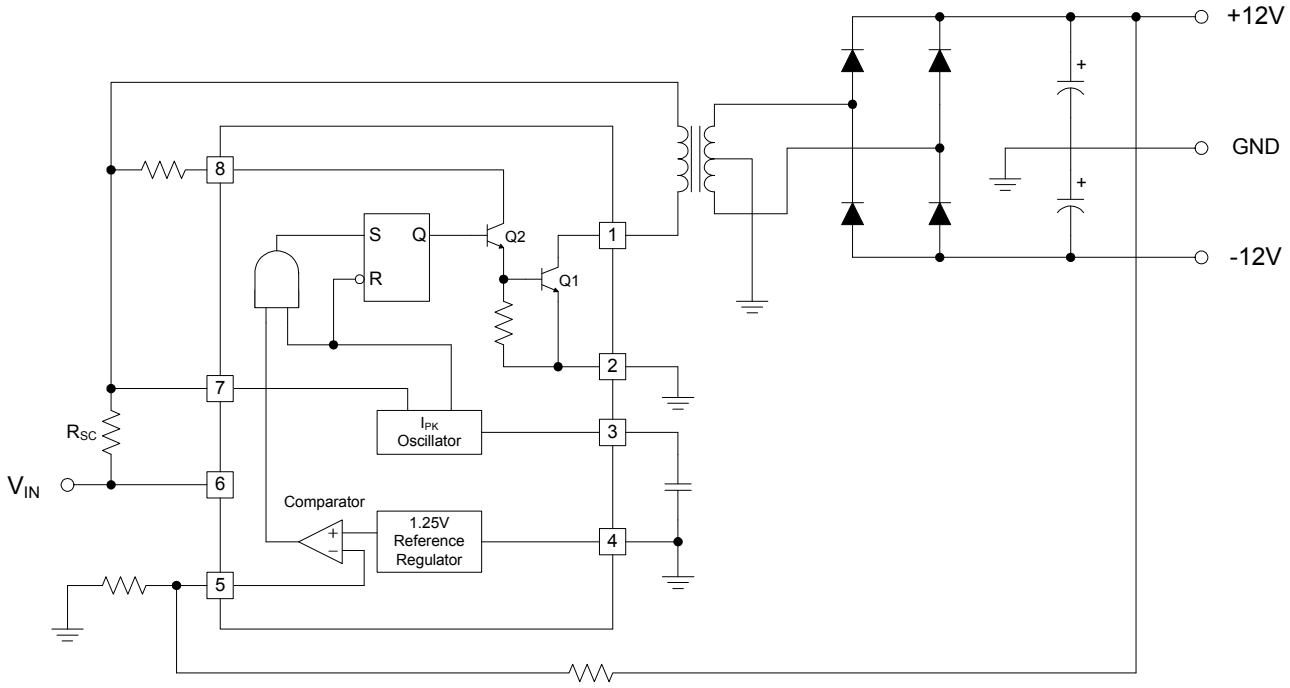
Voltage Inverting with External NPN Switch



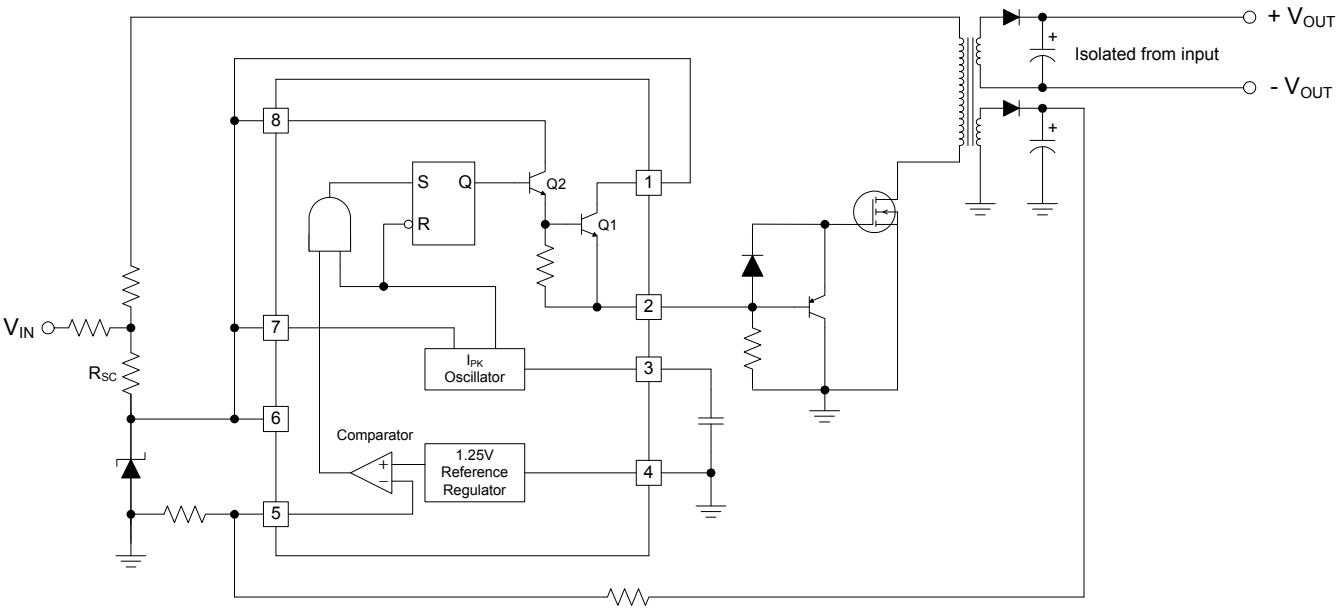
Voltage Inverting with External PNP Saturated Switch



Dual Output Voltage



Higher Output Power, Higher Input Voltage



Design Formula Table

Calculation	Step-UP	Step-Down	Voltage Inverting
t_{on}/t_{off}	$\frac{V_{OUT}+V_F-V_{IN(MIN)}}{V_{IN(MIN)}-V_{SAT}}$	$\frac{V_{OUT}+V_F}{V_{IN(MIN)}-V_{SAT}}$	$\frac{\lvert V_{OUT}\rvert+V_F}{V_{IN}-V_{SAT}}$
$(t_{on}/t_{off})max$	$\frac{1}{f_{MIN}}$	$\frac{1}{f_{MIN}}$	$\frac{1}{f_{MIN}}$
C_T	$4.0\times10^{-5}t_{on}$	$4.0\times10^{-5}t_{on}$	$4.0\times10^{-5}t_{on}$
$I_{PK(SWITCH)}$	$2I_{OUT(MAX)}(\frac{t_{off}}{t_{on}}+1)$	$2I_{OUT(MAX)}$	$2I_{OUT(MAX)}(\frac{t_{off}}{t_{on}}+1)$
R_{SC}	$0.3/I_{PK(SWITCH)}$	$0.3/I_{PK(SWITCH)}$	$0.3/I_{PK(SWITCH)}$
$L_{(MIN)}$	$(\frac{V_{IN(MIN)}-V_{SAT}}{I_{PK(SWITCH)}})\times t_{on(max)}$	$(\frac{V_{IN(MIN)}-V_{SAT}-V_{OUT}}{I_{PK(SWITCH)}})\times t_{on(max)}$	$(\frac{V_{IN(MIN)}-V_{SAT}}{I_{PK(SWITCH)}})\times t_{on(max)}$
C_O	$9\frac{I_{OUT}t_{on}}{V_{RIPPLE(PP)}}$	$\frac{I_{PK(SWITCH)}(t_{on}+t_{off})}{8V_{RIPPLE(PP)}}$	$9\frac{I_{OUT}t_{on}}{V_{RIPPLE(PP)}}$

TERMS AND DEFINITIONS

V_{SAT} - Saturation voltage of the output switch.

VF - Forward voltage drop of the output rectifier.

The following power supply characteristics must be chosen:

V_{IN} - Nominal input voltage.

V_{OUT} - Desired output voltage.

I_{OUT} - Desired output current.

f_{MIN}- Minimum desired output switching frequency at the selected values of V_{IN} and I_O.

$V_{RIPPLE(p-p)}$ – Desired peak-to-peak output ripple voltage. In practice the calculated capacitor value will need to be increased due to its equivalent series resistance and board layout. The ripple voltage should be kept to a low value since it will directly affect the line and load regulation.