Process C3015
CMOS 3μm Digital

Electrical Characteristics

T=25°C Unless otherwise noted

N-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_N	0.6	0.8	1.0	V	100x3μm
Body Factor	γ_N		0.6		$V^{1/2}$	100x3μm
Conduction Factor	β_N	42	47	52	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_N$	2.85	3.2	3.55	μm	100x3μm
Width Encroachment	ΔW_N		0.7		μm	Per side
Punch Through Voltage	$BVDSS_N$	12			V	
Poly Field Threshold Voltage	$VTF_{P(N)}$	12			V	

P-Channel Transistor	Symbol	Minimum	Typical	Maximum	Unit	Comments
Threshold Voltage	VT_P	–0.6	–0.8	–1.0	V	100x3μm
Body Factor	γ_P		0.55		$V^{1/2}$	100x3μm
Conduction Factor	β_P	13	15	19	$\mu A/V^2$	100x100μm
Effective Channel Length	$Leff_P$	2.85	3.2	3.55	μm	100x3μm
Width Encroachment	ΔW_P		0.9		μm	Per side
Punch Through Voltage	$BVDSS_P$	–12			V	
Poly Field Threshold Voltage	$VTF_{P(P)}$	–12			V	

Diffusion & Thin Films	Symbol	Minimum	Typical	Maximum	Unit	Comments
Well (field) Sheet Resistance	$\rho_{P\text{-well(f)}}$	3.2	4.8	6.5	KΩ/□	P-well
N+ Sheet Resistance	ρ_{N+}	16	21	27	Ω/□	
N+ Junction Depth	x_{jN+}		0.8		μm	
P+ Sheet Resistance	ρ_{P+}	50	80	100	Ω/□	
P+ Junction Depth	x_{jP+}		0.7		μm	
Gate Oxide Thickness	T_{GOX}	37.5	40.0	42.5	nm	
Gate Poly Sheet Resistance	ρ_{POLY1}	15	22	30	Ω/□	
Metal-1 Sheet Resistance	ρ_{M1}		30	60	mΩ/□	
Passivation Thickness	T_{PASS}		200+900		nm	oxide+nit.

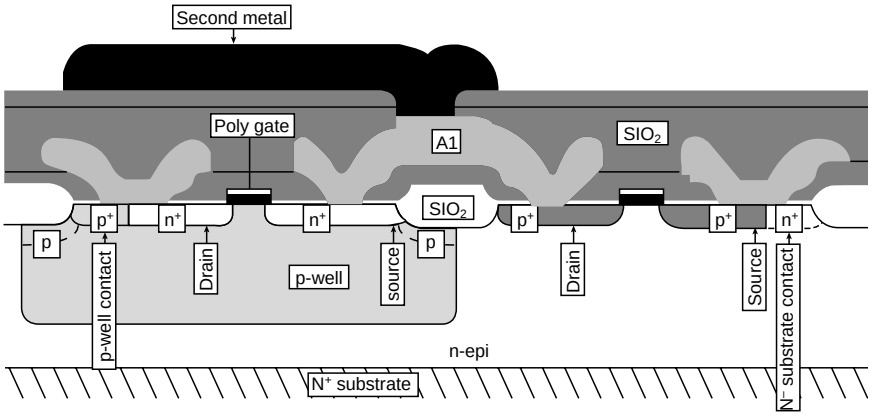
Capacitance	Symbol	Minimum	Typical	Maximum	Unit	Comments
Gate Oxide	C_{OX}	0.66	0.72	0.78	$fF/\mu m^2$	
Metal-1 to Poly-1	C_{M1P}		0.0523		$fF/\mu m^2$	
Metal-1 to Silicon	C_{M1S}	0.026	0.030	0.034	$fF/\mu m^2$	

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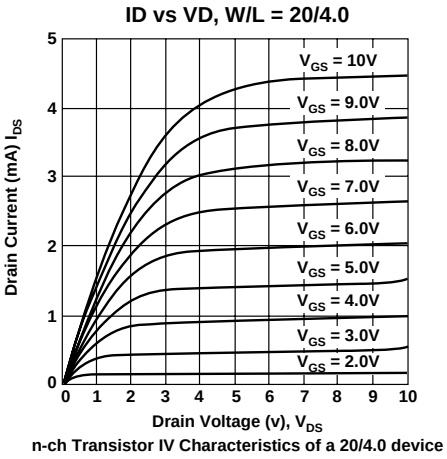
Physical Characteristics

Starting Material	N <100>	N+/P+ Width/Space	3.0 / 3.0µm
Starting Mat. Resistivity	15 - 25 Ω-cm	N+ To P+ Space	12µm
Typ. Operating Voltage	5V	Contact To Poly Space	2.5µm
Well Type	P-well	Contact Overlap Of Diffusion	1.5µm
Metal Layers	1	Contact Overlap Of Poly	1.0µm
Poly Layers	1	Metal-1 Overlap Of Contact	1.0 µm
Contact Size	2.0x2.0µm	Minimum Pad Opening	100x100µm
Metal-1 Width/Space	3.5 / 2.5µm	Minimum Pad-to-Pad Spacing	5.0µm
Gate Poly Width/Space	3.0 / 2.5µm	Minimum Pad Pitch	80.0µm

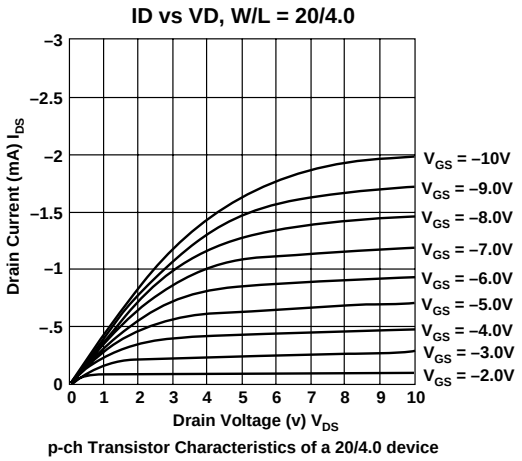
Special Feature of C3015 Process: 3 µm P-well digital process.



Cross-sectional view of the C3015 process



n-ch Transistor IV Characteristics of a 20/4.0 device



p-ch Transistor Characteristics of a 20/4.0 device