P40LF12SLK

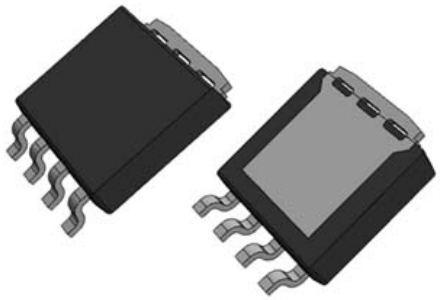
Power MOSFETs
120V, 40A, N-channel

Feature

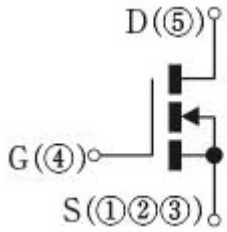
- N-channel
- Small SMD
- Large Current
- Low Ron
- 4.5V Gate Drive
- Low Capacitance
- Based on AEC-Q101
- Halogen free
- Pb free terminal
- RoHS:Yes

OUTLINE

Package (House Name): LF
Package (JEDEC Code): MO-235B similar



Equivalent circuit



Absolute Maximum Ratings (unless otherwise specified : Tc=25°C)

Item	Symbol	Conditions	Ratings	Unit
Storage temperature	Tstg		-55 to 175	°C
Channel tempertature	Tch		-55 to 175	°C
Drain-source voltage	V_{DSS}		120	V
Gate-source voltage	V_{GSS}		±20	V
Continuous drain current(DC)	I_D		40	A
Continuous drain current(Peak)	I_{DP}	Pulse width 10μs, duty=1/100	160	A
Total power dissipation	P_T		217	W
Single avalanche current	I_{AS}	Starting Tch=25°C Tch≦150°C	30	A
Single avalanche energy	E_{AS}	Starting Tch=25°C Tch≦150°C	109	mJ

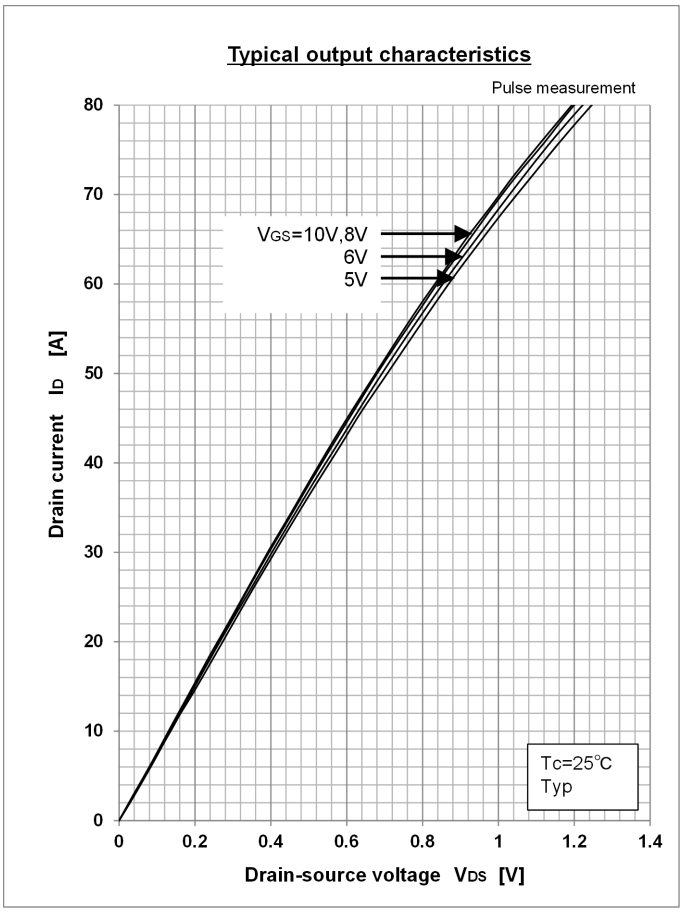
※ :See the original Specifications

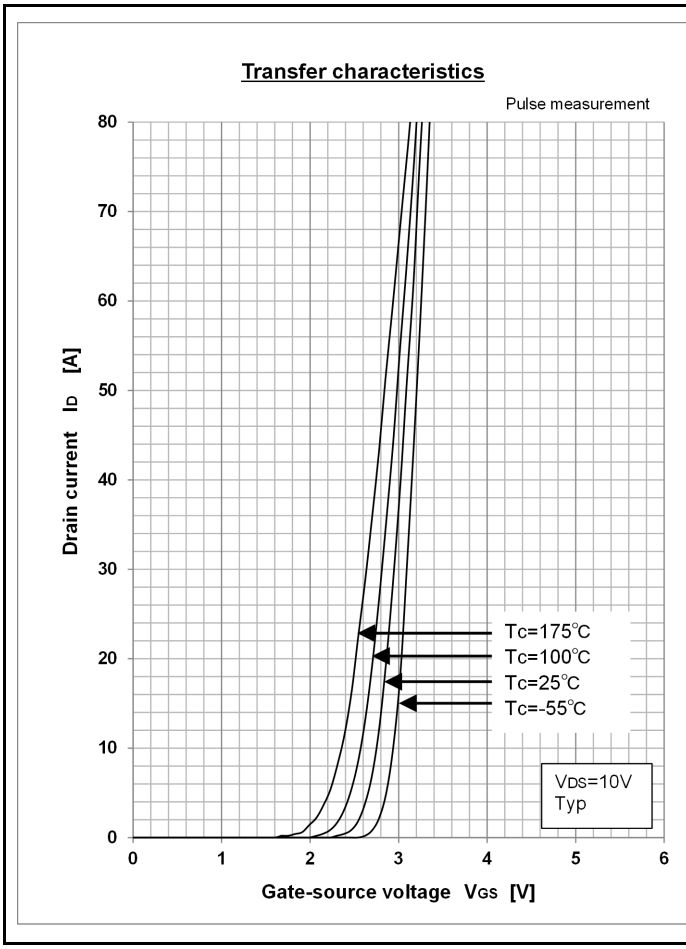
Electrical Characteristics (unless otherwise specified : Tc=25°C)

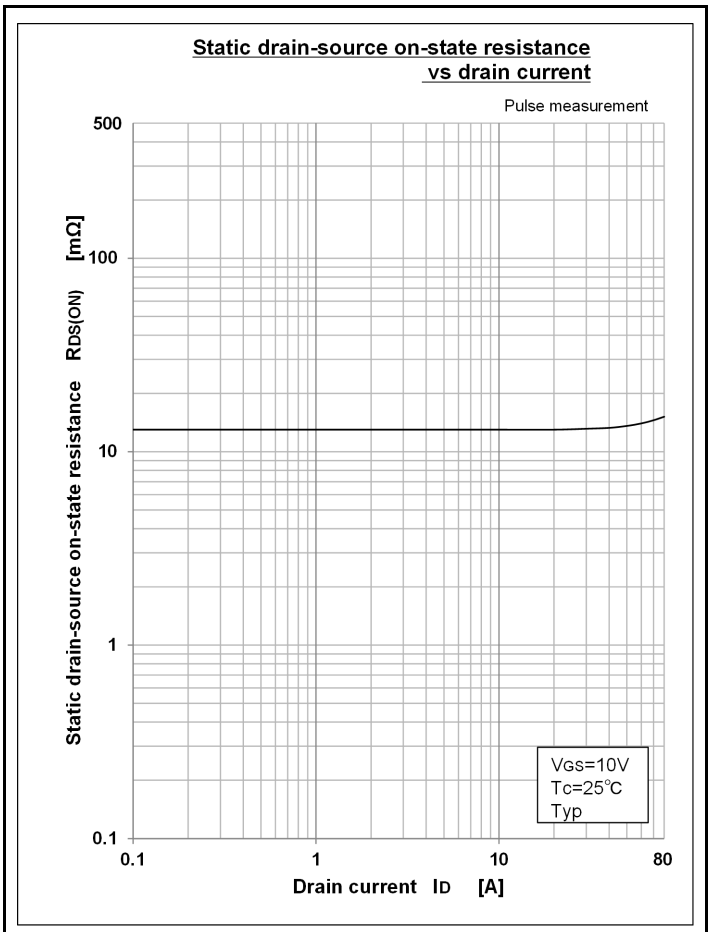
Item	Symbol	Conditions	Ratings			Unit
			MIN	TYP	MAX	
Drain-Source breakdown voltage	$V_{(BR)DSS}$	ID=1mA, VGS=0V	120			V
Zero gate voltage drain current	I_{DSS}	VDS=120V, VGS=0V			1	μA
Gate-source leakage current	I_{GSS}	VGS=±20V, VDS=0V			±0.1	μA
Forward transconductance	g_{fs}	ID=20A, VDS=10V	20			S
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=20A, VGS=10V		0.013	0.0163	Ω
Static drain-source on-state resistance	$R_{DS(ON)}$	ID=20A, VGS=4.5V		0.014	0.0187	Ω
Gate threshold voltage	Vth	ID=1mA, VDS=10V	1.5	2	2.5	V
Source-drain diode forward voltage	V_{SD}	IS=40A, VGS=0V			1.5	V
Thermal resistance	Rth(j-c)	Junction to case, with heatsink			0.69	°C/W
Total gate charge	Qg	VDD=96V, VGS=10V, ID=40A		102		nC
Gate to source charge	Qgs	VDD=96V, VGS=10V, ID=40A		17.5		nC
Gate to drain charge	Qgd	VDD=96V, VGS=10V, ID=40A		27		nC
Input capacitance	Ciss	VDS=25V, VGS=0V, f=1MHz		5000		pF
Reverce transfer capacitnce	Crss	VDS=25V, VGS=0V, f=1MHz		150		pF
Output capacitance	Coss	VDS=25V, VGS=0V, f=1MHz		312		pF
Turn-on delay time	td(on)	ID=20A, RL=3.00Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		5.6		ns
Rise time	tr	ID=20A, RL=3.00Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		8.5		ns
Turn-off delay time	td(off)	ID=20A, RL=3.00Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		106		ns
Fall time	tf	ID=20A, RL=3.00Ω, VDD=60V, Rg=0Ω, VGS(+)=10V, VGS(-)=0V		33		ns
Diode reverse recovery time	trr	IF=40A, VGS=0V, di/dt=100A/μs		63		ns
Diode reverse recovery charge	Qrr	IF=40A, VGS=0V, di/dt=100A/μs		147		nC

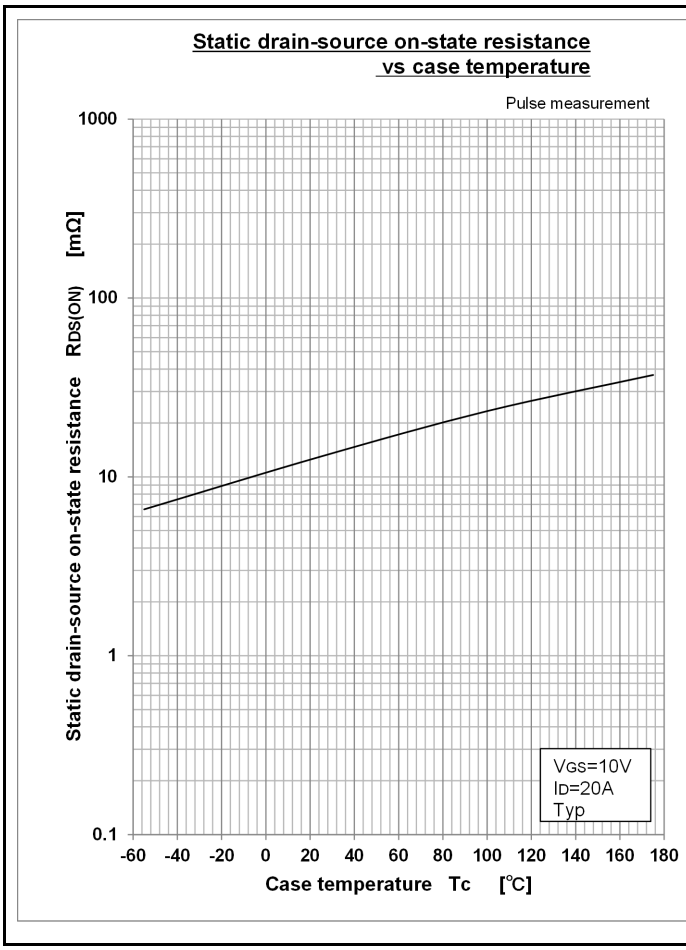
※ ：See the original Specifications

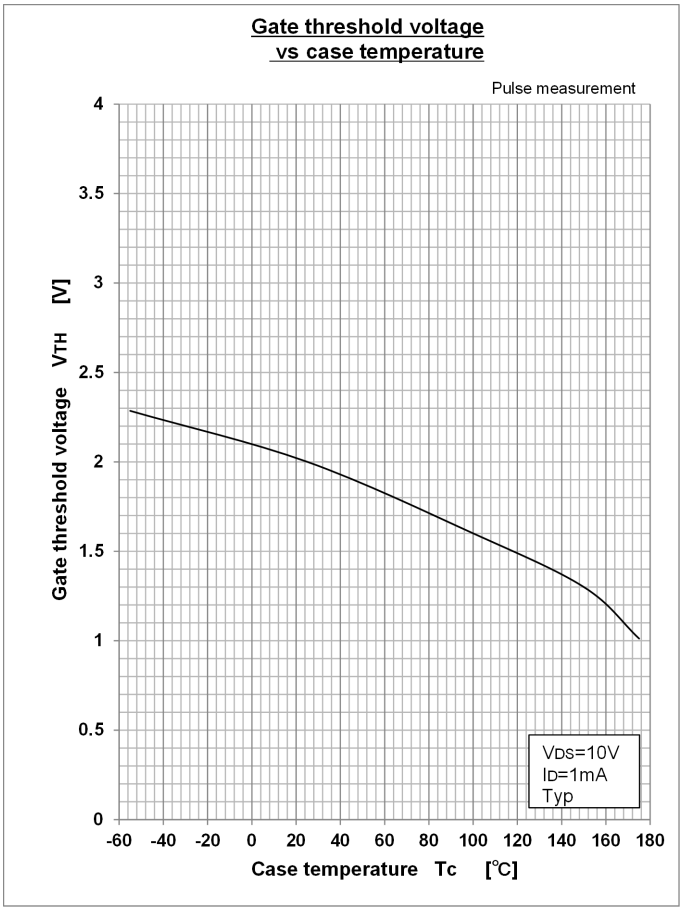
CHARACTERISTIC DIAGRAMS

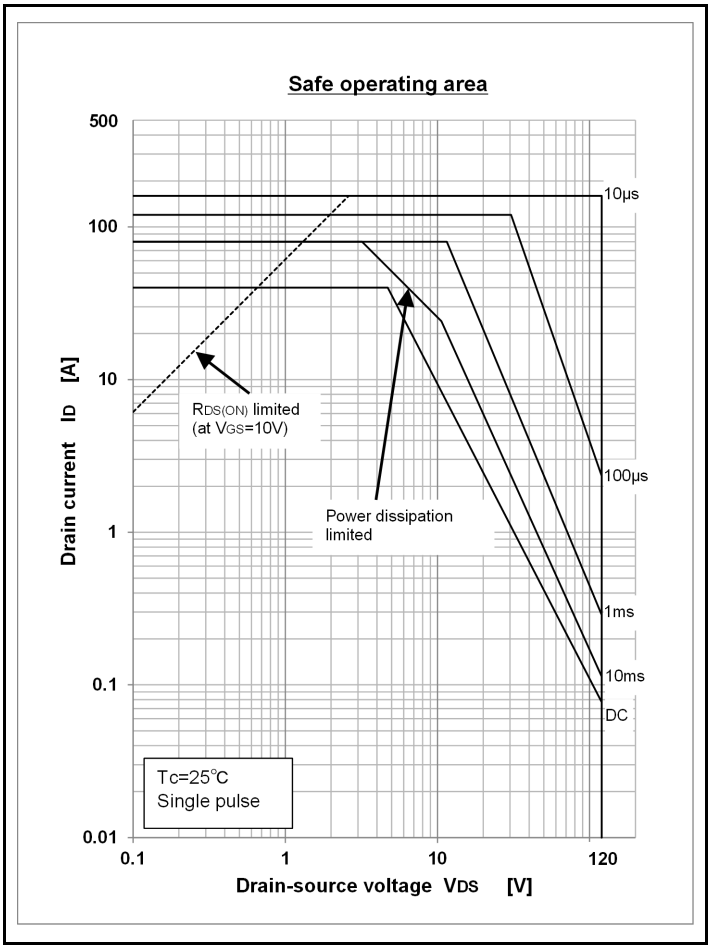


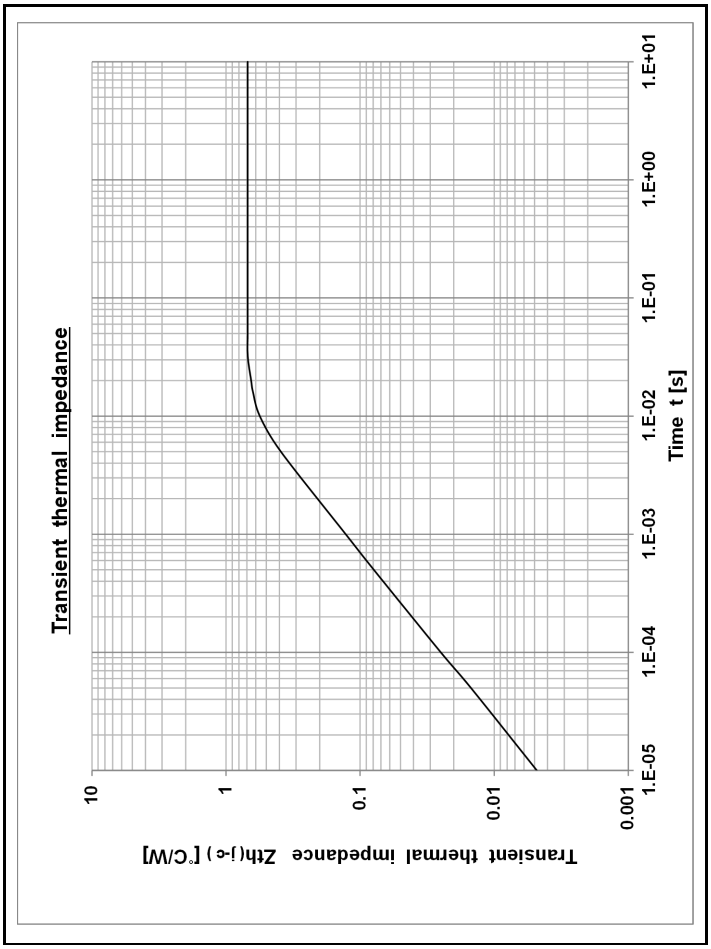


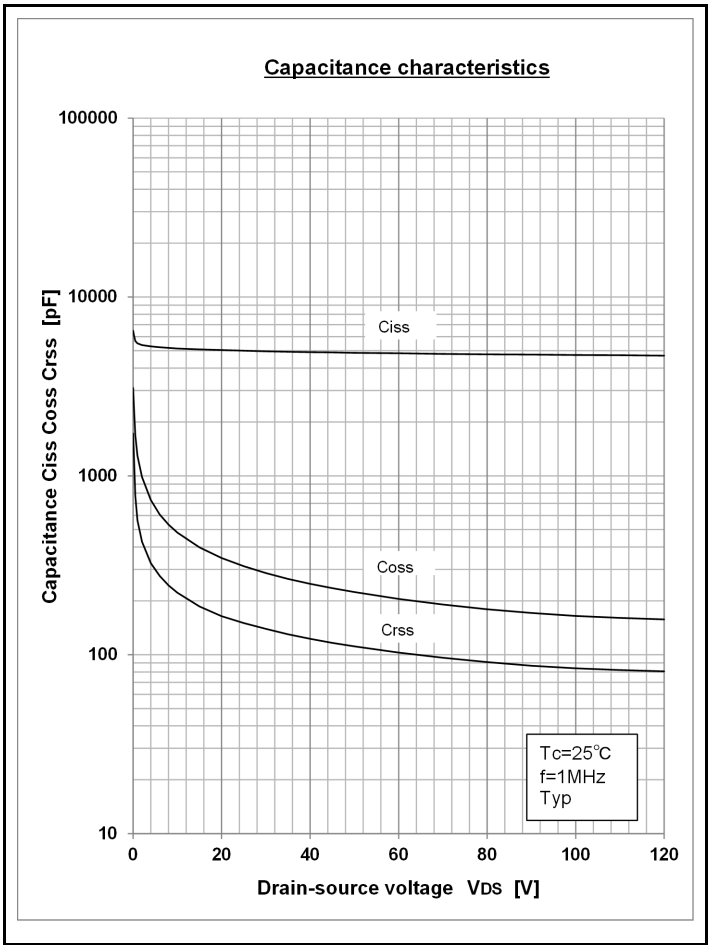


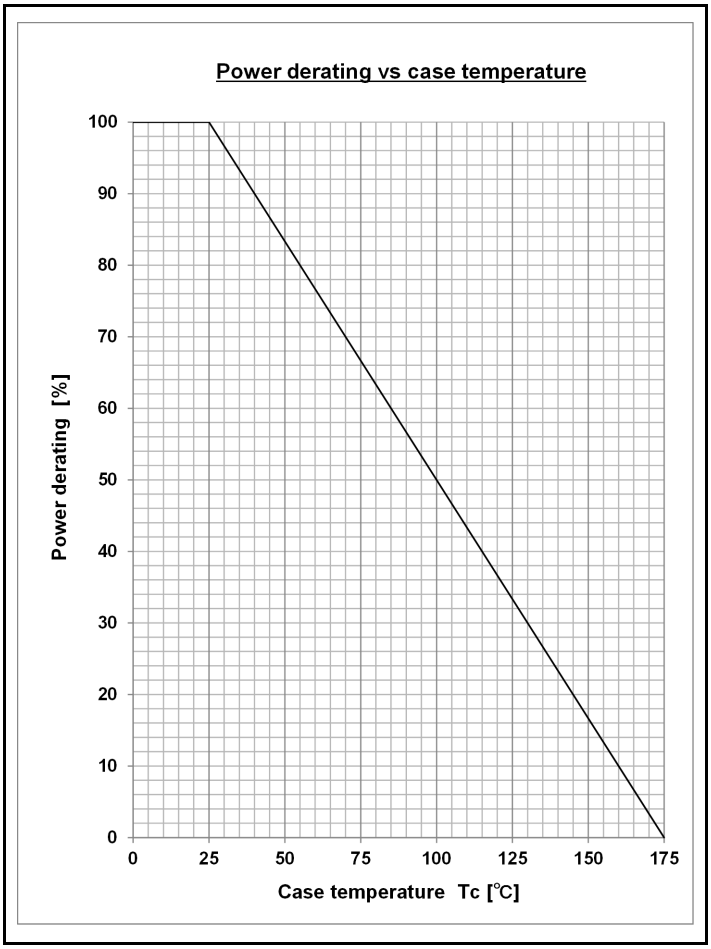


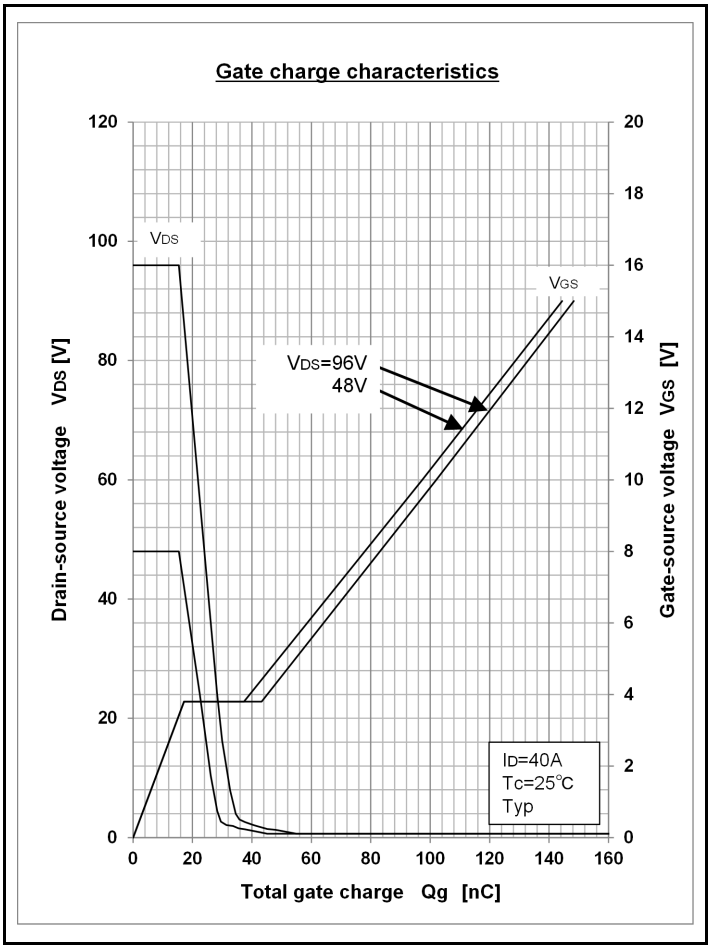

Gate threshold voltage
vs case temperature
Pulse measurement
Gate threshold voltage VTH [V]
Case temperature Tc [℃]
VDS=10V
ID=1mA
Typ

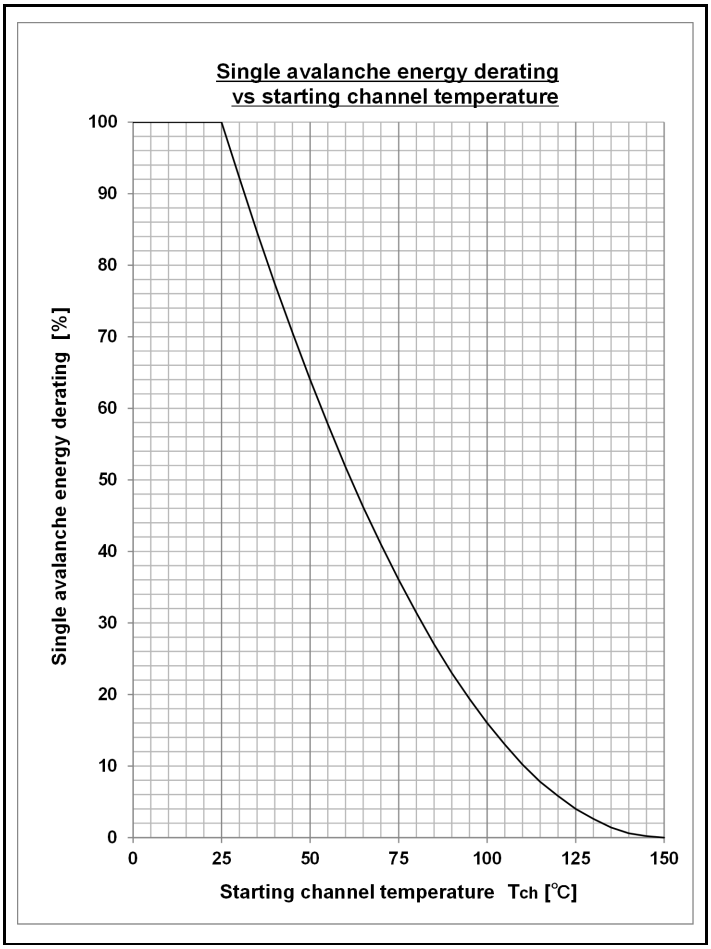

Safe operating area
Drain current ID [A]
Drain-source voltage VDS [V]
10μs
100μs
1ms
10ms
DC
RDS(ON) limited
(at VGS=10V)
Power dissipation
limited
Tc=25℃
Single pulse


Transient thermal impedance
Transient thermal impedance Zth(j-c) [℃/W]
Time t [s]


Capacitance characteristics
Capacitance Ciss Coss Crss [pF]
Drain-source voltage VDS [V]
Ciss
Coss
Crss
Tc=25℃
f=1MHz
Typ


Power derating vs case temperature
Power derating [%]
Case temperature Tc [℃]
0
10
20
30
40
50
60
70
80
90
100
0
25
50
75
100
125
150
175


Gate charge characteristics
Drain-source voltage VDS [V]
Gate-source voltage VGS [V]
Total gate charge Qg [nC]
VDS
VGS
VDS=96V
48V
ID=40A
Tc=25℃
Typ
0
20
40
60
80
100
120
0
2
4
6
8
10
12
14
16
18
20
0
20
40
60
80
100
120
140
160

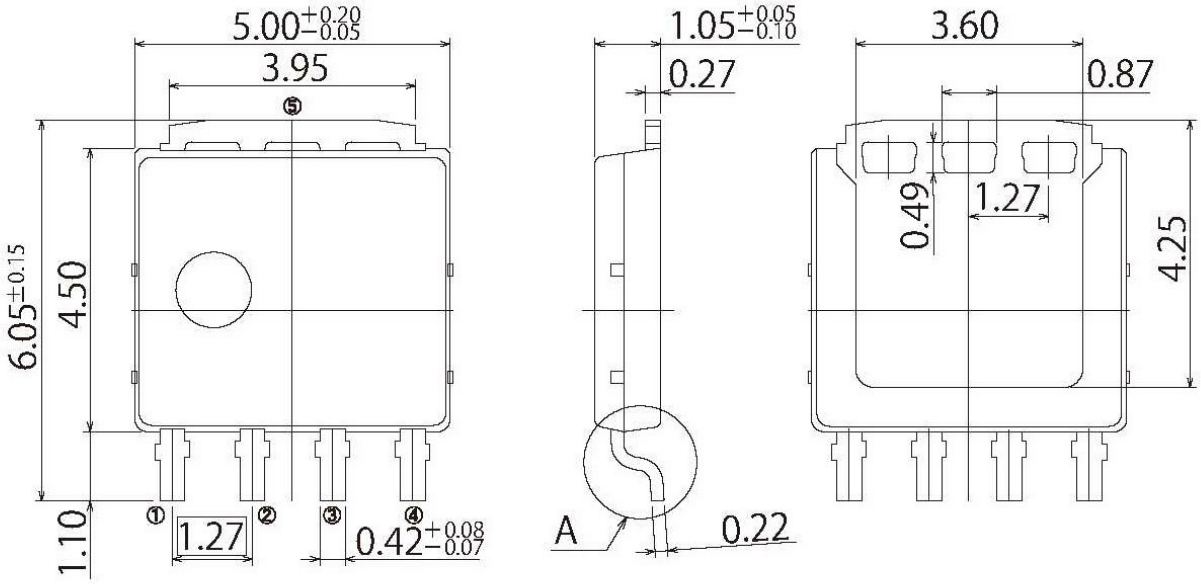

Single avalanche energy derating
vs starting channel temperature
Single avalanche energy derating [%]
Starting channel temperature Tch [℃]
0
10
20
30
40
50
60
70
80
90
100
0
25
50
75
100
125
150

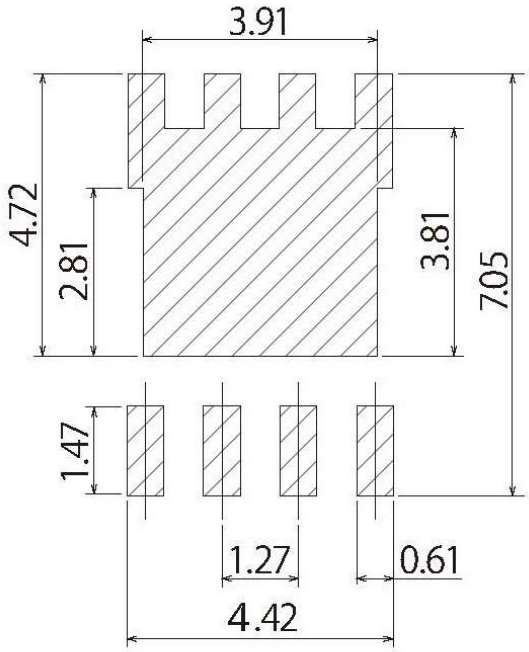
Outline Dimensions

unit:mm

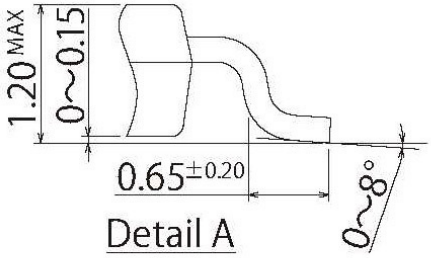
G7

JEDEC Code	MO-235B similar
JEITA Code	–
House Name	LF





Referential Soldering Pad



Detail A

・Optimize soldering pad to the board design and soldering condition.

Notes

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