iC-LTA

6-CH. INCREMENTAL OPTO ENCODER ARRAY

preliminary

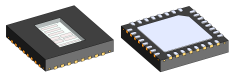
FEATURES

- Monolithic photodiode array with excellent signal matching
- Very compact size for small encoders
- Moderate track pitch for relaxed assembly tolerances
- Low noise signal amplifiers with high EMI tolerance
- Single-pin programming of 3 operating modes: analog, digital, and x2 interpolated
- Analog signals for alignment and resolution enhancement
- Selectable index gating: 1 T, 0.5 T (B-gated), 0.25 T (AB-gated)
- Complementary outputs: A, B, Z and NA, NB, NZ
- High output frequency for speedy drives and high resolution
- U, V, W commutation signals, analog and digital
- All outputs +/- 4 mA push-pull, current-limited and short-circuit-proof
- LED power control with 40 mA high-side driver
- Single 3.5 V to 5.5 V operation, low power consumption
- Operating temperature range of -40 °C to +110 °C (+120 °C)
- Space saving optoQFN / optoBGA packages (RoHS compliant)
- Custom made code disc and reticle designs on request

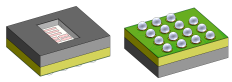
APPLICATIONS

- Incremental encoder
- Brushless DC motor commutation
- Industrial drives

PACKAGES

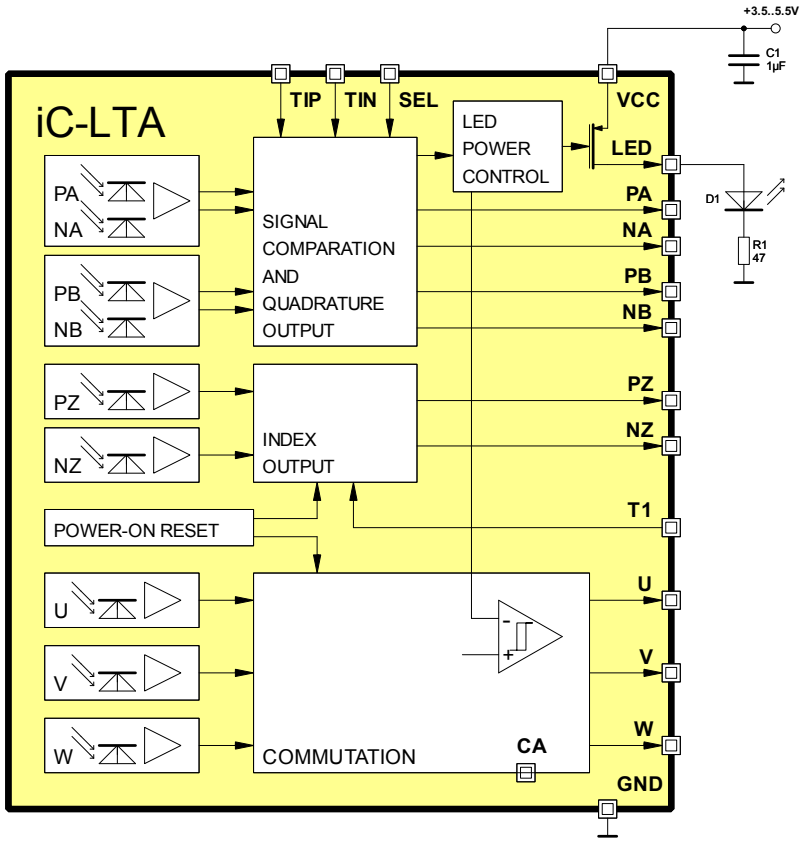


32-pin optoQFN
5 mm x 5 mm x 0.9 mm



15-pin optoBGA
6.2 mm x 5.2 mm x 1.7 mm

BLOCK DIAGRAM



DESCRIPTION

iC-LTA is a versatile optical sensor IC with integrated photosensors whose signals are converted into voltages by low-noise transimpedance amplifiers. Precise voltage comparators with hysteresis are used to generate the digital signals, supplied to the output pins via differential +/- 4 mA push-pull drivers.

The built-in LED power control with its 40 mA driver stage permits a direct connection of the encoder LED. Regardless of aging or changes in temperature the received optical power is kept constant.

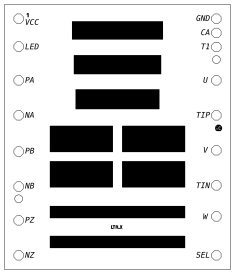
Selection input SEL chooses for three different operating modes: regular A/B operation, A/B operation with 2-fold interpolation, or analog operation. With analog operation the amplified signal voltages are available at the outputs for inspection and monitoring encoder assembly.

The typical application of iC-LTA are incremental encoders for motor feedback and commutation. To this end, iC-LTA provides a differential scanning for the A/B track and the index track Z. The layout of the signal amplifiers is such that there is an excellent paired channel matching, eliminating the needs for signal calibration.

Additionally, three more tracks are provided to generate motor commutation information for the U, V and W outputs, for instance with 120 degree phase shift to operate 3-phase brushless motors (period count and phase shift can be varied by the code disc applied).

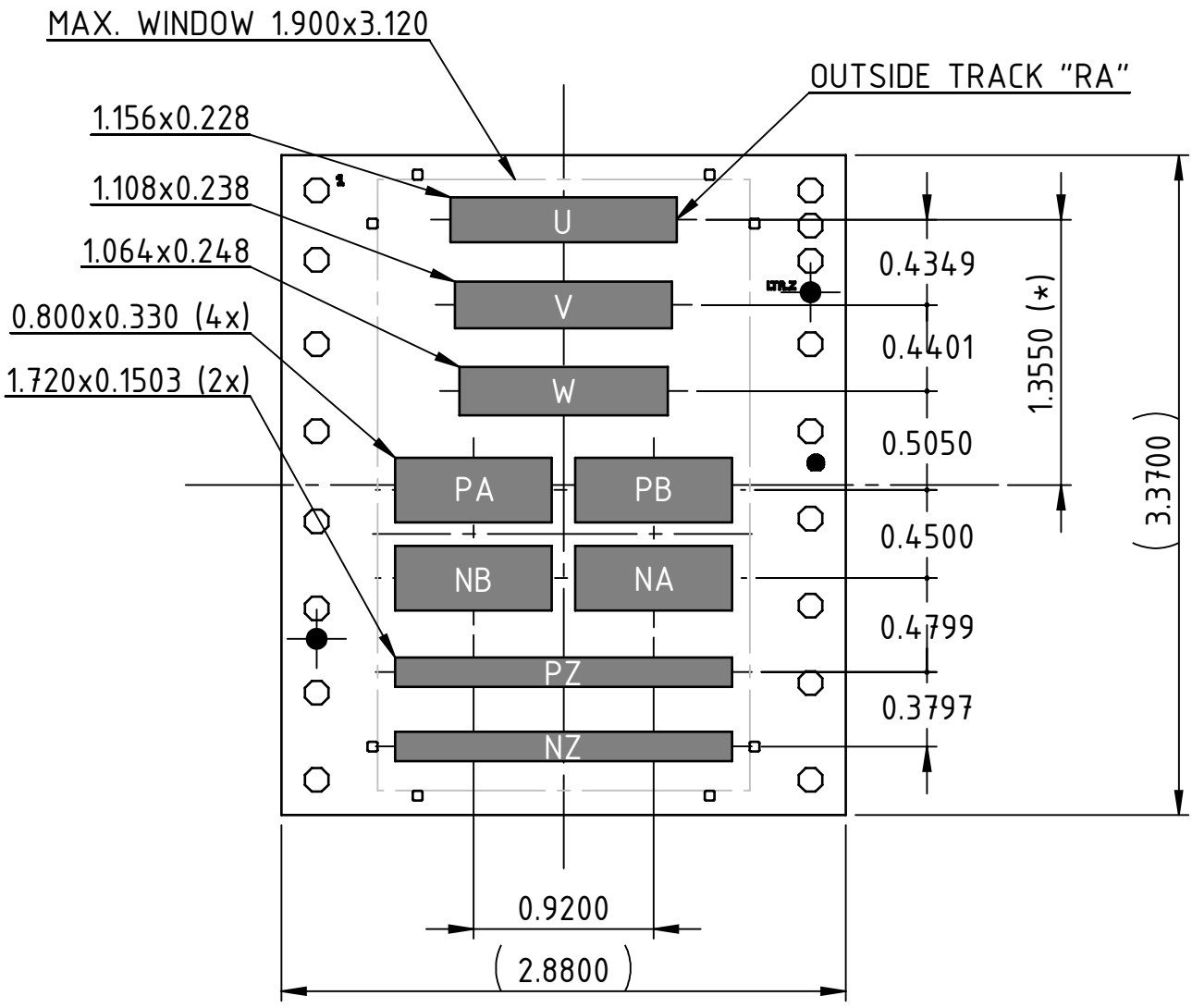
PACKAGING INFORMATION

PAD LAYOUT
Chip size 2.88 mm x 3.37 mm

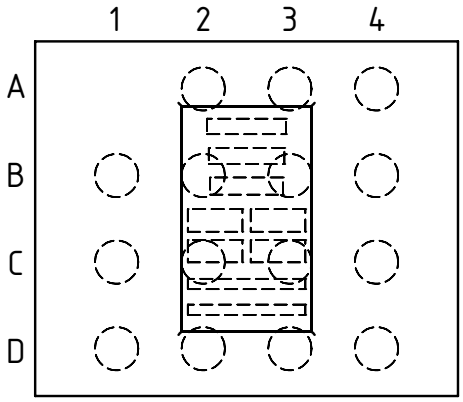


PAD FUNCTIONS

No.	Name	Function
		See pin configuration.



PIN CONFIGURATION
oBGA LSH2C (6.2 mm x 5.2 mm)

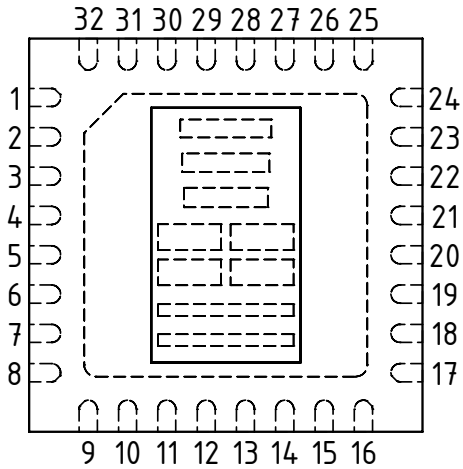


PIN FUNCTIONS

No.	Name	Function
A2	VCC	+3.5..5.5 V Supply Voltage
A3	LED	LED Controller, High-Side Current Source Output
A4	GND	Ground
B1	PA	Push-Pull Output A+ (Sin+)
B2	NA	Push-Pull Output A- (Sin-)
B3	TIP	Positive Test Current Input
B4	U	Push-Pull Output U
C1	PB	Push-Pull Output B+ (Cos+)
C2	NB	Push-Pull Output B- (Cos-)
C3	TIN	Negative Test Current Input
C4	V	Push-Pull Output V
D1	PZ	Push-Pull Output Z+ (Index+)
D2	NZ	Push-Pull Output Z- (Index-)
D3	SEL	Op. Mode Selection Input: lo = digital, hi = x2 interpolated open = analog (alignment)
D4	W	Push-Pull Output W

For dimensional specifications refer to the relevant package data sheet, available separately.

PIN CONFIGURATION
oQFN32-5x5 (5 mm x 5 mm)



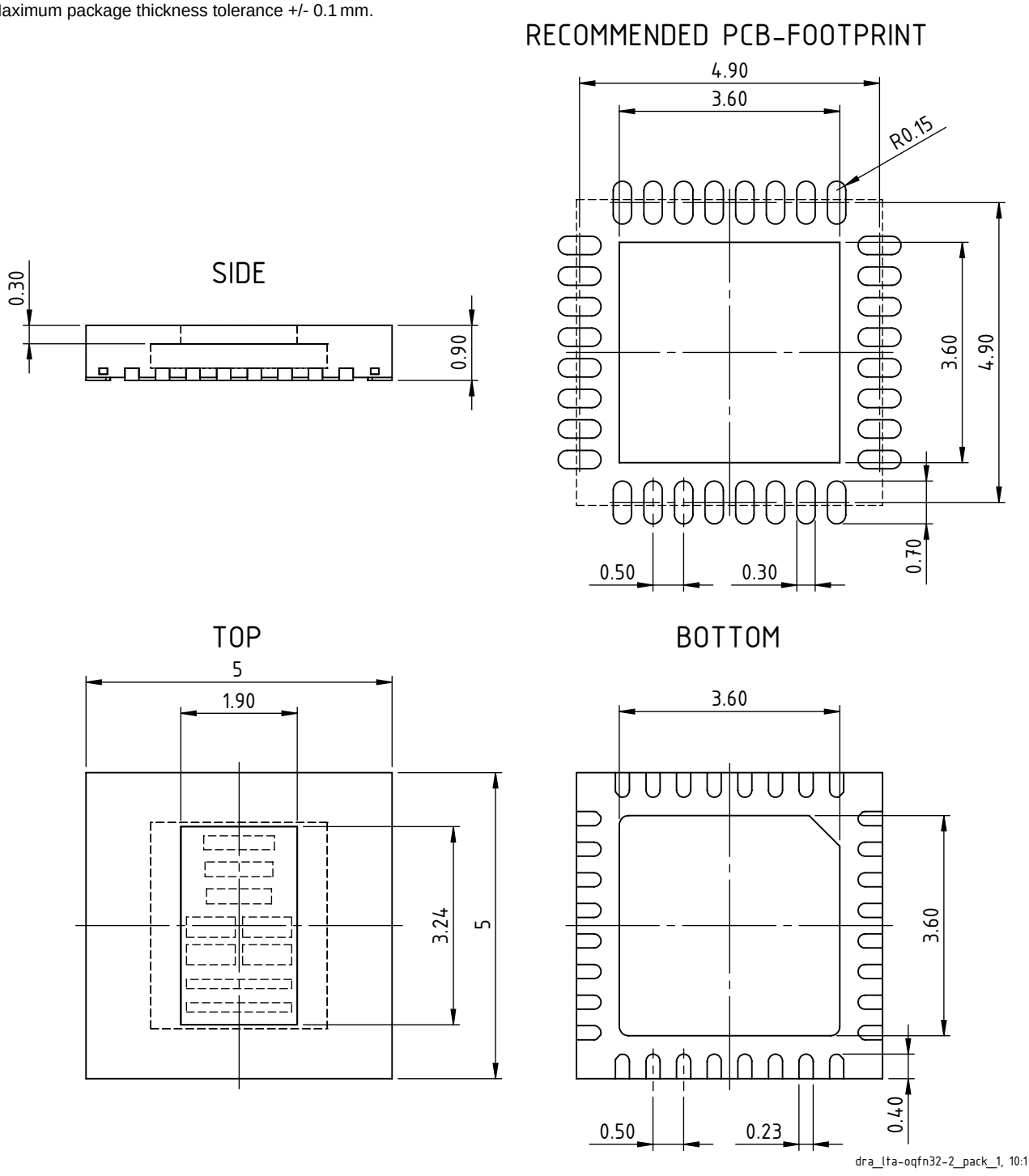
PIN FUNCTIONS

No.	Name	Function
1	VCC	+3.5..5.5 V Supply Voltage
2	LED	LED Controller, High-Side Current Source Output
3	PA	Push-Pull Output A+ / Analog Sin+ [1]
4	NA	Push-Pull Output A- / Analog Sin-
5	PB	Push-Pull Output B+ / Analog Cos+
6	NB	Push-Pull Output B- / Analog Cos-
7	PZ	Push-Pull Output Z+ / Analog Z+
8	NZ	Push-Pull Output Z- / Analog Z-
9..16	n.c.[2]	
17	SEL	Op. Mode Selection Input: lo = digital hi = x2 interpolated open = analog (alignment aid)
18	W	Push-Pull Output W / Analog W
19	TIN	Negative Test Current Input [3]
20	V	Push-Pull Output V / Analog V
21	TIP	Positive Test Current Input [3]
22	U	Push-Pull Output U / Analog U
23	T1	Index Length Selection Input: lo = 0.5 T (B-gated), hi = 1 T (ungated/T-gated), open = 0.25 T (A and B-gated)
24	GND	Ground
25..32	n.c.	
	BP	Backside Paddle [4]

1) Capacitive pin loads must be avoided when using the analog output signals.
2) Pin numbers marked n.c. are not in use.
3) The test pins TIP and TIN may remain unconnected.
4) The backside paddle may have a single link to GND. A current flow across the paddle is not permissible.

PACKAGE DIMENSIONS oQFN32-5x5

All dimensions given in mm.
Maximum molding excess +20 µm / -75 µm versus surface of glass/reticle.
Maximum package thickness tolerance +/- 0.1 mm.



ABSOLUTE MAXIMUM RATINGS

These ratings do not imply operating conditions; functional operation is not guaranteed. Beyond these ratings device damage may occur.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	VCC	Voltage at VCC		-0.3	6	V
G002	I(VCC)	Current in VCC		-20	20	mA
G003	V()	Voltage at Output Pins PA, NA, PB, NB, PZ, NZ, U, V, W#		-0.3	VCC + 0.3	V
G004	I()	Current in Output Pins PA, NA, PB, NB, PZ, NZ, U, V, W#		-20	20	mA
G005	V()	Voltage at LED		-0.3	VCC + 0.3	V
G006	I()	Current in LED		-120	20	mA
G007	V()	Voltage at TIP, TIN, SEL		-0.3	VCC + 0.3	V
G008	I()	Current in TIP, TIN, SEL		-20	20	mA
G009	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G010	Tj	Junction Temperature		-40	150	°C
G011	Ts	Chip Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range	package oQFN32-5x5, oBGA LSH2C	-40		110	°C
T02	Ts	Permissible Storage Temperature Range	package oQFN32-5x5, oBGA LSH2C	-40		110	°C
T03	Tpk	Soldering Peak Temperature	package oBGA LSH2C; tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering TOL (time on label) 8 h; Please refer to customer information file No. 7 for details.			245 230	°C °C
T04	Tpk	Soldering Peak Temperature	package oQFN32-5x5; tpk < 20 s, convection reflow tpk < 20 s, vapor phase soldering MSL 5A (max. floor live 24 h at 30 °C and 60 % RH); Please refer to customer information file No. 7 for details.			245 230	°C °C

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 3.5...5.5 V, Tj = -40...125 °C, $\lambda_{LED} = \lambda r = 740$ nm, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Total Device							
001	VCC	Permissible Supply Voltage		3.5		5.5	V
002	I(VCC)	Supply Current in VCC	no load, photocurrents within op. range		3	10	mA
003	Vc()lo	Clamp-Voltage lo at all pins	I() = -4 mA versus GND	-1.2		-0.3	V
004	Vc()hi	Clamp-Voltage hi at all pins	I() = 4 mA			11	V
005	Vc()hi	Clamp-Voltage hi at LED, PA, NA, PB, NB, PZ, NZ, U, V, W	I() = 4 mA, versus VCC	0.3		1.2	V
006	Vc()hi	Clamp-Voltage hi at SEL, TIP, TIN	I() = 4 mA, versus VCC	0.7		2.2	V
Photosensors							
101	λar	Spectral Application Range	Se(λar) = 0.25 x S(λ)max	400		950	nm
102	λpk	Peak Sensitivity Wavelength			680		nm
103	Aph()	Radiant Sensitive Area	PA, PB, NA, NB PZ, NZ U, V, W		0.264 0.258 0.264		mm^2 mm^2 mm^2
104	S(λr)	Spectral Sensitivity	λ_{LED} = 740 nm λ_{LED} = 850 nm		0.5 0.3		A/W A/W
106	E()mxpk	Permissible Irradiance	λ_{LED}= λpk, Vout() < Vout()mx; PA, PB, NA, NB U, V, W PZ, NZ		 0.55 0.4 0.45		 mW/cm^2 mW/cm^2 mW/cm^2
Photocurrent Amplifiers							
201	Iph()	Permissible Photocurrent Operating Range		0		550	nA
202	η()r	Photo Sensitivity (light-to-voltage conversion ratio)	for PA, PB, NA, NB for PZ, NZ, U, V, W	0.1 0.2	0.3 0.4	0.5 0.6	V/µW V/µW
203	Z()	Equivalent Transimpedance Gain	Z = Vout() / Iph(), Tj = 27 °C; for PA, PB, NA, NB for PZ, NZ, U, V, W	 0.56 0.66	 0.75 1.0	 1 1.36	 MΩ MΩ
204	TCZ	Temperature Coefficient Of Transimpedance Gain			-0.12		%/°C
205	ΔZ()pn	Transimpedance Gain Matching	SEL open, P vs. N path per diff. channel	-0.2		0.2	%
206	ΔVout()	Dark Signal Matching of A, B	SEL open, output vs. output	-8		8	mV
207	ΔVout()	Dark Signal Matching of U, V, W	SEL open, output vs. output	-12		12	mV
208	ΔVout()	Dark Signal Matching of A, B, Z, U, V, W	SEL open, any output vs. any output	-24		24	mV
209	ΔVout()pn	Dark Signal Matching	SEL open, P vs. N path per diff. channel	-2.5		2.5	mV
211	fc()hi	Cut-off Frequency (-3 dB)		400	500		kHz
Analog Outputs PA, NA, PB, NB, PZ, NZ, U, V, W							
301	Vout()mx	Maximum Output Voltage	illumination to E()mxpk	1.04	1.27	1.8	V
302	Vout()d	Dark Signal Level	load 100 kΩ vs. +2 V	640	770	985	mV
303	Vout()acmx	Maximum Signal Level	Vout()acmx = Vout()mx - Vout()d	0.3	0.5	0.75	V
304	Isc()hi	Short-Circuit Current hi	SEL open, load current to ground	100	1800	3000	µA
305	Isc()lo	Short-Circuit Current lo	SEL open, load current to IC	20	40	200	µA
306	Ri()	Internal Output Resistance	f = 1 kHz	250	750	2250	Ω
Comparators							
401	Vt()hi	Upper Comparator Threshold	Iph()p x Z()p > Iph()n x Z()n, resp. Iph()p x Z()p > internal VREF	5	12	25	mV
402	Vt()lo	Lower Comparator Threshold	Iph()p x Z()p < Iph()n x Z()n, resp. Iph()p x Z()p < internal VREF	-25	-12	-5	mV
403	Vt()hys	Comparator Hysteresis	Vt()hys = Vt()hi - Vt()lo	10	24	50	mV

ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = 3.5...5.5 V, Tj = -40...125 °C, $\lambda_{LED} = \lambda r = 740$ nm, unless otherwise noted

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
LED Power Control							
501	Iop()	Permissible LED Output Current		-40		0	mA
502	Vs()hi	Saturation Voltage hi	Vs()hi = VCC - V(LED), I() = -40 mA	0.25	0.5	1	V
503	Isc()hi	Short-Circuit Current hi	V() = 0 V	-150		-50	mA
Digital Output Drivers PA, NA, PB, NB, PZ, NZ, U, V, W							
601	fout	Maximum Output Frequency		800			kHz
602	Vs()lo	Saturation Voltage lo	VCC = 4.5...5.5 V, I() = 4mA, Tj = 70 °C			0.4	V
603	Vs()lo	Saturation Voltage lo	VCC = 4.5...5.5 V, I() = 4mA, Tj = 85 °C			0.5	V
604	Vs()lo	Saturation Voltage lo	VCC = 3.5...4.5 V, I() = 4mA			0.6	V
605	Isc()lo	Short-Circuit Current lo	V() = VCC	7		70	mA
606	Vs()hi	Saturation Voltage hi	Vs()hi = VCC - V(), I() = -4 mA; VCC = 4.5...5.5 V VCC = 3.5...4.5 V			 0.4 0.6	 V V
607	Isc()hi	Short-Circuit Current hi	V() = 0 V	-70		-7	mA
Selection Input SEL							
701	Vt1()hi	Upper Threshold Voltage hi	for A/B mode with x2 interpolation	78	80	82	%VCC
702	Vt1()lo	Upper Threshold Voltage lo	for A/B mode with x2 interpolation	68	70	72	%VCC
703	Vt1()hys	Upper Threshold Hysteresis	Vt1()hys = Vt1()hi - Vt1()lo	8	10	12	%VCC
704	Vt2()hi	Lower Threshold Voltage hi	for A/B mode	28	30	32	%VCC
705	Vt2()lo	Lower Threshold Voltage lo	for A/B mode	18	20	22	%VCC
706	Vt2()hys	Lower Threshold Hysteresis	Vt2()hys = Vt2()hi - Vt2()lo	8	10	12	%VCC
707	V0()	Pin-Open Voltage	for analog mode	45	50	55	%VCC
708	Rpd()	Pull-Down Resistor	SEL to GND, V(SEL) = VCC	70	100	140	kΩ
709	Rpu()	Pull-Up Resistor	VCC to SEL, V(SEL) = 0 V	70	100	140	kΩ
710	Vpd()	Pull-Down Voltage vs. VCC/2	Vpd() = V() - VCC/2; I() = 0...5 µA			0.5	V
711	Vpu()	Pull-Up Voltage vs. VCC/2	Vpu() = V() - VCC/2; I() = -5...0 µA	-0.5			V
Test Circuit Inputs TIP, TIN							
801	I()test	Permissible Test Current Range	test mode active	10		600	µA
802	V()test	Test Pin Voltage	test mode active, I() = 200 µA	1.25	1.5	1.75	V
803	Ipd()	Test Pin Pull-Down Current	test mode not active, V() = 0.4 V	60	100	160	µA
804	Ipd()	Test Pin Pull-Down Current	V() = VCC	0.7	2	3	mA
805	It()on	Test Mode Activation Threshold		80	130	190	µA
806	CR()	Test Mode Current Ratio I()/Iph()	test mode active, I() = 200 µA	1599	3000	5000	
Power-On-Reset Circuit							
901	VCCon	Turn-on Threshold VCC (power-on release)	increasing voltage at VCC		2.6	3.45	V
902	VCCoff	Turn-off Threshold VCC (power-down reset)	decreasing voltage at VCC	1.4	2.4		V
903	VCChys	Threshold Hysteresis	VCChys = VCCon - VCCoff	50	170	300	mV
Index Length Selection Input T1							
A01	Vt1()hi	Upper Threshold Voltage hi	for index length 1 T	78	80	82	%VCC
A02	Vt1()lo	Upper Threshold Voltage lo	for index length 1 T	68	70	72	%VCC
A03	Vt1()hys	Upper Threshold Hysteresis	Vt1()hys = Vt1()hi - Vt1()lo	8	10	12	%VCC
A04	Vt2()hi	Lower Threshold Voltage hi	for index length 0.5 T (B-gated)	28	30	32	%VCC
A05	Vt2()lo	Lower Threshold Voltage lo	for index length 0.5 T (B-gated)	18	20	22	%VCC
A06	Vt2()hys	Lower Threshold Hysteresis	Vt2()hys = Vt2()hi - Vt2()lo	8	10	12	%VCC
A07	V0()	Pin-Open Voltage	for index length 0.25 T (AB-gated)	45	50	55	%VCC
A08	Rpu()	Pull-Up Resistor	VCC to T1, V(T1) = 0 V	70	100	140	kΩ
A09	Rpd()	Pull-Down Resistor	T1 to GND, V(T1) = VCC	70	100	140	kΩ
A10	Vpd()	Pull-Down Voltage vs. VCC/2	Vpd() = V() - VCC/2; I() = 0...5 µA			0.5	V
A11	Vpu()	Pull-Up Voltage vs. VCC/2	Vpu() = V() - VCC/2; I() = -5...0 µA	-0.5			V

DIGITAL OUTPUT SIGNALS

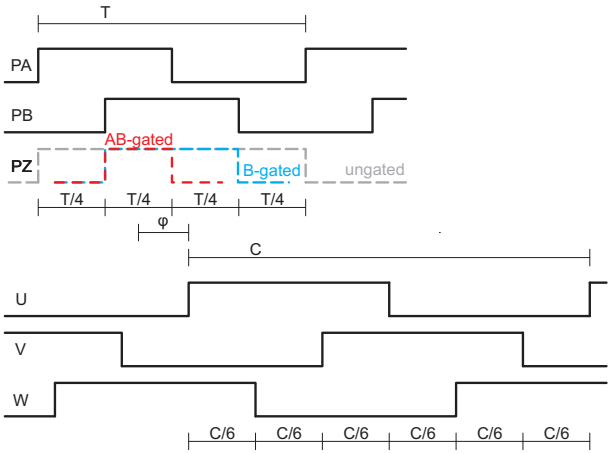


Figure 1: Typical encoder quadrature and motor commutation signals.

iC-LTA's photo-sensor array requires an external reticle (placed either on side of the IC or on side of the LED), and thus allows for a free definition of the optical radius and cycles per revolution for the A and B encoder quadrature signals.

The pulse count, period length and phase shift for the U, V, W commutation signals is also determined by the code disc design.

Contracted code disc designs and IC packaging with custom reticle can be offered on request; contact iC-Haus for details.

ANALOG OUTPUT SIGNALS

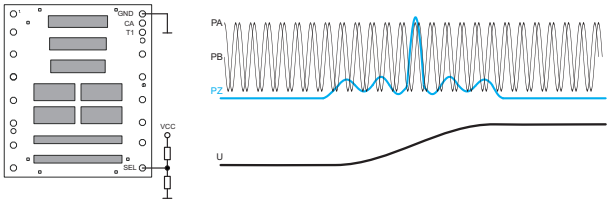


Figure 2: Analog signal output (pin SEL open).

When the operating mode selection input SEL is left open, all digital outputs are disabled and analog output signals are available for test and alignment.

If analog signals are desired permanently, noise immunity can be improved by wiring pin SEL to an external VCC/2 reference.

INDEX GATING

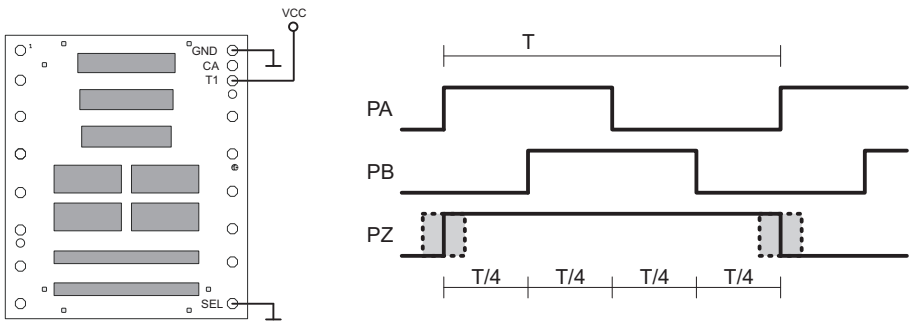


Figure 3: Ungated index signal (T1 = high) at x1 interpolation (SEL = low).

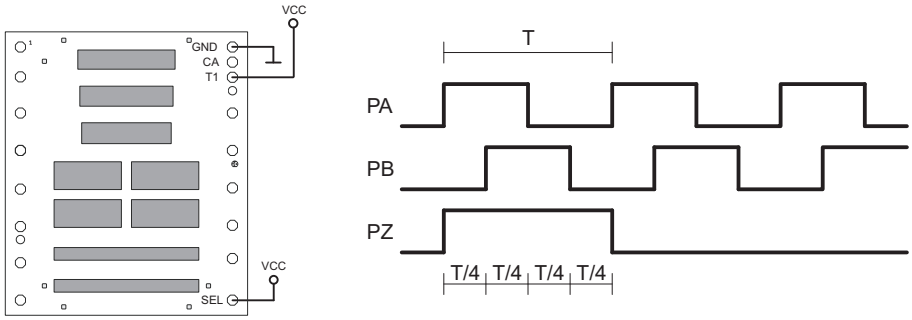


Figure 4: T-gated index signal (T1 = high) at x2 interpolation (SEL = high).

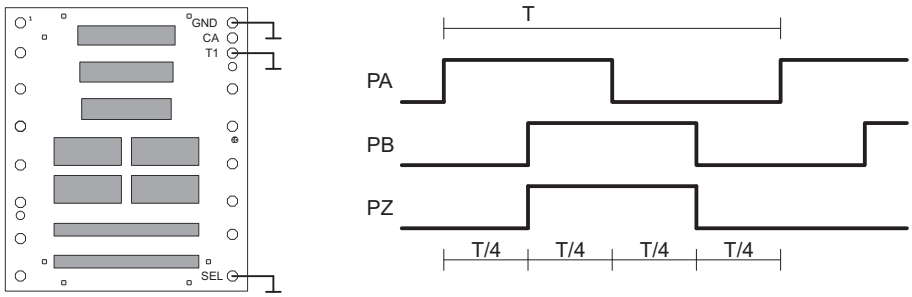


Figure 5: B-gated index signal (T1 = low) at x1 interpolation (SEL = low).

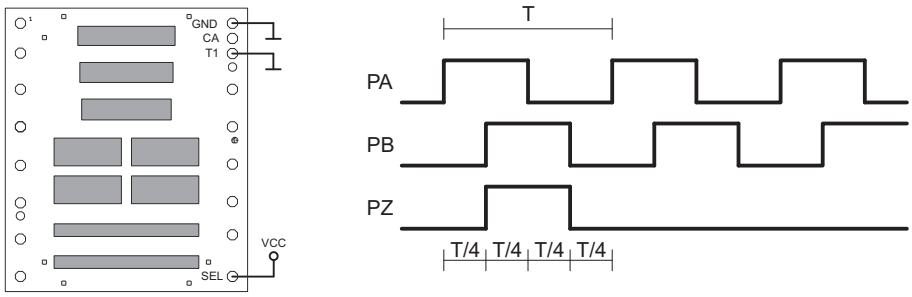


Figure 6: B-gated index signal (T1 = low) at x2 interpolation (SEL = high).

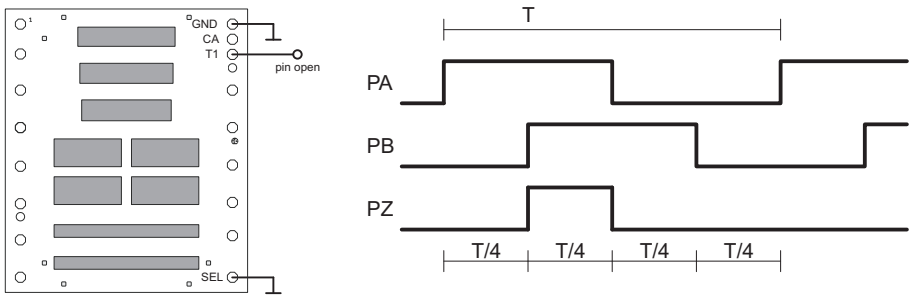


Figure 7: AB-gated index signal (T1 = open or VCC/2) at x1 interpolation (SEL = low).

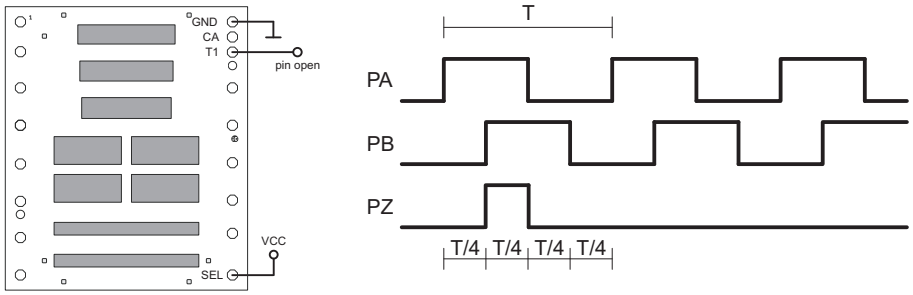


Figure 8: AB-gated index signal (T1 = open or VCC/2) at x2 interpolation (SEL = high).

APPLICATION CIRCUITS

Please refer to iC-PTxx series IC's application notes which are available separately.

DESIGN REVIEW: Notes on Chip Functions

iC-LTA_Y		
No.	Function, Parameter/Code	Description and Application Hints
1	Index gating 1/4 T	Package oBGA LSH2C: Index length preset to 1/4 T (AB-gated). (Package oQFN32-5x5 is not available.)

Table 4: Chip release iC-LTA_Y

iC-LTA_X		
No.	Function, Parameter/Code	Description and Application Hints
1	Index length selection input T1	Package oBGA LSH2C: Index length preset to 1/4 T (AB-gated). Package oQFN32-5x5: Index length selection input T1 available on pin no. 23.

Table 5: Chip release iC-LTA_X

ORDERING INFORMATION

Type	Package	Options	Order Designation
iC-LTA	15-pin optoBGA, 6.2 mm x 5.2 mm, thickness 1.7 mm	AB-gated index, glass lid	iC-LTA oBGA LSH2C
		AB-gated index, on-chip reticle	iC-LTA oBGA LSH2C-xR
iC-LTA	32-pin optoQFN, 5 mm x 5 mm, thickness 0.9 mm	selectable index gating, glass lid	iC-LTA oQFN32-5x5
		selectable index gating, on-chip reticle	iC-LTA oQFN32-5x5-xR

For technical support, information about prices and terms of delivery please contact:

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