

M62364FP

8-bit 8ch Multiplying D/A Converter with Buffer Amplifiers

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Description

The M62364FP is a CMOS 8-bit 8ch D/A converter having a multiplying function and output buffer amplifiers. It has a serial data input and can easily communicate with a microcontroller by the simple three-wiring method (DI, CLK, LD).

The output buffer amplifiers operating in AB-class has both sinking and driving capabilities of 1.0 mA or more and can operate in a whole supply range from V_{DD} to GND.

The IC is suitable for a use in automatic adjustment applications in conjunction with a MCU by utilizing the terminal D_O for a cascading connection.

Features

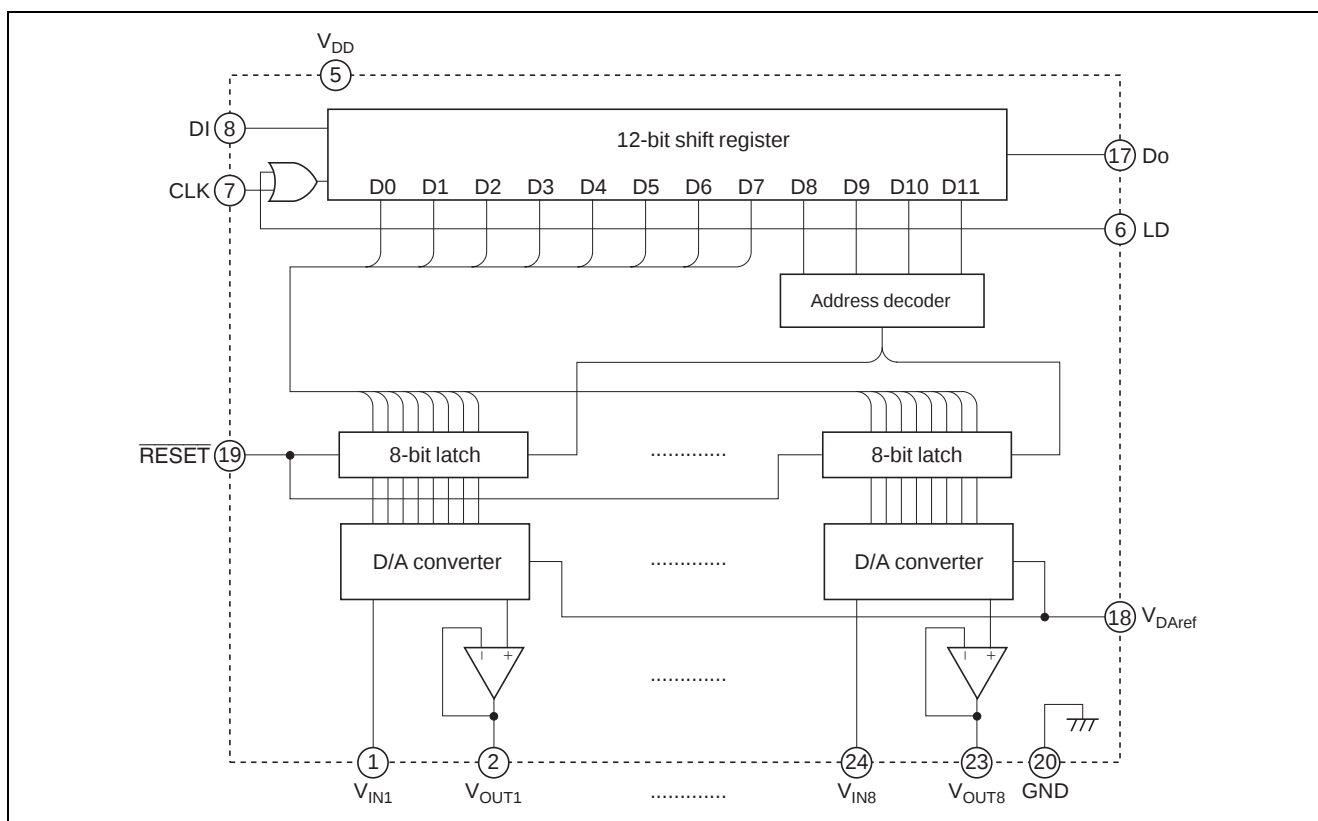
- Three-wiring serial data transmission
- Doubled precision 8ch D/A converter employing an R-2R with higher-order segment method
- 8 buffer amplifiers operating in a whole supply voltage range from V_{DD} to GND
- 4 quadrant multiplication

Application

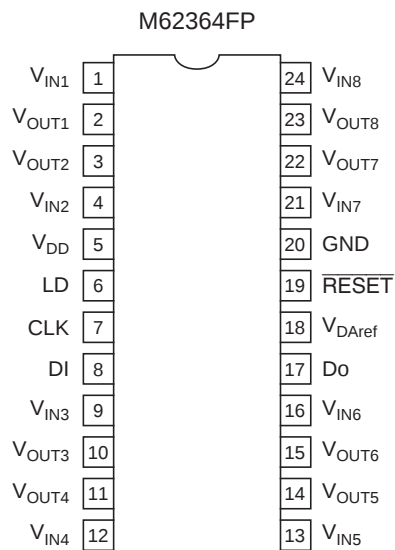
Digital to analog conversion for consumer and industrial equipment.

Gain setting and automatic adjustment of display-monitor and CTV.

Block Diagram



Pin Arrangement



Pin Description

Pin No.	Pin Name	Function
8	DI	Serial data input
17	DO	Serial data output
7	CLK	Shift clock input. Input data of DI are taken into the 12-bit shift register on a rising edge of the clock.
6	LD	A low state enables data loading to the 12-bit shift register. During a rising edge of LD, the data will be loaded to the output register.
19	$\overline{\text{RESET}}$	Reset 8-bit latches
2	V _{OUT1}	D/A converter output with 8-bit resolution
3	V _{OUT2}	
10	V _{OUT3}	
11	V _{OUT4}	
14	V _{OUT5}	
15	V _{OUT6}	
22	V _{OUT7}	
23	V _{OUT8}	
5	V _{DD}	Power supply
20	GND	Ground
1	V _{IN1}	D/A converter input
4	V _{IN2}	
9	V _{IN3}	
12	V _{IN4}	
13	V _{IN5}	
16	V _{IN6}	
21	V _{IN7}	
24	V _{IN8}	
18	V _{DAref}	D/A converter reference voltage input

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.3 to +7.0	V
Digital input voltage	V_{IND}	-0.3 to +7.0	V
Analog input voltage	V_{IN}	-0.3 to $V_{DD} + 0.3$	V
Analog output voltage	V_{OUT}	-0.3 to $V_{DD} + 0.3$	V
D/A reference voltage	V_{DAref}	-0.3 to $V_{DD} + 0.3$	V
Operating temperature	T_{opr}	-20 to +75	°C
Storage temperature	T_{stg}	-40 to +125	°C

Electrical Characteristics

<Ana/Dig Common Part>

($V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} \geq V_{IN}$, GND, $V_{DAref} = 0\text{ V}$, $T_a = -20$ to $+85^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Supply voltage	V_{DD}	2.7	5.0	5.5	V	
Supply current	I_{DD}	—	—	3.5	mA	CLK = 1 MHz, $V_{CC} = 3\text{ V}$, $I_{AO} = 0\text{ }\mu\text{A}$

<Digital Part>

($V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} \geq V_{IN}$, GND, $V_{DAref} = 0\text{ V}$, $T_a = -20$ to $+85^\circ\text{C}$, unless otherwise noted.)

Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input leak current	I_{ILK}	-10	—	10	μA	$V_{IN} = 0$ to V_{DD}
Digital input "Low" voltage	V_{IL}	—	—	$0.2 V_{DD}$	V	
Digital input "High" voltage	V_{IH}	$0.8 V_{DD}$	—	—	V	
D _O terminal output "Low" voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.5\text{ mA}$
D _O terminal output "High" voltage	V_{OH}	$V_{DD} - 0.4$	—	—	V	$I_{OH} = -400\text{ }\mu\text{A}$

<Analog Part>

($V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} \geq V_{IN}$, GND, $V_{DAref} = 0\text{ V}$, $T_a = -20$ to $+85^\circ\text{C}$, unless otherwise noted.)

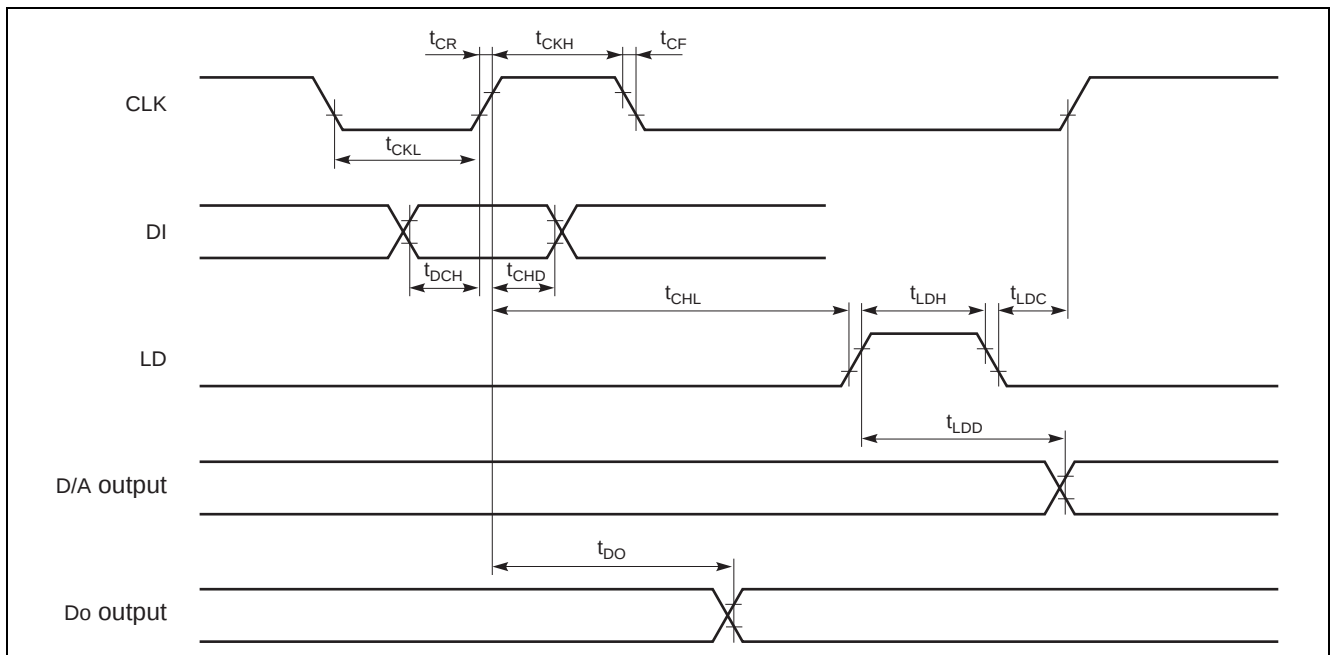
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Input current	I_{IN}	—	—	0.30	mA	$V_{IN} = 5\text{ V}$, $V_{DAref} = 0\text{ V}$ Proportional to Max. input current condition ($V_{IN} - V_{DAref}$) and digital data of each channels
D/A reference input current	I_{DAref}	-2.40	—	—	mA	$V_{IN} = 5\text{ V}$, $V_{DAref} = 0\text{ V}$ Proportional to Max. input current condition ($V_{IN} - V_{DAref}$) and digital data of each channels
Resolution	RES	—	8	—	bit	
Differential nonlinearity	DNL	-1	—	1	LSB	$V_{DAref} = 0.050\text{ V}$ (10 mV/LSB) Without load ($I_{AO} = \pm 0$)
Nonlinearity	NL	-1	—	1	LSB	
Buffer amplifier output voltage range	V_{AO}	0.1	—	$V_{CC} - 0.1$	V	$I_{AO} = \pm 100\text{ }\mu\text{A}$
		0.2	—	$V_{CC} - 0.2$		$I_{AO} = \pm 500\text{ }\mu\text{A}$
Buffer amplifier output current range	I_{AO}	-1	—	1	mA	Upper saturation voltage = 0.4 V Lower saturation voltage = 0.4 V
Output capacitive load	C_O	—	—	0.1	μF	
Buffer amplifier output impedance	R_O	—	5	—	Ω	

AC Characteristics

($V_{DD} = 5\text{ V} \pm 10\%$, $V_{DD} \geq V_{IN}$, GND , $V_{DAREF} = 0\text{ V}$, $T_a = -20\text{ to }+85^\circ\text{C}$, unless otherwise noted.)

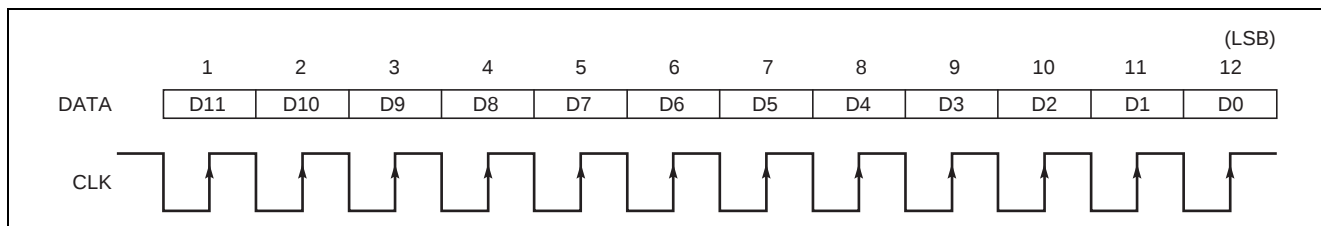
Item	Symbol	Limits			Unit	Conditions
		Min	Typ	Max		
Clock "L" pulse width	t_{CKL}	200	—	—	ns	
Clock "H" pulse width	t_{CKH}	200	—	—	ns	
Clock rise time	t_{CR}	—	—	200	ns	
Clock fall time	t_{CF}	—	—	200	ns	
Data setup time	t_{DCH}	60	—	—	ns	
Data hold time	t_{CHD}	100	—	—	ns	
LD setup time	t_{CHL}	200	—	—	ns	
LD hold time	t_{LDC}	100	—	—	ns	
LD "H" pulse duration time	t_{LDH}	100	—	—	ns	
Data output delay time	t_{DO}	70	—	350	ns	$C_L = 100\text{ pF}$
D/A output setting time	t_{LDD}	—	—	300	μs	$C_L \leq 100\text{ pF}$, $V_{AO}: 0.1 \leftrightarrow 2.6\text{ V}$ This time until the output becomes the final value of 1/2 LSB

Timing Chart



Digital Data Format

12-bit serial data



Data Assignment

D0	D1	D2	D3	D4	D5	D6	D7	: DAC data
(LSB)							(MSB)	
D8	D9	D10	D11	: DAC select data				

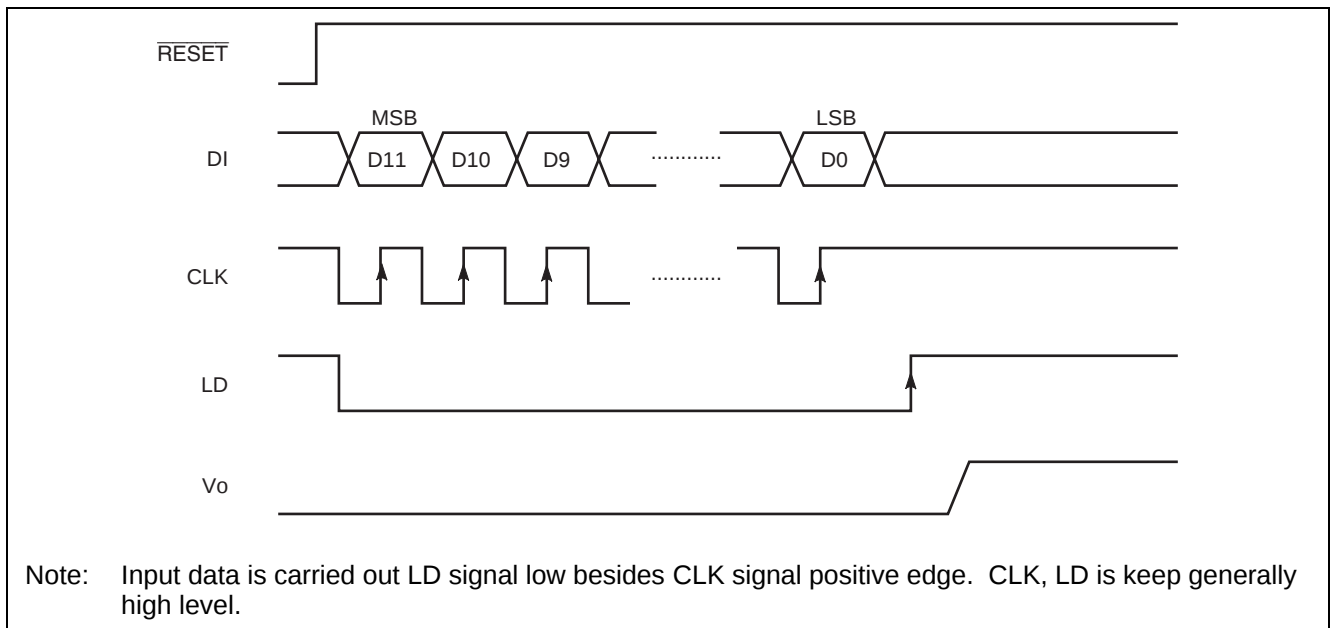
DAC Data

D0	D1	D2	D3	D4	D5	D6	D7	D/A Output
0	0	0	0	0	0	0	0	$V_{D\text{Aref}}$
1	0	0	0	0	0	0	0	$(V_{\text{IN}} - V_{D\text{Aref}}) / 256 \times 1 + V_{D\text{Aref}}$
0	1	0	0	0	0	0	0	$(V_{\text{IN}} - V_{D\text{Aref}}) / 256 \times 2 + V_{D\text{Aref}}$
1	1	0	0	0	0	0	0	$(V_{\text{IN}} - V_{D\text{Aref}}) / 256 \times 3 + V_{D\text{Aref}}$
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	$(V_{\text{IN}} - V_{D\text{Aref}}) / 256 \times 255 + V_{D\text{Aref}}$

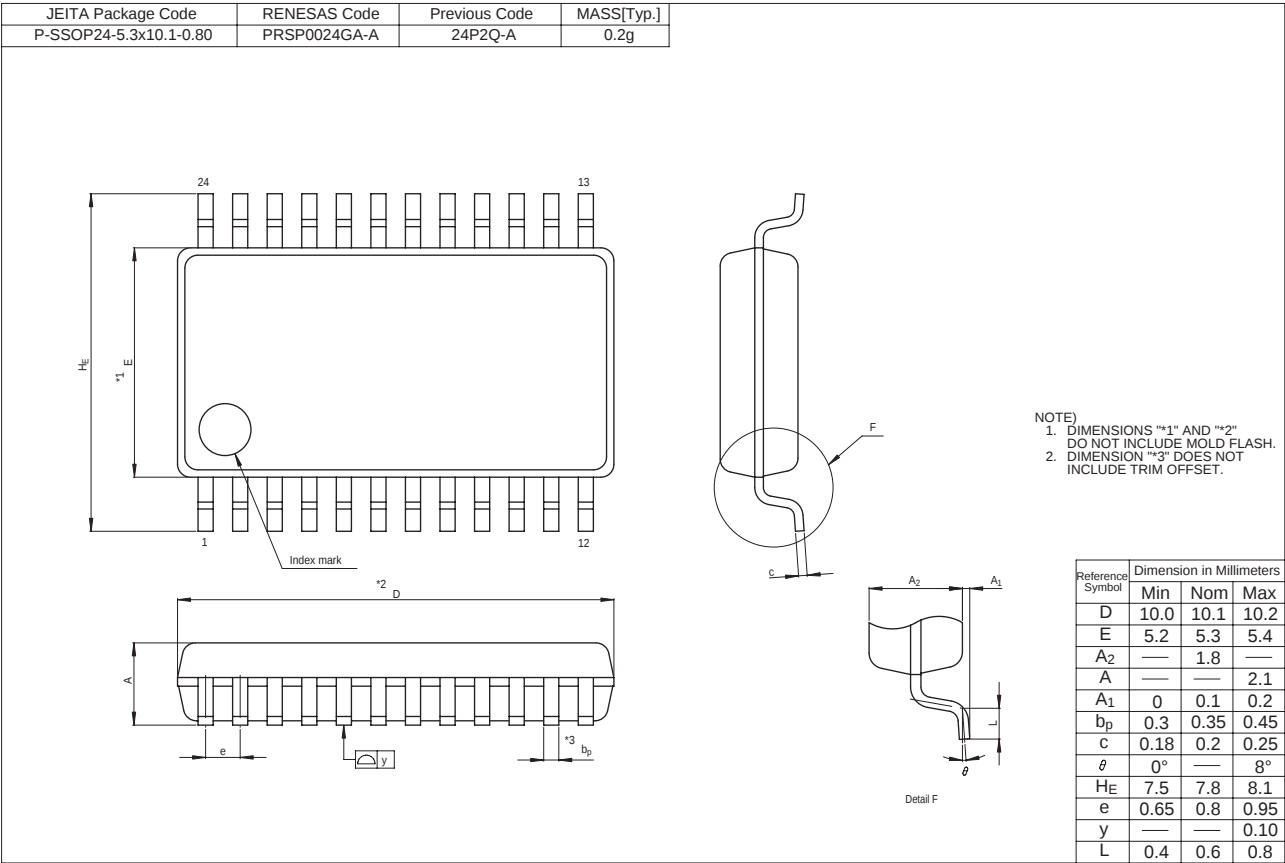
DAC Select Data

D8	D9	D10	D11	DAC Selection
0	0	0	0	Don't care
0	0	0	1	V_{OUT1} selection
0	0	1	0	V_{OUT2} selection
0	0	1	1	V_{OUT3} selection
0	1	0	0	V_{OUT4} selection
0	1	0	1	V_{OUT5} selection
0	1	1	0	V_{OUT6} selection
0	1	1	1	V_{OUT7} selection
1	0	0	0	V_{OUT8} selection
1	0	0	1	Don't care
1	0	1	0	Don't care
1	0	1	1	Don't care
1	1	0	0	Don't care
1	1	0	1	Don't care
1	1	1	0	Don't care
1	1	1	1	Don't care

Timing Chart (Model)



Package Dimensions



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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

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Renesas Technology Hong Kong Ltd.
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Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 3518-3399

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510