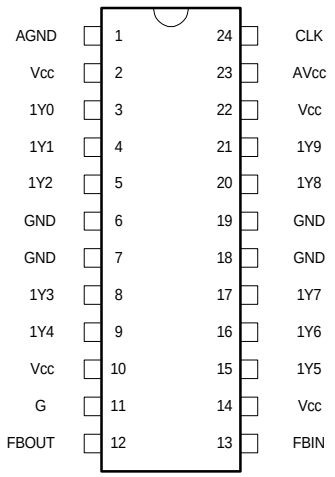
HC2510C

Features

- **Phase-Locked Loop Clock Distribution for Synchronous DRAM Applications**
- **Supports PC-100 and Meets "PC100 SDRAM registered DIMM Specification Rev. 1.2"**
- **Distributes One Clock Input to One Bank of Ten Outputs**
- **No External RC Network Required**
- **External Feedback (FBIN) Pin is Used to Synchronize the Outputs to the Clock Input**
- **Separate Output Enable for Each Output Bank**
- **Operates at 3.3 V V_{cc}**
- **125 MHz Maximum Frequency**
- **On-chip Series Damping Resistors**
- **Support Spread Spectrum Clock(SSC) Synthesizers**
- **ESD Protection Exceeds 3000 V per MIL-STD-883, Method 3015 ; Exceeds 350 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 400 mA per JESD 17**
- **Packaged in Plastic 24-Pin Thin Shrink Small-Outline Package**

Pin Configuration

TSSOP 24 PACKAGE
(TOP VIEW)



General Description

The HC2510C is a low-skew, low jitter, phase-locked loop(PLL) clock driver, distributing high frequency clock signals for SDRAM.

The HC2510C operates at 3.3V V_{cc} and provides integrated series-damping resistors that make it ideal for driving point-to-point loads. The propagation delay from the CLK input to any clock output is nearly zero.

Ten outputs provide low-skew and low-jitter clocks. All outputs can be enabled or disabled via the control input(G). Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK.

The HC2510C is specially designed to interface with high speed SDRAM applications in the range of 25MHz to 125MHz and includes an internal RC network which provides excellent jitter characteristics and eliminates the needs for external components. For the test purpose, the PLL can be bypassed by strapping AV_{cc} to ground.

The HC2510C is characterized for operation from 0°C to 85°C.

Function Table

INPUTS		OUTPUTS	
G	CLK	1Y (0:9)	FBOUT
X	L	L	L
L	H	L	H
H	H	H	H

Functional Block Diagram

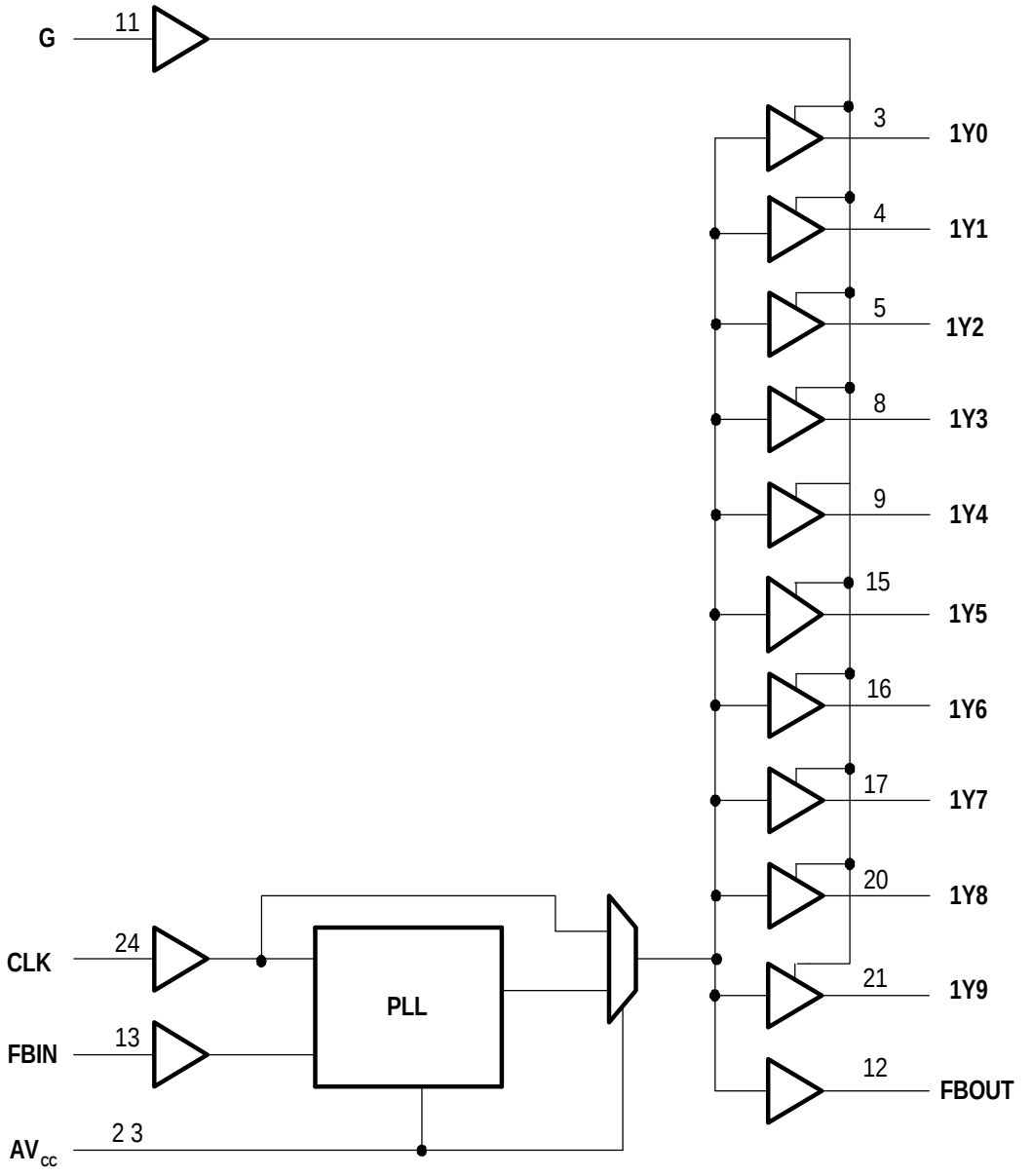


Table 1. Pin Description

Pin Name	Pin No.	Type	Functional Description
CLK	24	I	Clock Input. CLK provides the reference signal to the internal PLL.
FBIN	13	I	Feedback Input. FBIN provides the feedback signal to the internal PLL.
G	11	I	Output Bank Enable. When G is high, all outputs 1Y(0:9) are enabled. When G is low, Outputs 1Y(0:9) are disable to a logic-low state.
FBOUT	12	O	Feedback Output. FBOUT completes the feedback loop of the PLL by being wired to FBIN.
1Y(0:9)	3,4,5,8,9 15,16,17,20,21	O	Clock Outputs. These outputs provide low-skew copies of CLKIN. Each output has an embedded series-damping resistor.
AV_{cc}	23	Power	Analog Power Supply. AV_{cc} provides the power reference for the analog circuitry. AV_{cc} can be also used to bypass the PLL for the test purpose. When AV_{cc} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs.
AGND	1	Ground	Analog Ground. AGND provides the ground reference for the analog circuitry.
V_{cc}	2,10,14,22	Power	Power Supply
GND	6,7,18,19	Ground	Ground

Table 2. Absolute Maximum Ratings Over Operating Free-air Temperature Range

Symbols	Parameter	Value	Unit	Conditions
V_{cc}	Supply Voltage Range	**-0.5 to 4.6**	V	
V_I	Input Voltage Range	**-0.5 to 6.5**	V	
V_o	Voltage Range applied to any input in the high or low state	**-0.5 to Vcc+0.5**	V	
I_{IK}	Input Clamp Current	**±50**	mA	V_I <0 or V_I >V_{cc}
I_{OK}	Output Clamp Current	**±50**	mA	V_o<0 or V_o >V_{cc}
I_o	Continuous Output Current	**±50**	mA	V_o =0 to V_{cc}
P_{MAX}	Maximum Power Dissipaiton	**0.7**	W	
T_{stg}	Storage Temperature Range	**- 65 to 150**	°C	

Table 3. Recommended Operating Conditions

Symbol	Parameter	Value		Unit	Condition
		Min	Max		
AV_{CC}	Supply Voltage	**3**	**3.6**	V	
V_{IH}	High-level Input Voltage	**2**		V	
V_{IL}	Low-level Input Voltage		**0.8**	V	
V_I	Input Voltage	**0**	V_{CC}	V	
I_{OH}	High-level Output Current		**-12**	mA	
I_{OL}	Low-level Output Current		**12**	mA	
T_A	Operating Free-air Temperature	**0**	**85**	°C	

Table 4. Electrical Characteristics Over Recommended Operating Free-air Temperature Range

Symbol	Value			Unit	AV_{CC} (V)	Test Conditions
	Min	Typ	Max			
V_{IK}			**-1.2**	V	3	I_I = -18mA
V_{OH}	**Vcc-0.2**			V	Min to Max	I_{OH} = -100µA
	2.1				3	I_{OH} = -12 mA
	2.4				3	I_{OH} = -6 mA
V_{OL}			**0.2**	V	Min to Max	I_{OL} =100 mA
			0.8		3	I_{OL} = 12 mA
			0.55		3	I_{OL} = 6 mA
I_I			±**5**	µA	3.6	V_I =V_{CC} or GND
I_{CC}			**10**	µA	3.6	V_I =V_{CC} or GND, I_O = 0, Ouputs: low or high
ΔI_{CC}			**500**	µA	3.3 to 3.6	One input at V_{CC} - 0.6V, Other Inputs at V_{CC} or GND
C_i		**4**		pF	3.3	V_I = V_{CC} or GND
C_o		**6**		pF	3.3	V_O = V_{CC} or GND

Table 5.Timing Requirements Over Recommended Ranges of Supply Voltage and Operating free-air Temperature

Symbol	Parameter	Value		Unit
		Min	Max	
f_{clock}	Clock Frequency	25	125	MHz
	Input Clock Duty Cycle	40	60	%
	Stabilization Time♣		1	ms

♣ Time to obtain phase lock of its feedback signal to its reference signal.

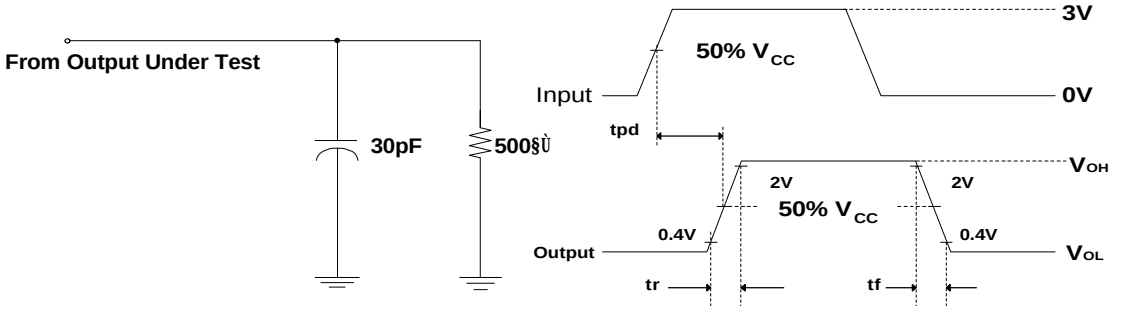
Table 6. Switching Characteristics Over Recommended Ranges of Supply Voltage and Operating Free-air Temperature. (C_L=30pF) †

Parameter	From(Input)	TO(Output)	V_{CC} = 3.3V ±0.165V			V_{CC} = 3.3V±0.3V			Unit
			Min	Typ	Max	Min	Typ	Max	
$t_{phase\ error}$ ♣	66MHz < CLKIN↑< 100MHz	FBIN↑	150		150				ps
	CLKIN↑ = 100MHz	FBIN↑	-50		50				ps
t_{sk}	Any Y of FBOUT	Any Y or FBOUT						200	ps
Jitter(pk-pk)	CLKIN > 66MHz	Any Y or FBOUT				-100		100	ps
Duty Cycle	CLKIN > 66MHz	Any Y or FBOUT				45		55	%
t_r		Any Y or FBOUT		1.3	1.9	0.8		2.1	ns
t_f		Any Y or FBOUT		1.7	2.5	1.2		2.7	ns

†These parameters are not production tested.

♣ Phase error does not include jitter.

Figure 1. Load Circuit and Voltage Waveforms



Load Circuit For Outputs

Voltage Waveforms Propagation Delay Times

Notes: 1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100MHz, Z_o =50Ω, t_r =1.2ns, t_f=1.2ns

2.The outputs are measured one at a time with one transition per measurement.

Figure 2. Phase Error and Skew Calculation

