WM8721

Internet Audio DAC with Integrated Headphone Driver

DESCRIPTION

The WM8721 is a low power stereo DAC with an integrated headphone driver. The WM8721 is designed specifically for portable MP3 audio and speech players. The WM8721 is also ideal for MD, CD machines and DAT players.

Stereo 24-bit multi-bit sigma delta DACs are used with oversampling digital interpolation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported.

Stereo audio outputs are buffered for driving headphones from a programmable volume control, line level outputs are also provided along with anti-thump mute and power up/down circuitry.

The device is controlled via a 2 or 3 wire serial interface. The interface provides access to all features including volume controls, mutes, de-emphasis and extensive power management facilities. The device is available in a small 20-pin SSOP package.

A USB mode is provided where all audio rates can be derived from a simple 12MHz or 24MHz master clock, eliminating the need for a PLL or multiple crystals.

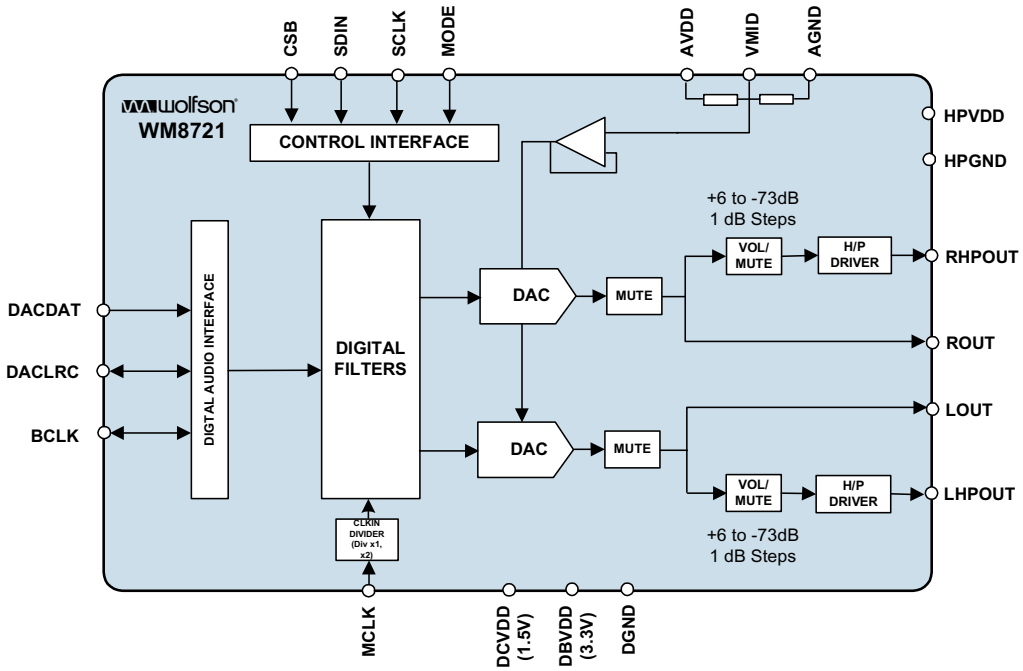
FEATURES

- Audio Performance
  - DAC SNR 100dB ('A' weighted) at AVDD = 3.3V
  - 1.42 – 3.6V Digital Supply Operation
  - 2.7 – 3.6V Analogue Supply Operation
- Low Power
  - Headphone Playback: 20mW at AVDD = 3.3V
- DAC Sampling Frequency: 8kHz – 96kHz
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- Stereo Audio Outputs
- Output Volume and Mute Controls
- Highly Efficient Headphone Driver
- 20-Pin SSOP Package

APPLICATIONS

- Portable MP3 Players
- CD and Minidisc Players

BLOCK DIAGRAM

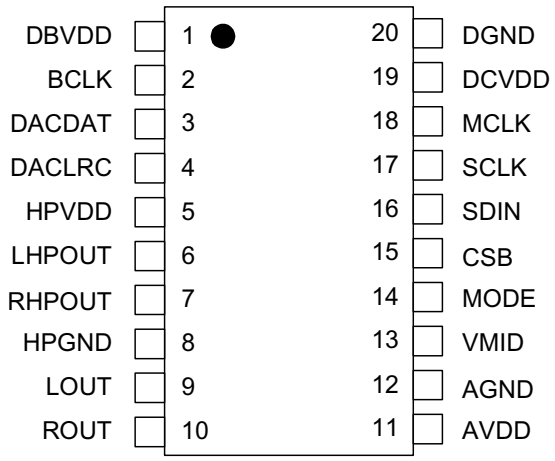


Copyright ©2004 Wolfson Microelectronics plc

TABLE OF CONTENTS

DESCRIPTION 1
FEATURES 1
APPLICATIONS 1
BLOCK DIAGRAM 1
TABLE OF CONTENTS 2
PIN CONFIGURATION 3
ORDERING INFORMATION 3
PIN DESCRIPTION 4
ABSOLUTE MAXIMUM RATINGS 5
RECOMMENDED OPERATING CONDITIONS 5
ELECTRICAL CHARACTERISTICS 6
TERMINOLOGY 7
POWER CONSUMPTION 7
MASTER CLOCK TIMING 8
DIGITAL AUDIO INTERFACE – MASTER MODE 8
DIGITAL AUDIO INTERFACE – SLAVE MODE 9
MPU INTERFACE TIMING 9
DEVICE DESCRIPTION 11
INTRODUCTION 11
AUDIO SIGNAL PATH 11
DEVICE OPERATION 16
AUDIO DATA SAMPLING RATES 21
ACTIVATING DSP AND DIGITAL AUDIO INTERFACE 25
SOFTWARE CONTROL INTERFACE 25
POWER DOWN MODES 27
REGISTER MAP 28
DAC FILTER RESPONSES 32
DIGITAL DE-EMPHASIS CHARACTERISTICS 33
RECOMMENDED EXTERNAL COMPONENTS 35
PACKAGE DIMENSIONS 36
IMPORTANT NOTICE 37
ADDRESS: 37

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
XWM8721EDS	-25 to +85°C	20-pin SSOP	MSL 1	260°C
XWM8721EDS/R	-25 to +85°C	20-pin SSOP (tape and reel)	MSL 1	260°C
WM8721SEDS	-25 to +85°C	20-pin SSOP (lead free)	MSL 1	260°C
WM8721SEDS/R	-25 to +85°C	20-pin SSOP (lead free, tape and reel)	MSL 1	260°C

Note:
Reel quantity = 2,000

PIN DESCRIPTION

20 PIN SSOP	NAME	TYPE	DESCRIPTION
1	DBVDD	Supply	Digital Buffers VDD
2	BCLK	Digital Input/Output	Digital Audio Port Clock
3	DACDAT	Digital Input	DAC Digital Audio Data Input
4	DACLRC	Digital Input/Output	DAC Sample Rate Clock
5	HPVDD	Supply	Headphone VDD
6	LHPOUT	Analogue Output	Left Channel Headphone Output
7	RHPOUT	Analogue Output	Right Channel Headphone Output
8	HPGND	Ground	Headphone GND
9	LOUT	Analogue Output	Left Channel Line Output
10	ROUT	Analogue Output	Right Channel Line Output
11	AVDD	Supply	Analogue VDD
12	AGND	Ground	Analogue GND
13	VMID	Analogue Output	Mid-rail reference decoupling point
14	MODE	Digital Input	Control Interface Selection, Pull up (when ACTIVE not set)
15	CSB	Digital Input	3-Wire MPU Chip Select / 2-Wire MPU interface address selection, active low, Pull up (when ACTIVE not set)
16	SDIN	Digital Input/Output	3-Wire MPU Data Input / 2-Wire MPU Data Input
17	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
18	MCLK	Digital Input	Master Clock Input (MCLK)
19	DCVDD	Supply	Digital Core VDD
20	DGND	Ground	Digital GND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+3.63V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. The digital supply core voltage (DCVDD) must always be less than or equal to the analogue supply voltage (AVDD).

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.42	1.5	3.6	V
Digital supply range (Buffer)	DBVDD		2.7	3.3	3.6	V
Analogue supply range	AVDD, HPVDD		2.7	3.3	3.6	V
Ground	DGND, AGND, HPGND			0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DBVDD	V
Input HIGH level	V_{IH}		0.7 x DBVDD			V
Output LOW	V_{OL}	I_{OL} = 1mA			0.1 x DBVDD	V
Output HIGH	V_{OH}	I_{OH}= -1mA	0.9 x DBVDD			V
Power On Reset Threshold (DCVDD)						
DCVDD Threshold On -> Off	V_{th}			0.9		V
Hysteresis	V_{IH}			0.3		V
DCVDD Threshold Off -> On	V_{OL}			0.6		V
Analogue Reference Levels						
Reference voltage (VMID)	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50k		Ω
Line Output for DAC Playback Only (Load = 10k Ω. 50pF)						
0dBfs Full scale output voltage		At LINE outputs		1.0 x AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,2)	SNR	A-weighted, @ fs = 48kHz	95	100		dB
		A-weighted @ fs = 96kHz		100		dB
		A-weighted, @ fs = 48kHz, AVDD = 2.7V		98		dB
Dynamic Range (Note 2)	DR	A-weighted, -60dB full scale input	85	100		dB
Total Harmonic Distortion	THD	1kHz, 0dBfs		-86	-80	dB
		1kHz, -3dBfs		-90		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
DAC channel separation		1kHz, 0dB		100		dB
Stereo Headphone Output						
0dB Full scale output voltage				1.0 x AVDD/3.3		Vrms
Max Output Power	P_O	RL = 32Ω		30		mW
		RL = 16Ω		55		
Signal to Noise Ratio (Note 1,2)	SNR	A-weighted	90	98		dB
Total Harmonic Distortion	THD	1kHz, R_L = 32 Ω @ P_O = 10mW rms (-5dB)		0.056 -65	0.1 -60	% dB
		1kHz, R_L = 32 Ω @ P_O = 20mW rms (-2dB)		0.56 -45	1.0 -40	
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Programmable Gain		1kHz	-73	6	6	dB
Programmable Gain Step Size		1kHz		1		dB
Mute attenuation		1kHz, 0dB		80		dB

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio of the rms values of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

POWER CONSUMPTION

MODE DESCRIPTION	POWEROFF	OUTPD	DACPD	CURRENT CONSUMPTION				
				AVDD (3.3V)	HPVDD (3.3V)	DCVDD (1.5V)	DBVDD (3.3V)	UNITS
DAC Playback	0	0	0	3.5	1.7	1.3	0.1	mA
Standby	0	1	1	17	0.4	0.7	0.2	µA
Power Down	1	1	1	0.4	0.3	0.7	0.1	µA

Table 1 Powerdown Mode Current Consumption Examples

Notes:

1. T_A = +25°C. Slave Mode, fs = 48kHz, MCLK = 256fs (12.288MHz).
2. All figures are quiescent, with no signal.
3. The power dissipation in the headphone itself not included in the above table.

MASTER CLOCK TIMING

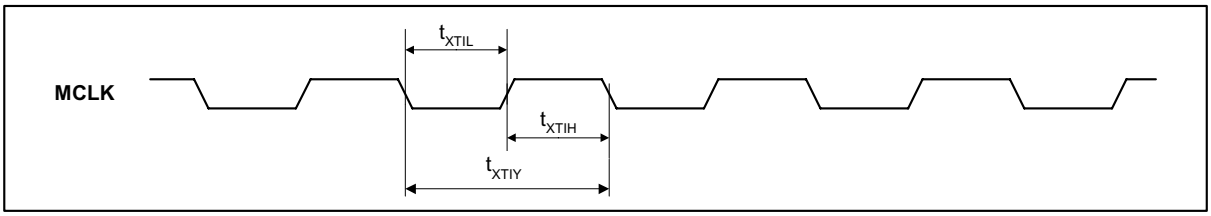


Figure 1 System Clock Timing Requirements

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK System clock pulse width high	t_{XTIH}		18			ns
MCLK System clock pulse width low	t_{XTIL}		18			ns
MCLK System clock cycle time	t_{XTIY}		54			ns
MCLK Duty cycle			40:60		60:40	

DIGITAL AUDIO INTERFACE – MASTER MODE

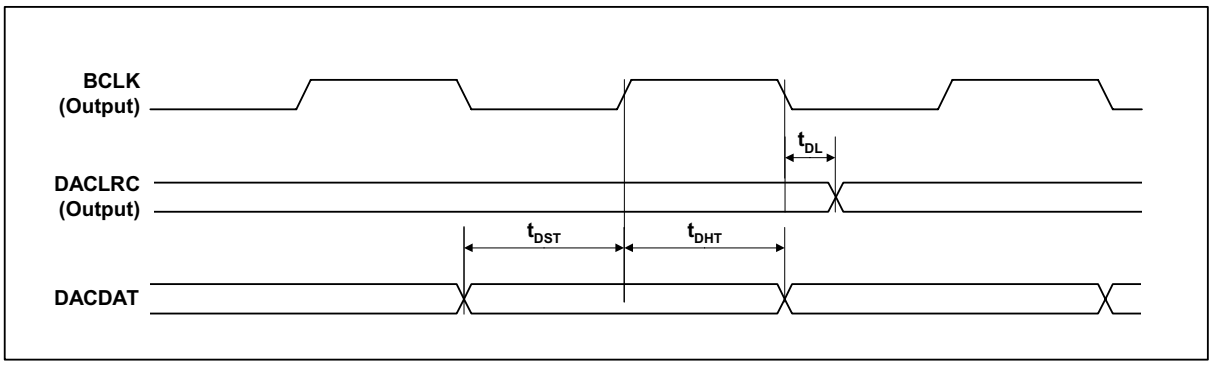


Figure 2 Digital Audio Data Timing - Master Mode

Test Conditions

AVDD, HPVDD, DVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
DACLRC propagation delay from BCLK falling edge	t_{DL}		0		10	ns
DACDAT setup time to BCLK rising edge	t_{DST}		10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}		10			ns

DIGITAL AUDIO INTERFACE – SLAVE MODE

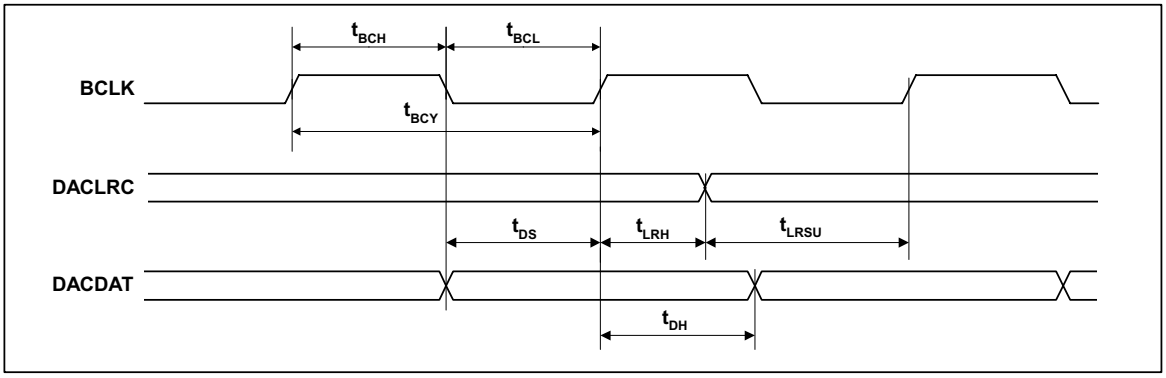


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD, HPVDD, DVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, slave mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
DACLRC set-up time to BCLK rising edge	t_{LRSU}		10			ns
DACLRC hold time from BCLK rising edge	t_{LRH}		10			ns
DACDAT set-up time to BCLK rising edge	t_{DS}		10			ns
DACDAT hold time from BCLK rising edge	t_{DH}		10			ns

MPU INTERFACE TIMING

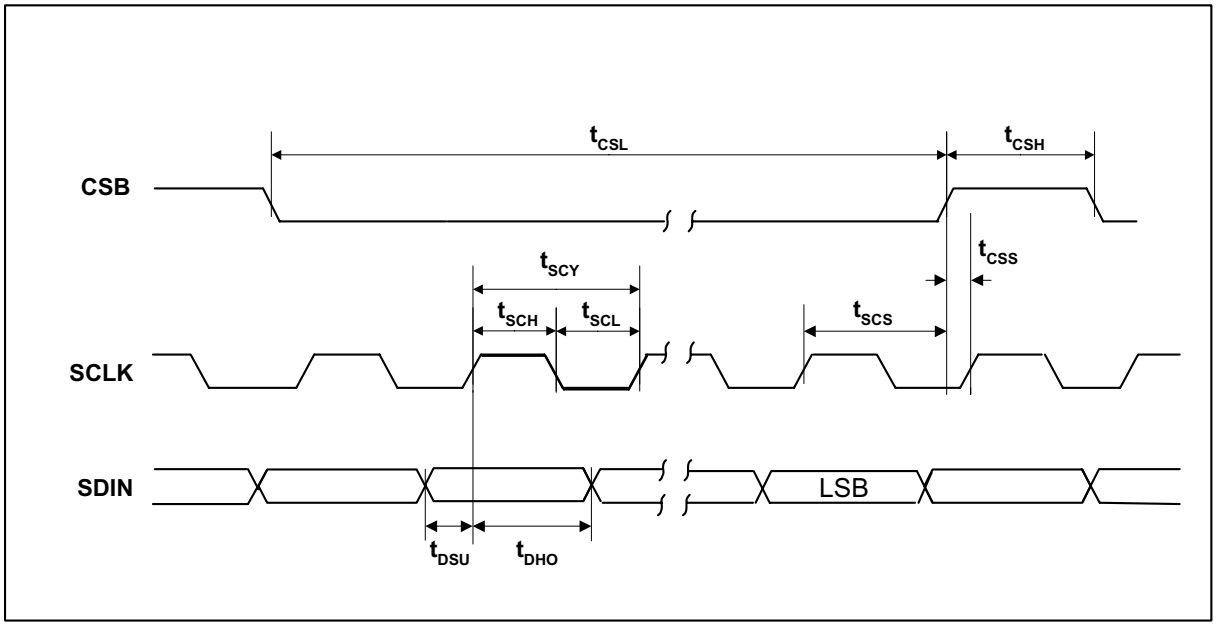


Figure 4 Program Register Input Timing - 3-Wire MPU Interface Timing

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK rising edge to CSB rising edge	t_{SCS}		60			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		20			ns
SCLK pulse width high	t_{SCH}		20			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
CSB pulse width low	t_{CSL}		20			ns
CSB pulse width high	t_{CSH}		20			ns
CSB rising to SCLK rising	t_{CSS}		20			ns

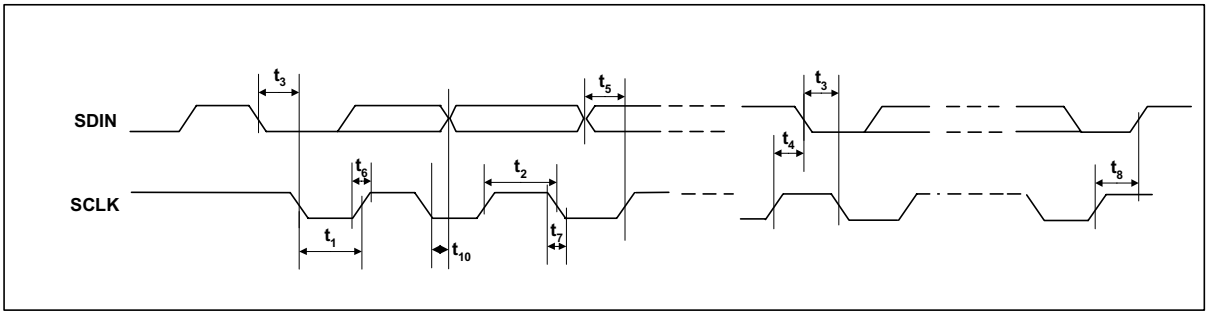


Figure 5 Program Register Input Timing – 2-Wire MPU Interface Timing

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK Frequency			0		400	kHz
SCLK Low Pulsewidth	t_1		600			ns
SCLK High Pulsewidth	t_2		1.3			us
Hold Time (Start Condition)	t_3		600			ns
Setup Time (Start Condition)	t_4		600			ns
Data Setup Time	t_5		100			ns
SDIN, SCLK Rise Time	t_6				300	ns
SDIN, SCLK Fall Time	t_7				300	ns
Setup Time (Stop Condition)	t_8		600			ns
Data Hold Time	t_{10}				900	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8721 is a low power audio DAC designed specifically for portable audio products. It's features, performance and low power consumption make it ideal for portable MP3, CD and mini-disc players.

The WM8721 includes line and headphone outputs from the on-board DAC, configurable digital audio interface and a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The on-board digital to analogue converter (DAC) accepts digital audio from the digital audio interface. Digital filter de-emphasis at 32kHz, 44.1kHz and 48kHz can be applied to the digital data under software control. The DAC employs a high quality multi-bit high-order oversampling architecture to deliver optimum performance with low power consumption.

The DAC outputs are available both at line level and through a headphone amplifier capable of efficiently driving low impedance headphones. The headphone output volume is adjustable in the analogue domain over a range of +6dB to –73dB and can be muted.

The design of the WM8721 minimises power consumption without compromising performance. It includes the ability to power off selective parts of the circuitry under software control, thus conserving power. Separate power save modes can be configured under software control including a standby and power off mode.

Special techniques allow the audio to be muted and the device safely placed into standby, sections of the device powered off, volume levels adjusted without any audible clicks, pops or zipper noises. Therefore standby and power off modes maybe used dynamically under software control, whenever playback is not required.

The device caters for a number of different sampling rates including industry standard 8kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz. The WM8721 has two schemes to support the programmable sample rates: Normal industry standard 256/384fs sampling mode may be used. A special USB mode is included, where all audio sampling rates can be generated from a 12.00MHZ USB clock. The digital filters used for playback are optimised for each sampling rate used.

The digital audio interface can support a range of audio data formats including I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified. The digital audio interface can operate in both master or slave modes.

The software control uses either a 2 or 3-wire MPU interface.

AUDIO SIGNAL PATH

DAC FILTERS

The DAC filters perform true 24 bit signal processing to convert the incoming digital audio data from the digital audio interface at the specified sample rate to multi-bit oversampled data for processing by the analogue DAC. Figure 6 illustrates the DAC digital filter path.

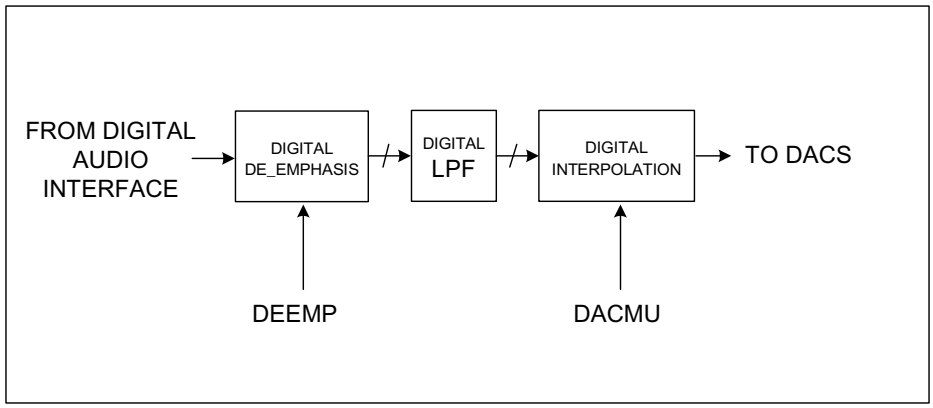


Figure 6 DAC Filter Schematic

The DAC digital filter can apply digital de-emphasis under software control, as shown in Table 2. The DAC can also perform a soft mute where the audio data is digitally brought to a mute level. This removes any abrupt step changes in the audio that might otherwise result in audible clicks in the audio outputs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000101 Digital Audio Path Control	2:1	DEEMP[1:0]	00	De-emphasis Control (Digital) 11 = 48kHz 10 = 44.1kHz 01 = 32kHz 00 = Disable
	3	DACMU	1	DAC Soft Mute Control (Digital) 1 = Enable soft mute 0 = Disable soft mute

Table 2 DAC Software Control

DAC

The WM8721 employs a multi-bit sigma delta oversampling digital to analogue converter. The scheme for the converter is illustrated Figure 7.

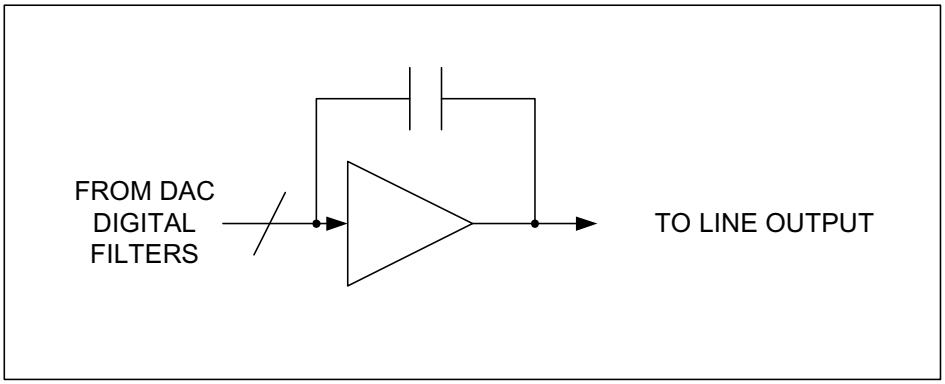


Figure 7 Multi-Bit Oversampling Sigma Delta Schematic

The DAC converts the multi-level digital audio data stream from the DAC digital filters into high quality analogue audio.

LINE OUTPUTS

The WM8721 provides two low impedance line outputs LOUT and ROUT, suitable for driving typical line loads of impedance 10K and capacitance 50pF.

The LOUT and ROUT outputs are only available at a line output level and are not level adjustable in the analogue domain, having a fixed gain of 0dB. The level is fixed such that at the DAC full scale level the output level is 1Vrms at AVDD = 3.3 volts. Note that the DAC full scale level tracks directly with AVDD. The scheme is shown in Figure 9. The line output includes a low order audio low pass filter for removing out-of band components from the sigma-delta DAC. Therefore no further external filtering is required in most applications.

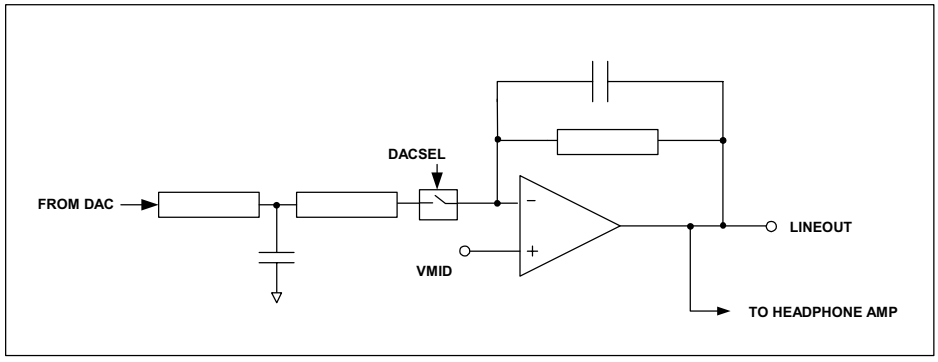


Figure 8 Line Output Schematic

The line output is muted by either programming the DACMU (digital) bit as per table 2, or by writing to the DACSEL (analogue) bit as per table 3. Whenever the DAC is muted or the device placed into standby mode the DC voltage is maintained at the line outputs to prevent any audible clicks from being present.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000100 Analogue Audio Path Control	4	DACSEL	0	DAC Select 1 = Select DAC 0 = Don't select DAC

Table 3 Output Software Control

The recommended external components are shown in Figure 9.

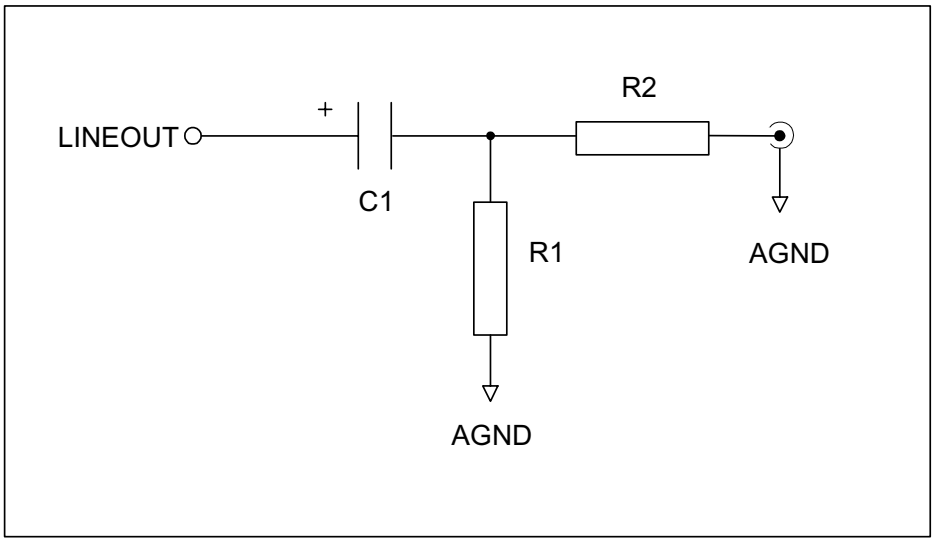


Figure 9 Line Outputs Application Drawing

Recommended values are C1 = 10µF, R1 = 47k, R2 = 100Ω

C1 forms a DC blocking capacitor to the line outputs. R1 prevents the output voltage from drifting so protecting equipment connected to the line output. R2 forms a de-coupling resistor preventing abnormal loads from disturbing the device. Note that poor choice of dielectric material for C1 can have dramatic effects on the measured signal distortion at the output.

HEADPHONE AMPLIFIER

The WM8721 has a stereo headphone output available on LHPOUT and RHPOUT. The output is designed specifically for driving 16 or 32Ω headphones with maximum efficiency and low power consumption. The headphone output includes a high quality volume level adjustment and mute function.

The scheme of the circuit is shown in Figure 10.

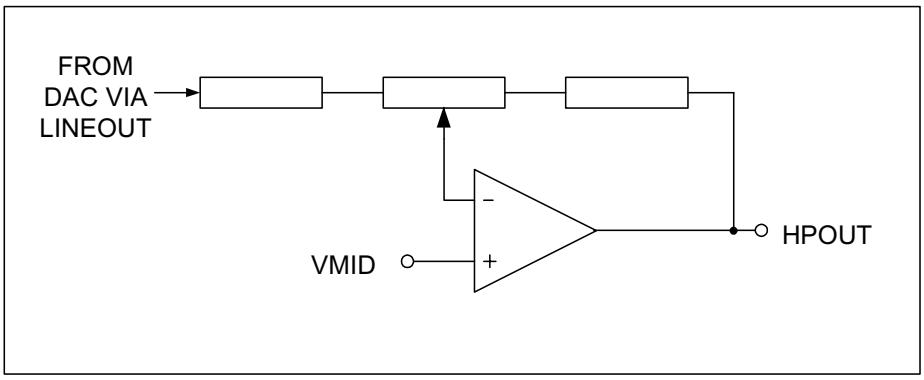


Figure 10 Headphone Amplifier Schematic

LHPOUT and RHPOUT volumes can be independently adjusted under software control using the LHPVOL[6:0] and RHPVOL[6:0] bits respectively of the headphone output control registers. The adjustment is logarithmic with an 80dB range in 1dB steps from +6dB to –73dB.

The headphone outputs can be separately muted by writing codes less than 0110000 to LHPVOL[6:0] or RHPVO[6:0]L bits. Whenever the headphone outputs are muted or the device placed into standby mode, the DC voltage is maintained at the line outputs to prevent any audible clicks from being present.

A zero cross detect circuit is provided at the input to the headphones under the control of the LZCEN and RZCEN bits of the headphone output control register. Using these controls the volume control values are only updated when the input signal to the gain stage is close to the analogue ground level. This minimises any audible clicks and zipper noise as the gain values are changed or the device muted. Note that this circuit has no time out so if only DC levels are being applied to the gain stage input of more than approximately 20mV, then the gain will not be updated. This zero cross function is enabled when the LZCEN and RZCEN bit is set high during a volume register write. If there is concern that a DC level may have blocked a volume change (one made with LZCEN or RZCEN set high) then a subsequent volume write of the same value, but with the LZCEN or RZCEN bit set low will force a volume update, regardless of the DC level.

LHPOUT and RHPOUT volume and zero-cross setting can be changed independently. Alternatively, the user can lock the two channels together, allowing both to be updated simultaneously, halving the number of serial writes required, provided that the same gain is needed for both channels. This is achieved through writing to the HPBOTH bit of the control register. Setting LRHPBOTH whilst writing to LHPVOL and LZCEN will simultaneously update the Right Headphone controls similarly. The corresponding effect on updating RLHPBOTH is also achieved.

The software control is given in Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000010 Left Headphone Out	6:0	LHPVOL[6:0]	1111001 (0dB)	Left Channel Headphone Output Volume Control 1111111 = +6dB . . 1dB steps down to 0110000 = -73dB 0000000 to 0101111 = MUTE
	7	LZCEN	0	Left Channel Zero Cross detect Enable 1 = Enable 0 = Disable
	8	LRHPBOTH	0	Left to Right Channel Headphone Volume, Mute and Zero Cross Data Load Control 1 = Enable Simultaneous Load of LHPVOL[6:0] and LZCEN to RHPVOL[6:0] and RZCEN 0 = Disable Simultaneous Load
0000011 Right Headphone Out	6:0	RHPVOL[6:0]	1111001 (0dB)	Right Channel Headphone Output Volume Control 1111111 = +6dB . . 1dB steps down to 0110000 = -73dB 0000000 to 0101111 = MUTE
	7	RZCEN	0	Right Channel Zero Cross Detect Enable 1 = Enable 0 = Disable
	8	RLHPBOTH	0	Right to Left Channel Headphone Volume, Mute and Zero Cross Data Load Control 1 = Enable Simultaneous Load of RHPVOL[6:0] and RZCEN to LHPVOL[6:0] and LZCEN 0 = Disable Simultaneous Load

Table 4 Headphone Output Software Control

The recommended external components required to complete the application are shown in Figure 11.

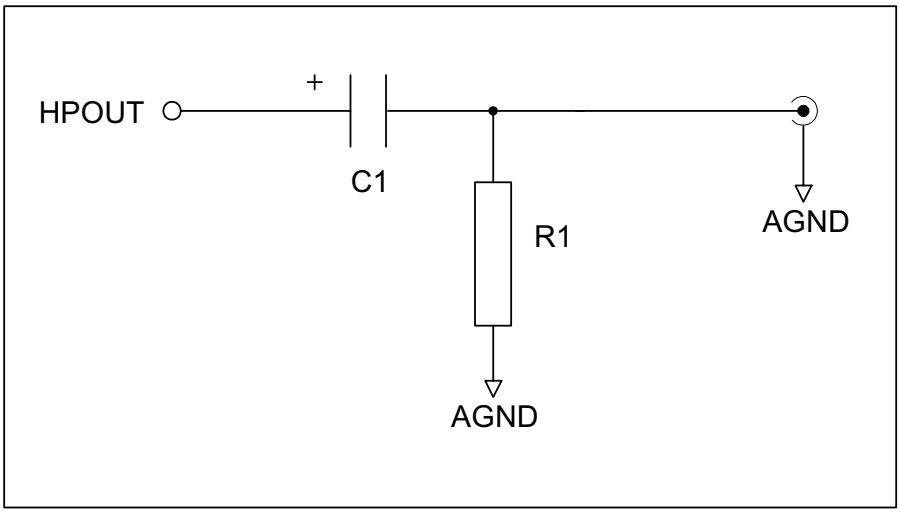


Figure 11 Headphone Output Application Drawing

Recommended values are C1 = 220uF (10V electrolytic), R1 = 47k

C1 forms a DC blocking capacitor to isolate the dc of the HPOUT from the headphones. R1 form a pull down resistor to discharge C1 to prevent the voltage at the connection to the headphones from rising to a level that may damage the headphones.

DEVICE OPERATION

DEVICE RESETTING

The WM8721 contains a power on reset circuit that resets the internal state of the device to a known condition. The power on reset is applied as DCVDD powers on and released only after the voltage level of DCVDD crosses a minimum turn off threshold. If DCVDD later falls below a minimum turn on threshold voltage then the power on reset is re-applied. The threshold voltages and associated hysteresis are shown in the Electrical Characteristics table.

The user also has the ability to reset the device to a known state under software control as shown in the table below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001111 Reset Register	8:0	RESET	not reset	Reset Register Writing 000000000 to register resets device

Table 5 Software Control of Reset

When using the software reset. In 3-wire mode the reset is applied on the rising edge of CSB and released on the next rising edge of SCLK. In 2-wire mode the reset is applied for the duration of the ACK signal (approximately 1 SCLK period, refer to Figure 19).

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin with no software configuration necessary.

Note that on the WM8721, MCLK is used to derive clocks for the DAC path. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

CORE CLOCK

The WM8721 DSP core can be clocked either by MCLK or MCLK divided by 2. This is controlled by software as shown in Table 6 below.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001000 Sampling Control	6	CLKIDIV2	0	Core Clock divider select 1 = Core Clock is MCLK divide by 2 0 = Core Clock is MCLK

Table 6 Software Control of Core Clock

Having a programmable MCLK divider allows the device to be used in applications where higher frequency master Clocks are available. For example the device can support 512fs master clocks whilst fundamentally operating in a 256fs mode.

DIGITAL AUDIO INTERFACES

WM8721 may be operated in either one of the 4 offered audio interface modes. These are:

- Right justified
- Left justified
- I^2S
- DSP mode

All four of these modes are MSB first and operate with data 16 to 32 bits, except in right justified mode where 32 bit data is not supported.

The digital audio interface receives the digital audio data for the internal DAC digital filters on the DACDAT input. DACDAT is the formatted digital audio data stream output to the DAC digital filters with left and right channels multiplexed together. DACLRC is an alignment clock that controls whether Left or Right channel data is present on DACDAT. DACDAT and DACLRC are synchronous with the BCLK signal with each data bit transition signified by a BCLK high to low transition. DACDAT is always an input. BCLK and DACLRC are either outputs or inputs depending whether the device is in master or slave mode. Refer to the MASTER/SLAVE OPERATION section

There are four digital audio interface formats accommodated by the WM8721. These are shown in the figures below. Refer to the Electrical Characteristic section for timing information.

Left Justified mode is where the MSB is available on the first rising edge of BCLK following a DACLRC transition.

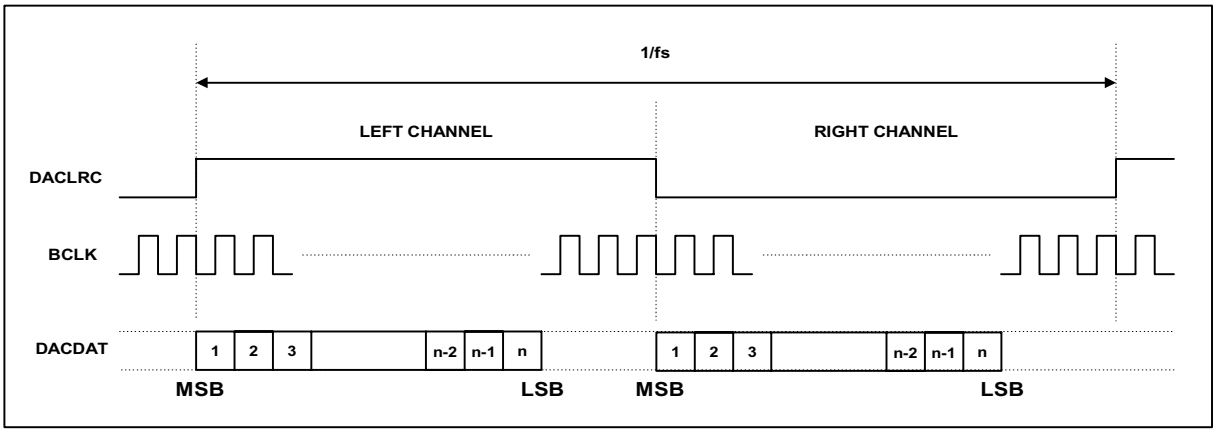


Figure 12 Left Justified Mode

I^2S mode is where the MSB is available on the 2nd rising edge of BCLK following a DACLRC transition.

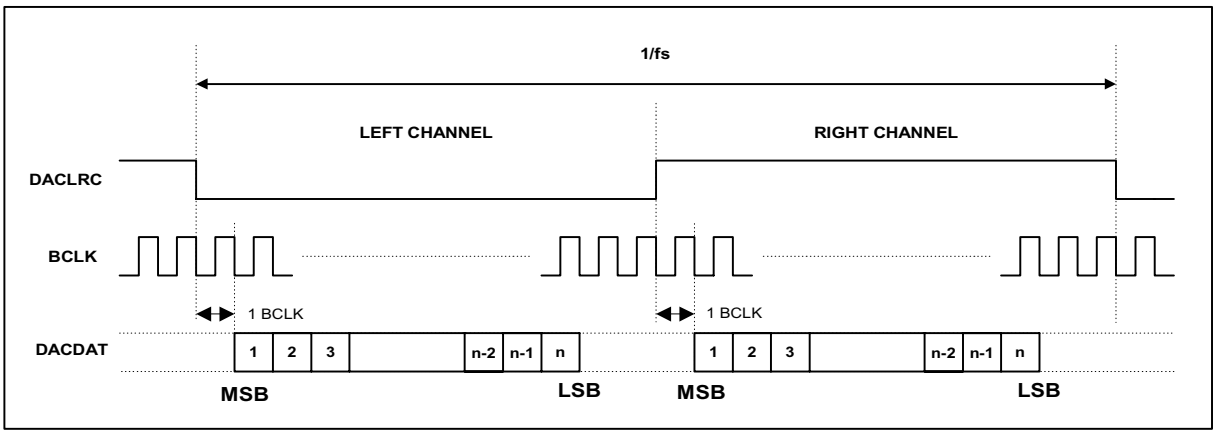


Figure 13 I^2S Mode

Right Justified mode is where the LSB is available on the rising edge of BCLK preceding a DACLRC transition, yet MSB is still transmitted first.

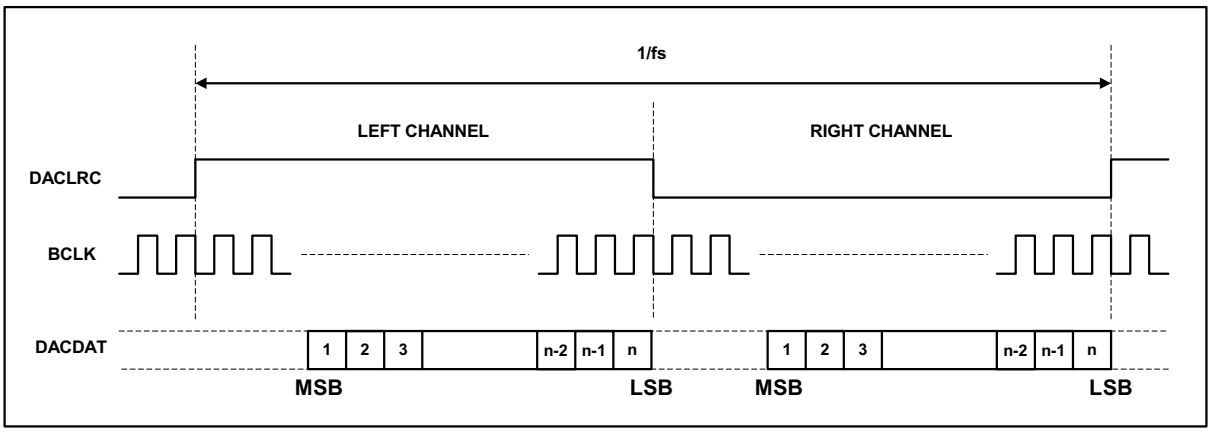


Figure 14 Right Justified Mode

DSP mode is where the left channel MSB is available on either the 1st or 2nd rising edge of BCLK (selectable by LRP) following a DACLRC transition high. Right channel data immediately follows left channel data.

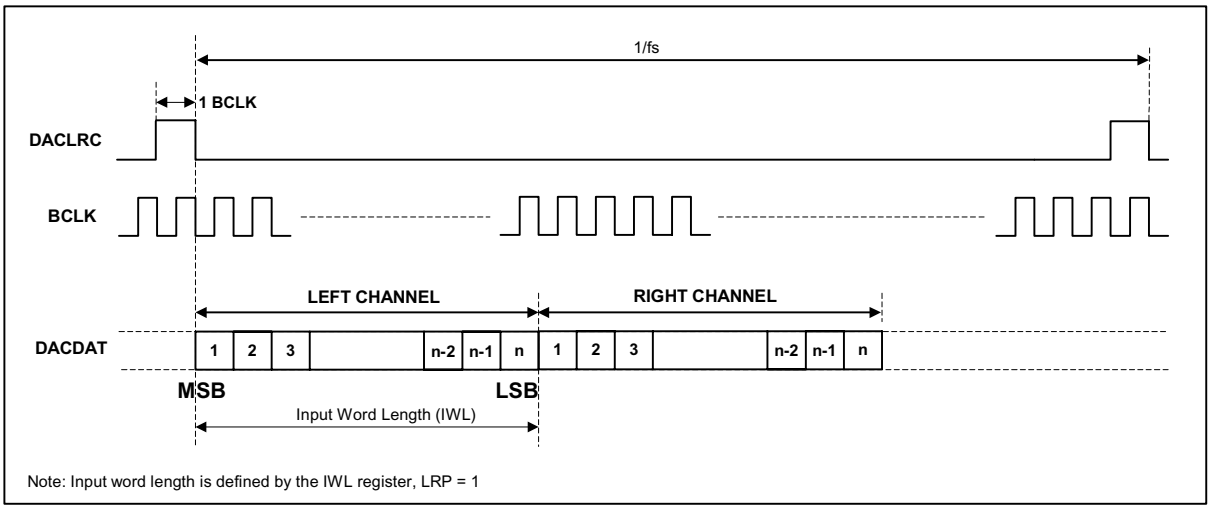


Figure 15 DSP Mode

In all modes DACLRC must always change on the falling edge of BCLK, refer to Figure 12, Figure 13, Figure 14 and Figure 15.

Operating the digital audio interface in DSP mode allows ease of use for supporting the various sample rates and word lengths. The only requirement is that all data is transferred within the correct number of BCLK cycles to suit the chosen word length.

In order for the digital audio interface to offer similar support in the three other modes (Left Justified, I^2S and Right Justified), the DACLRC and BCLK frequencies, continuity and mark-space ratios need more careful consideration.

In Slave mode, DACLRC inputs are not required to have a 50:50 mark-space ratio. BCLK input need not be continuous. It is however required that there are sufficient BCLK cycles for each DACLRC transition to clock the chosen data word length. The non-50:50 requirement on the DACLRC is of use in some situations such as with a USB 12MHz clock. Here simply dividing down a 12MHz clock within the DSP to generate DACLRC and BCLK will not generate the appropriate DACLRC since it will no longer change on the falling edge of BCLK. For example, with 12MHz/32k fs mode there are 375 MCLK per DACLRC. In these situations DACLRC can be made non 50:50.

In Master mode, DACLRC will be output with a 50:50 mark-space ratio with BCLK output at 64fs x base frequency (ie 48kHz). The exception again is in USB mode where BCLK is always 12MHz. So for example in 12MHz/32k fs mode there are 375 master clocks per DACLRC period. Therefore the DACLRC output will have a mark space ratio of 187:188.

The DAC digital audio interface modes are software configurable as indicated in Table 7. Note that dynamically changing the software format may result in erroneous operation of the interfaces and is therefore not recommended.

The length of the digital audio data is programmable at 16/20/24 or 32 bits. Refer to the software control table below. The data is signed 2's complement. The DAC digital filters process data using 24 bits. If the DAC is programmed to receive 16 or 20 bit data, the WM8721 packs the LSBs with zeros. If the DAC is programmed to receive 32 bit data, then it strips the LSBs.

The DAC outputs can be swapped under software control using LRP and LRSWAP as shown in Table 7. Stereo samples are normally generated as a Left/Right sampled pair. LRSWAP reverses the order so that a Left sample goes to the right DAC output and a Right sample goes to the left DAC output. LRP swaps the phasing so that a Right/Left sampled pair is expected and preserves the correct channel phase difference, except in DSP mode, where LRP controls the positioning of the MSB relative to the rising edge of DACLRC.

DACDAT is always an input. It is expected to be set low by the audio interface controller when the WM8721 is powered off or in standby.

DACLRC and BCLK can be either outputs or inputs depending on whether the device is configured as a master or slave. If the device is a master then the DACLRC and BCLK signals are outputs that default low. If the device is a slave then the DACLRC and BCLK are inputs. It is expected that these are set low by the audio interface controller when the WM8721 is powered off or in standby.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000111 Digital Audio Interface Format	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode, frame sync + 2 data packed words 10 = I^2S Format, MSB-First left-1 justified 01 = MSB-First, left justified 00 = MSB-First, right justified
	3:2	IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	4	LRP	0	DACLRC phase control (in left, right or I^2S modes) 1 = Right Channel DAC data when DACLRC high 0 = Right Channel DAC data when DACLRC low (opposite phasing in I^2S mode) *or* DSP mode A/B select (in DSP mode only) 1 = MSB is available on 2nd BCLK rising edge after DACLRC rising edge 0 = MSB is available on 1st BCLK rising edge after DACLRC rising edge
	5	LRSWAP	0	DAC Left Right Clock Swap 1 = Right Channel DAC Data Left 0 = Right Channel DAC Data Right
	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	7	BCLKINV	0	Bit Clock Invert 1 = Invert BCLK 0 = Don't invert BCLK

Table 7 Digital Audio Interface Control

Note: If right justified 32 bit mode is selected then the WM8721 defaults to 24 bits.

MASTER AND SLAVE MODE OPERATION

The WM8721 can be configured as either a master or slave mode device. As a master mode device the WM8721 controls sequencing of the data and clocks on the digital audio interface. As a slave device the WM8721 responds with data to the clocks it receives over the digital audio interface. The mode is set with the MS bit of the control register as shown in Table 8.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000111 Digital Audio Interface Format	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode

Table 8 Programming Master/Slave Modes

As a master mode device the WM8721 controls the sequencing of data transfer (DACDAT) and output of clocks (BCLK, DACLRC) over the digital audio interface. It uses the timing generated from the MCLK input as the reference for the clock and data transitions. This is illustrated in Figure 16. DACDAT is always an input to the WM8721 independent of master or slave mode.

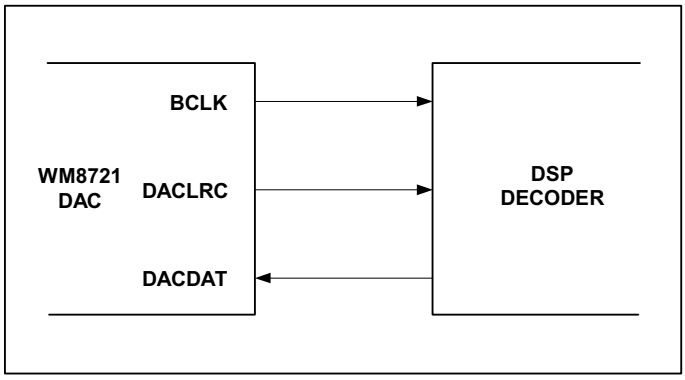


Figure 16 Master Mode

As a slave device the WM8721 sequences the data transfer (DACDAT) over the digital audio interface in response to the external applied clocks (BCLK, DACLRC). This is illustrated in Figure 17.

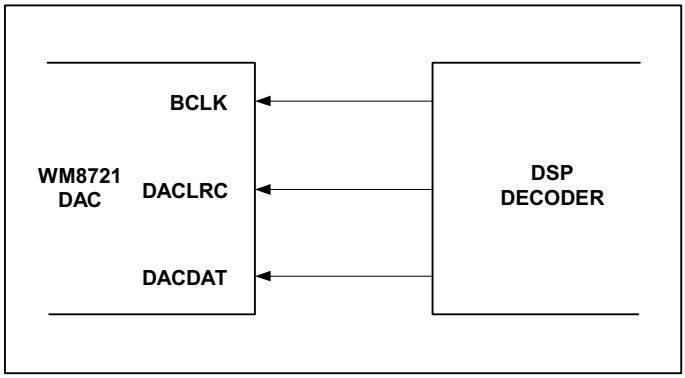


Figure 17 Slave Mode

Note that the WM8721 relies on controlled phase relationships between audio interface BCLK, DACLRC and the master MCLK. To avoid any timing hazards, refer to the timing section for detailed information.

AUDIO DATA SAMPLING RATES

The WM8721 provides for two modes of operation (normal and USB) to generate the required DAC sampling rates. Normal and USB modes are programmed under software control according to the table below.

In Normal mode, the user controls the sample rate by using an appropriate MCLK frequency and the sample rate control register setting. The WM8721 can support sample rates from 8ks/s up to 96ks/s.

In USB mode, the user must use a fixed MLCK frequency of 12MHz to generate sample rates from 8ks/s to 96ks/s. It is called USB mode since the common USB (Universal Serial Bus) clock is at 12MHz and the WM8721 can be directly used within such systems. WM8721 can generate all the normal audio sample rates from this one Master Clock frequency, removing the need for different master clocks or PLL circuits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION	
0001000 Sampling Control	0	USB/ NORMAL	0	Mode Select 1 = USB mode (250/272fs) 0 = Normal mode (256/384fs)	
	1	BOSR	0	Base Over-Sampling Rate	
				USB Mode 0 = 250fs 1 = 272fs	Normal Mode 96/88.2 kHz 0 = 256fs 0 = 128fs 1 = 384fs 1 = 192fs
	5:2	SR[3:0]	0000	DAC sample rate control; See USB Mode and Normal Mode Sample Rate sections for operation	

Table 9 Sample Rate Control

NORMAL MODE SAMPLE RATES

In normal mode MCLK is set up according to the desired sample rates of the DAC. For DAC sampling rates of 8, 32, 48 or 96kHz, MCLK frequencies of either 12.288MHz (256fs) or 18.432MHz (384fs) can be used. DAC sampling rates of 8, 44.1 or 88.2kHz from MCLK frequencies of either 11.2896MHz (256fs) or 16.9344MHz (384fs) can be used.

The table below should be used to set up the device to work with the various sample rate combinations. Refer to Digital Filter Characteristics section for an explanation of the different filter types.

SAMPLING RATE DAC	MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
KHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	12.288	0 (256fs)	0	0	0	0	1
	18.432	1 (384fs)	0	0	0	0	
8	12.288	0 (256fs)	0	0	0	1	1
	18.432	1 (384fs)	0	0	0	1	
32	12.288	0 (256fs)	0	1	1	0	1
	18.432	1 (384fs)	0	1	1	0	
96	12.288	0 (128fs)	0	1	1	1	2
	18.432	1 (192fs)	0	1	1	1	
44.1	11.2896	0 (256fs)	1	0	0	0	1
	16.9344	1 (384fs)	1	0	0	0	
8 (Note 1)	11.2896	0 (256fs)	1	0	0	1	1
	16.9344	1 (384fs)	1	0	0	1	
88.2	11.2896	0 (128fs)	1	1	1	1	2
	16.9344	1 (192fs)	1	1	1	1	

Table 10 Normal Mode Sample Rate Look-up Table

Notes:

1. 8k not exact, actual = 8.018kHz

2. All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

The BOSR bit represents the base over-sampling rate. This is the rate that the WM8721 digital signal processing is carried out at. In Normal mode, with BOSR = 0, the base over-sampling rate is at 256fs, with BOSR = 1, the base over-sampling rate is at 384fs. This can be used to determine the actual audio data rate required by the DAC.

The exact sample rates achieved are defined by the relationships in Table 11 below.

TARGET SAMPLING RATE	ACTUAL SAMPLING RATE			
	BOSR=0		BOSR=1	
	MCLK=12.288	MCLK=11.2896	MCLK=18.432	MCLK=16.9344
kHz	kHz	kHz	kHz	kHz
8	8	8.018	8	8.018
	(12.288MHz/256) x 1/6	(11.2896MHz/256) x 2/11	(18.432MHz/384) x 1/6	(16.9344MHz/384) x 2/11
32	32	*not available*	32	*not available*
	(12.288MHz/256) x 2/3		(18.432MHz/384) x 2/3	
44.1	*not available*	44.1	*not available*	44.1
		11.2896MHz/256		16.9344MHz /384
48	48	*not available*	48	*not available*
	12.288MHz/256		18.432MHz/384	
88.2	*not available*	88.2	*not available*	88.2
		(11.2896MHz/256) x 2		(16.9344MHz /384) x 2
96	96	*not available*	96	*not available*
	(12.288MHz/256) x 2		(18.432MHz/384) x 2	

Table 11 Normal Mode Actual Sample Rates

128/192FS NORMAL MODE

The Normal Mode sample rates are designed for standard 256fs and 384fs MCLK rates. However the WM8721 is also capable of being clocked from a 128/192fs MCLK for application over limited sampling rates as shown in the table below.

SAMPLING RATE		MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
ADC	DAC							
kHz	kHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	48	6.144	0	0	1	1	1	2
		9.216	1	0	1	1	1	
44.1	44.1	5.6448	0	1	1	1	1	2
		8.4672	1	1	1	1	1	

Table 12 128/192fs Normal Mode Sample Rate Look-up Table

512/768fs NORMAL MODE

512 fs and 768 fs MCLK rates can be accommodated by using the CLKIDIV2 bir (register 8, bit 6). The core clock to the DSP will be divided by 2 so an external 512/768fs MCLK will become 256/384 fs internally and the device otherwise operates as in Table 9 but with MCLK at twice the specified rate.

USB MODE SAMPLE RATES

In USB mode the MCLK input is 12MHz only.

SAMPLING RATE DAC	MCLK FREQUENCY	SAMPLE RATE REGISTER SETTINGS					DIGITAL FILTER TYPE
kHz	MHz	BOSR	SR3	SR2	SR1	SR0	
48	12.000	0	0	0	0	0	0
44.1 (Note 2)	12.000	1	1	0	0	0	1
8	12.000	0	0	0	0	1	0
8 (Note 1)	12.000	1	1	0	0	1	1
32	12.000	0	0	1	1	0	0
96	12.000	0	0	1	1	1	3
88.2 (Note 3)	12.000	1	1	1	1	1	2

Table 13 USB Mode Sample Rate Look-up Table

Notes:

1. 8k not exact, actual = 8.021kHz
2. 44.1k not exact, actual = 44.118kHz
3. 88.1k not exact, actual = 88.235kHz
4. All other combinations of BOSR and SR[3:0] that are not in the truth table are invalid

The BOSR bit represents the base over-sampling rate. This is the rate that the WM8721 digital signal processing is carried out at and the sampling rate will always be a sub-multiple of this. In USB mode, with BOSR = 0, the base over-sampling rate is defined at 250fs, with BOSR = 1, the base over-sampling rate is defined at 272fs. This can be used to determine the actual audio sampling rate required by the DAC.

The exact sample rates supported for all combinations are defined by the relationships in Table 14 below.

TARGET SAMPLING RATE	ACTUAL SAMPLING RATE	
	BOSR=0 (250fs)	BOSR=1 (272fs)
kHz	kHz	kHz
8	8	8.021
	12MHz/(250 x 48/8)	12MHz/(272 x 11/2)
32	32	*not available*
	12MHz/(250 x 48/32)	
44.1	*not available*	44.118
		12MHz/272
48	48	*not available*
	12MHz/250	
88.2	*not available*	88.235
		12MHz/136
96	96	*not available*
	12MHz/125	

Table 14 USB Mode Actual Sample Rates

ACTIVATING DSP AND DIGITAL AUDIO INTERFACE

To prevent any communication problems from arising across the Digital Audio Interface it is disabled (tristate) at power on. Once the Audio Interface and the Sampling Control has been programmed it is activated by setting the ACTIVE bit under Software Control.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 Active Control	0	ACTIVE	0	Activate Interface 1 = Active 0 = Inactive

Table 15 Activating DSP and Digital Audio Interface

It is recommended that between changing any content of Digital Audio Interface or Sampling Control Register that the active bit is reset then set.

SOFTWARE CONTROL INTERFACE

The software control interface may be operated using either a 3-wire or 2-wire MPU interface. Selection of interface format is achieved by setting the state of the MODE pin.

In 3-wire mode, SDIN is used for the program data, SCLK is used to clock in the program data and CSB is used to latch in the program data. In 2-wire mode, SDIN is used for serial data and SCLK is used for the serial clock. In 2-wire mode, the state of CSB pin allows the user to select one of two addresses.

Unused bits in the Register Map should be set to '0' unless specified otherwise (see Powerdown section).

SELECTION OF SERIAL CONTROL MODE

The serial control interface may be selected to operate in either 2 or 3-wire modes. This is achieved by setting the state of the MODE pin.

MODE	INTERFACE FORMAT
0	2 wire
1	3 wire

Table 16 Control Interface Mode Selection

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

The WM8721 can be controlled using a 3-wire serial interface. SDIN is used for the program data, SCLK is used to clock in the program data and CSB is use to latch in the program data. The 3-wire interface protocol is shown in Figure 18.

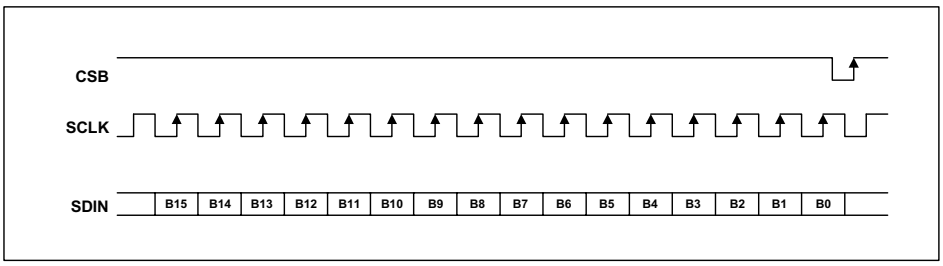


Figure 18 3-Wire Serial Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits
3. CSB is edge sensitive not level sensitive. The data is latched on the rising edge of CSB

2-WIRE SERIAL CONTROL MODE

The WM8721 supports a 2-wire MPU serial interface. The device operates as a slave device only. The WM8721 has one of two slave addresses that are selected by setting the state of pin 15 (SSOP) / 26 (QFN), (CSB).

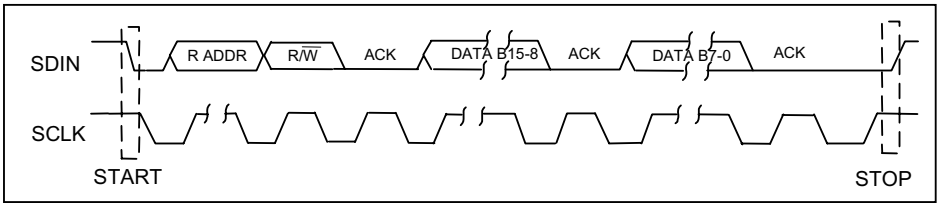


Figure 19 2-Wire Serial Interface

Notes:

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

CSB STATE	Address
0	0011010
1	0011011

Table 17 2-Wire MPU Interface Address Selection

To control the WM8721 on the 2-wire bus the master control device must initiate a data transfer by establishing a start condition, defined by a high to low transition on SDIN while SCLK remains high. This indicates that an address and data transfer will follow. All peripherals on the 2-wire bus respond to the start condition and shift in the next eight bits (7-bit address + R/W bit). The transfer is MSB first. The 7-bit address consists of a 6-bit base address + a single programmable bit to select one of two available addresses for this device (see Table 17). If the correct address is received and the R/W bit is '0', indicating a write, then the WM8721 will respond by pulling SDIN low on the next clock pulse (ACK). The WM8721 is a write only device and will only respond to the R/W bit indicating a write. If the address is not recognised the device will return to the idle condition and wait for a new start condition and valid address.

Once the WM8721 has acknowledged a correct address, the controller will send eight data bits (bits B15-B8). WM8721 will then acknowledge the sent data by pulling SDIN low for one clock pulse. The controller will then send the remaining eight data bits (bits B7-B0) and the WM8721 will then acknowledge again by pulling SDIN low.

A stop condition is defined when there is a low to high transition on SDIN while SCLK is high. If a start or stop condition is detected out of sequence at any point in the data transfer then the device will jump to the idle condition.

After receiving a complete address and data sequence the WM8721 returns to the idle state and waits for another start condition. Each write to a register requires the complete sequence of start condition, device address and R/W bit followed by the 16 register address and data bits.

POWER DOWN MODES

The WM8721 contains power conservation modes in which various circuit blocks may be safely powered down in order to conserve power. This is software programmable as shown in Table 18.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000110 Power Down Control	3	DACPD	1	DAC Power Down 1 = Enable Power Down 0 = Disable Power Down
	4	OUTPD	1	Line Output Power Down 1 = Enable Power Down 0 = Disable Power Down
	7	POWEROFF	1	Power Off Device 1 = Device Power Off 0 = Device Power On

Table 18 Power Conservation Modes Software Control

Note:

When writing to register 0000110 bits 5 and 6 should be set to 1.

The power down control can be used to either a) permanently disable functions when not required in certain applications or b) to dynamically power up and down functions depending on the operating mode, e.g.: during playback or pause. Please follow the special instructions below if dynamic implementations are being used.

DACPD: Powers down the DAC and DAC Digital Filters. If this is done dynamically then audible pops will result unless the following guidelines are followed. In order to prevent pops, the DAC should first be soft-muted (DACMU), the output should then be de-selected from the line and headphone output (DACSEL), then the DAC powered down (DACPD). This is of use when the device enters Pause or Stop modes.

OUTPD: Powers down the Line Headphone Output. If this is done dynamically then audible pops may result unless the DAC is first soft-muted (DACMU). This is of use when the device enters Pause or Stop modes.

The device can be put into a standby mode (STANDBY) by powering down all the audio circuitry under software control by setting DACPD and OUTPD, but not setting POWEROFF.

In STANDBY mode the Control Interface, a small portion of the digital and areas of the analogue circuitry remain active. The active analogue includes the analogue VMID reference so that the analogue line outputs and headphone outputs remain biased to VMID. This reduces any audible effects caused by DC glitches when entering or leaving STANDBY mode.

The device can be powered off by writing to the POWEROFF bit of the Power Down register. In POWEROFF mode the Control Interface and a small portion of the digital remain active. The analogue VMID reference is disabled.

REGISTER MAP

The complete register map is shown in Table 21. The detailed description can be found in the relevant text of the device description. There are 9 registers with 9 bits per register. These can be controlled using either the 2 wire or 3 wire MPU interface.

REGISTER	B 15	B 14	B 13	B 12	B 11	B 10	B 9	B8	B7	B6	B5	B4	B3	B2	B1	B0
R2 (04h)	0	0	0	0	0	1	0	LRHP BOTH	LZCEN	LHPVOL						
R3 (06h)	0	0	0	0	0	1	1	RLHP BOTH	RZCEN	RHPVOL						
R4 (08h)	0	0	0	0	1	0	0	0	0	0	0	DAC SEL	0	0	0	0
R5 (0Ah)	0	0	0	0	1	0	1	0	0	0	0	0	DAC MU	DEEMPH		0
R6 (0Ch)	0	0	0	0	1	1	0	0	POWER OFF	1	1	OUTPD	DACPD	1	1	1
R7 (0Eh)	0	0	0	0	1	1	1	0	BCLK INV	MS	LR SWAP	LRP	IWL		FORMAT	
R8 (10h)	0	0	0	1	0	0	0	0	0	CLKI DIV2	SR				BOSR	USB/ NORM
R9 (12h)	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	ACTIVE
R15(1Eh)	0	0	0	1	1	1	1	RESET								
	ADDRESS							DATA								

Table 19 Mapping of Program Registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000010 Left Headphone Out	6:0	LHPVOL [6:0]	1111001 (0dB)	Left Channel Headphone Output Volume Control 1111111 = +6dB . . 1dB steps down to 0110000 = -73dB 0000000 to 0101111 = MUTE
	7	LZCEN	0	Left Channel Zero Cross detect Enable 1 = Enable 0 = Disable
	8	LRHPBOTH	0	Left to Right Channel Headphone Volume, Mute and Zero Cross Data Load Control 1 = Enable Simultaneous Load of LHPVOL[6:0] and LZCEN to RHPVOL[6:0] and RZCEN 0 = Disable Simultaneous Load

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Right Headphone Out	6:0	RHPVOL [6:0]	1111001 (0dB)	Right Channel Headphone Output Volume Control 1111111 = +6dB . . 1dB steps down to 0110000 = -73dB 0000000 to 0101111 = MUTE
	7	RZCEN	0	Right Channel Zero Cross detect Enable 1 = Enable 0 = Disable
	8	RLHPBOTH	0	Right to Left Channel Headphone Volume, Mute and Zero Cross Data Load Control 1 = Enable Simultaneous Load of RHPVOL[6:0] and RZCEN to LHPVOL[6:0] and LZCEN 0 = Disable Simultaneous Load
0000100 Audio Path Control	4	DACSEL	0	DAC Select (Analogue) 1 = Select DAC 0 = Don't select DAC
0000101 Digital Audio Path Control	2:1	DEEMP[1:0]	00	De-emphasis Control (Digital) 11 = 48kHz 10 = 44.1kHz 01 = 32kHz 00 = Disable
	3	DACMU	1	DAC Soft Mute Control (Digital) 1 = Enable soft mute 0 = Disable soft mute
0000110 Power Down Control	3	DACPD	1	DAC Power Down 1 = Enable Power Down 0 = Disable Power Down
	4	OUTPD	1	Outputs Power Down 1 = Enable Power Down 0 = Disable Power Down
	7	POWEROFF	1	POWEROFF mode 1 = Enable POWEROFF 0 = Disable POWEROFF

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000111 Digital Audio Interface Format	1:0	FORMAT[1:0]	10	Audio Data Format Select 11 = DSP Mode, frame sync + 2 data packed words 10 = I^2S Format, MSB-First left-1 justified 01 = MSB-First, left justified 00 = MSB-First, right justified
	3:2	IWL[1:0]	10	Input Audio Data Bit Length Select 11 = 32 bits 10 = 24 bits 01 = 20 bits 00 = 16 bits
	4	LRP	0	DACLRC phase control (in left, right or I^2S modes) 1 = Right Channel DAC data when DACLRC high 0 = Right Channel DAC data when DACLRC low (opposite phasing in I^2S mode) *or* DSP mode A/B select (in DSP mode only) 1 = MSB is available on 2nd BCLK rising edge after DACLRC rising edge 0 = MSB is available on 1st BCLK rising edge after DACLRC rising edge
	5	LRSWAP	0	DAC Left Right Clock Swap 1 = Right Channel DAC Data Left 0 = Right Channel DAC Data Right
	6	MS	0	Master Slave Mode Control 1 = Enable Master Mode 0 = Enable Slave Mode
	7	BCLKINV	0	Bit Clock Invert 1 = Invert BCLK 0 = Don't invert BCLK
0001000 Sampling Control	0	USB/ NORMAL	0	Mode Select 1 = USB mode (250/272fs) 0 = Normal mode (256/384fs)
	1	BOSR	0	Base Over-Sampling Rate USB Mode: 0 = 250fs, 1 = 272fs Normal Mode: 0 = 256fs, 1 = 384fs
	5:2	SR[3:0]	0000	DAC sample rate control; See USB Mode and Normal Mode Sample Rate sections for operation
	6	CLKIDIV2	0	Core Clock divider select 1 = Core Clock is MCLK divide by 2 0 = Core Clock is MCLK
0001001 Active Control	0	ACTIVE	0	Activate Interface 1 = Active 0 = Inactive
0001111 Reset Register	8:0	RESET	not reset	Reset Register Writing 00000000 to register resets device

Table 20 Register Map Description

Note: All other bits not explicitly defined in the register table should be set to zero unless specified otherwise (see Powerdown section).

DIGITAL FILTER CHARACTERISTICS

The DAC employs different digital filters. There are 4 types of digital filter, called Type 0, 1, 2 and 3. The performance of Types 0 and 1 is listed in the table below, the responses of all filters is shown in the proceeding pages.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Filter Type 0 (USB mode, 250fs operation)					
Passband	+/- 0.03dB	0		0.416fs	
	-6dB		0.5fs		
Passband Ripple				+/-0.03	dB
Stopband		0.584fs			
Stopband Attenuation	f > 0.584fs	-50			dB
DAC Filter Type 1 (USB mode, 272fs or Normal mode operation)					
Passband	+/- 0.03dB	0		0.4535fs	
	-6dB		0.5fs		
Passband Ripple				+/- 0.03	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-50			dB

Table 21 Digital Filter Characteristics

DAC FILTER RESPONSES

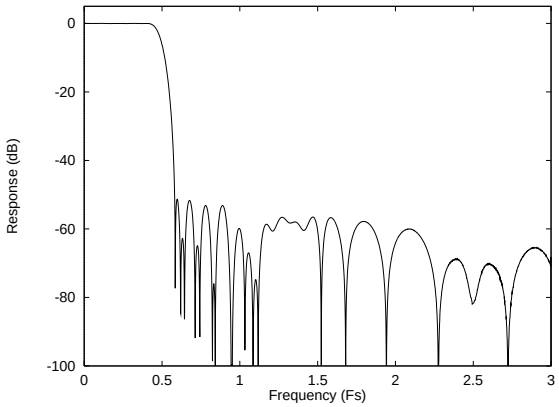


Figure 20 DAC Digital Filter Frequency Response –Type 0

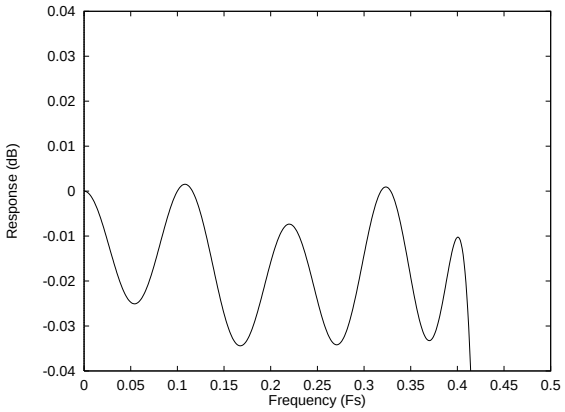


Figure 21 DAC Digital Filter Ripple –Type 0

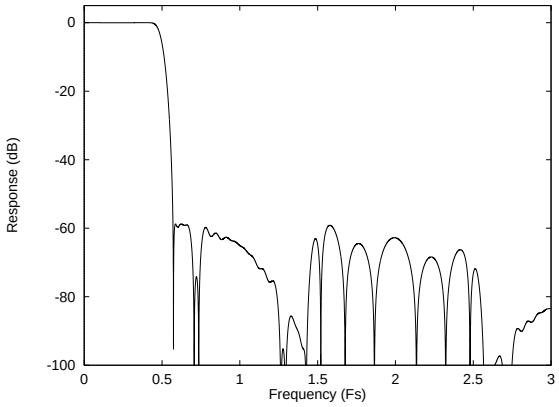


Figure 22 DAC Digital Filter Frequency Response –Type 1

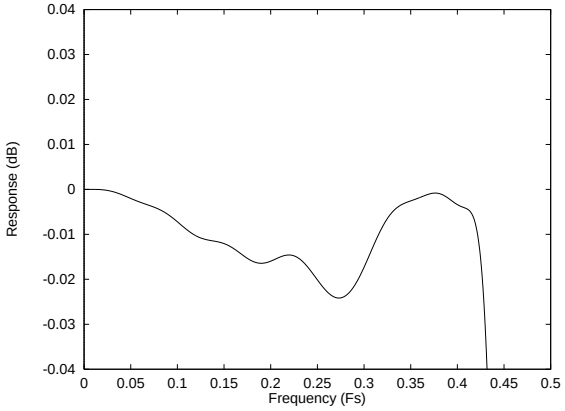


Figure 23 DAC Digital Filter Ripple –Type 1

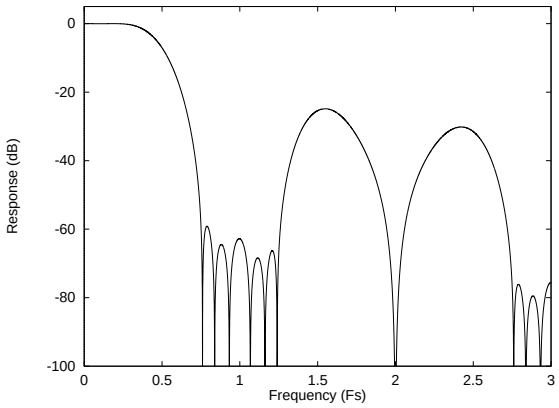


Figure 24 DAC Digital Filter Frequency Response –Type 2

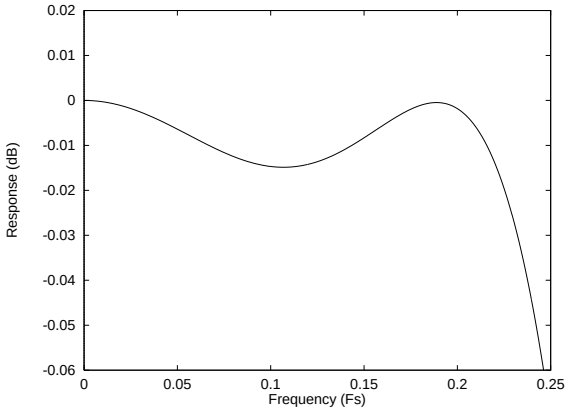


Figure 25 DAC Digital Filter Ripple –Type 2

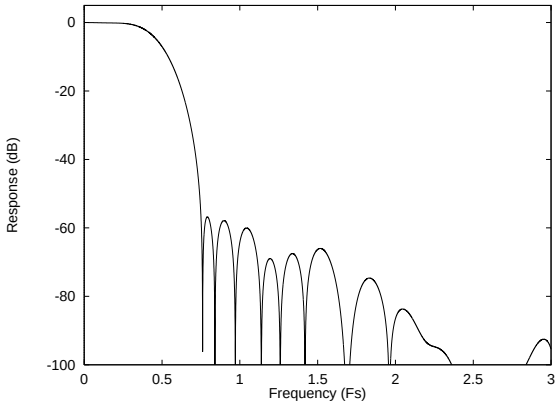


Figure 26 DAC Digital Filter Frequency Response –Type 3

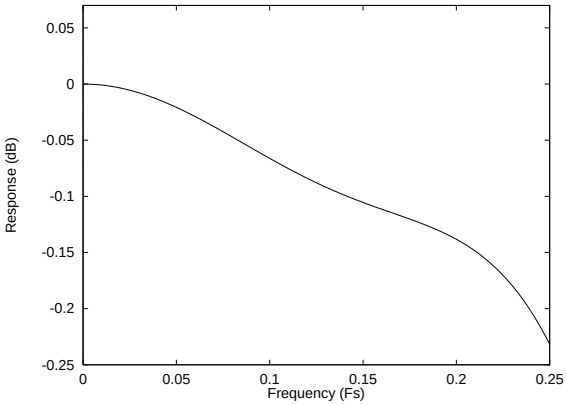


Figure 27 DAC Digital Filter Ripple –Type 3

DIGITAL DE-EMPHASIS CHARACTERISTICS

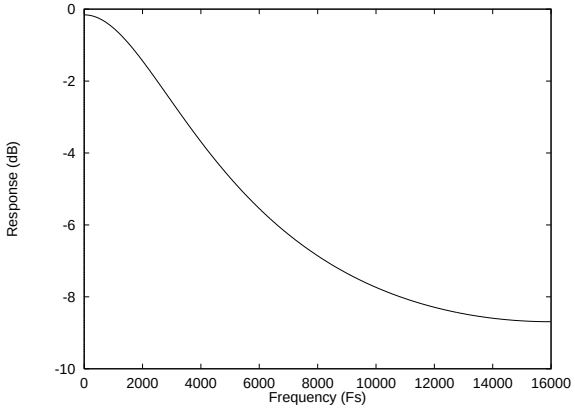


Figure 28 De-Emphasis Frequency Response (32kHz)

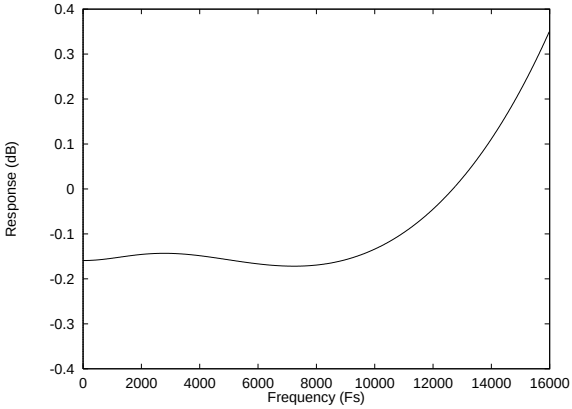


Figure 29 De-Emphasis Error (32kHz)

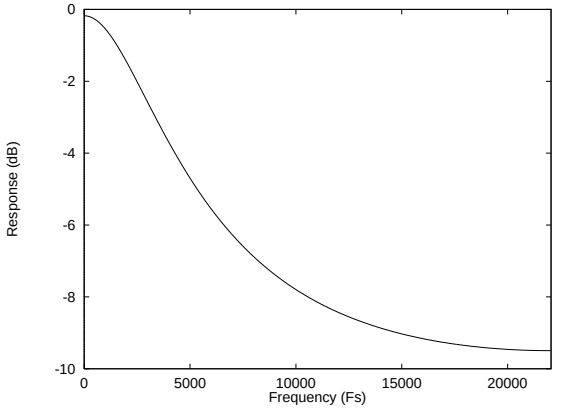


Figure 30 De-Emphasis Frequency Response (44.1kHz)

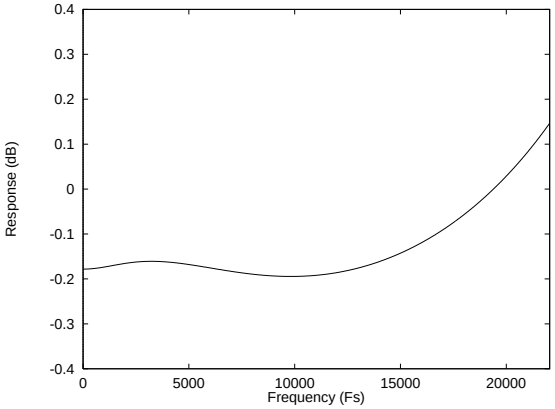


Figure 31 De-Emphasis Error (44.1kHz)

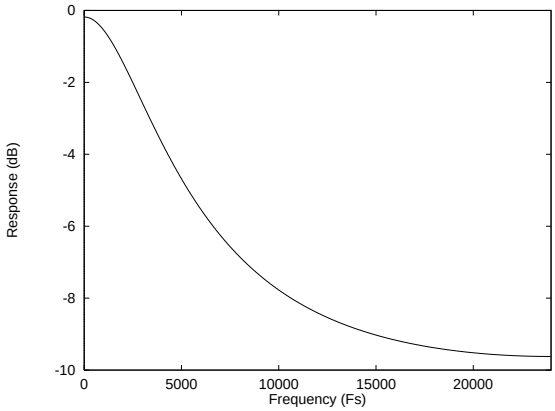


Figure 32 De-Emphasis Frequency Response (48kHz)

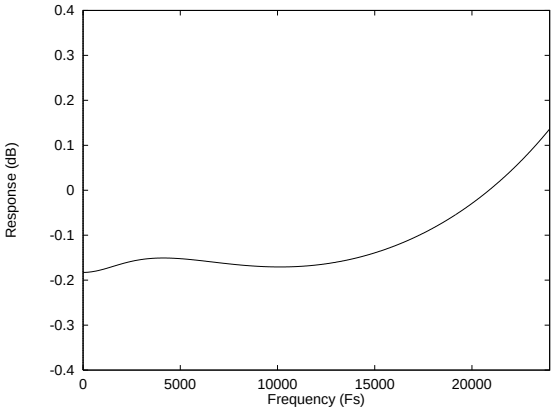
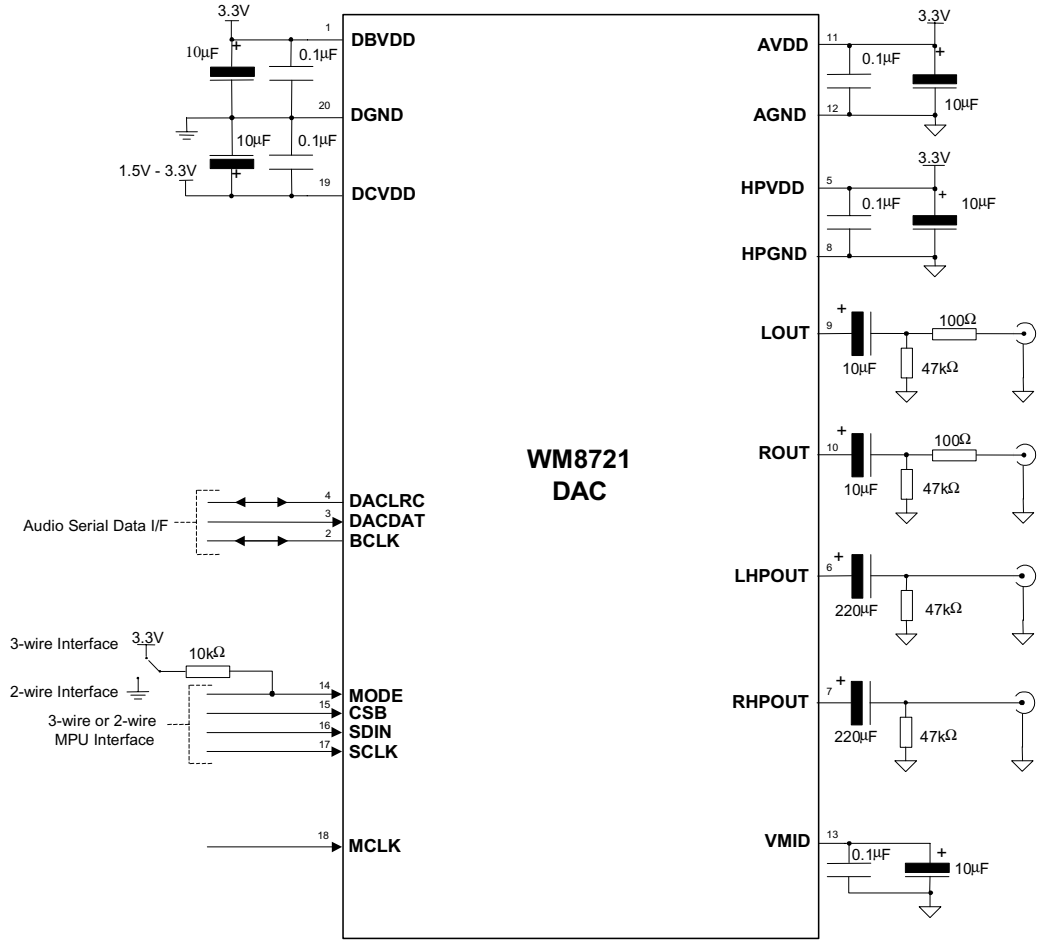


Figure 33 De-Emphasis Error (48kHz)

RECOMMENDED EXTERNAL COMPONENTS

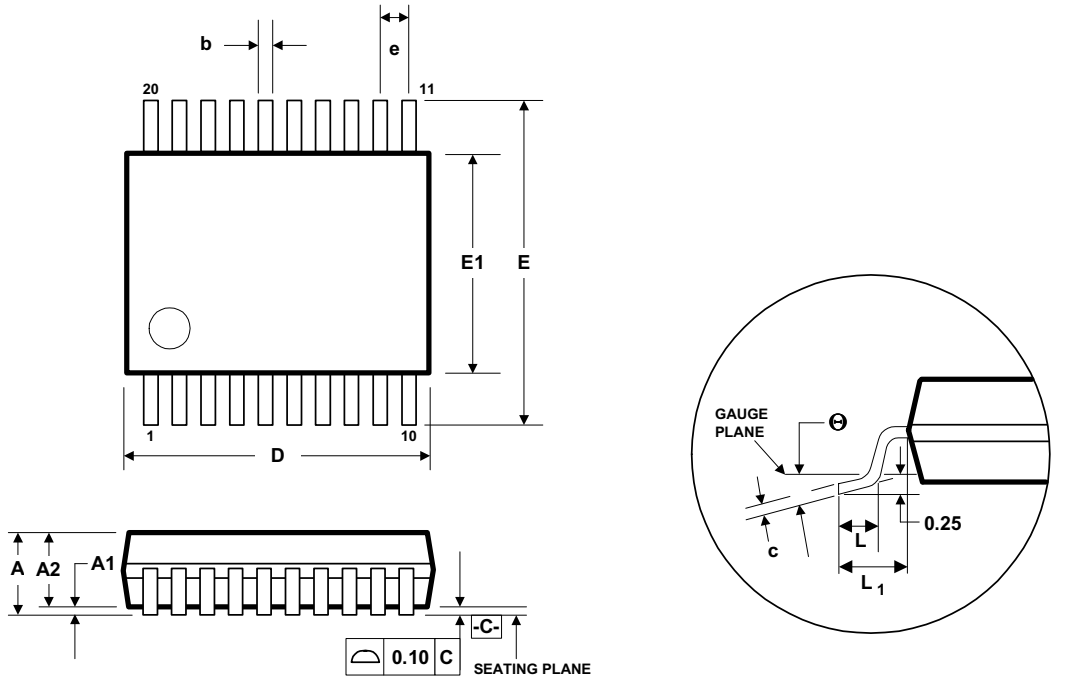


Note
1. Where possible, it is recommended that NPO or COG type capacitors should be used for best performance.
2. The recommended external components are the same for both the QFN and SSOP packages.

Figure 34 External Components Diagram

PACKAGE DIMENSIONS

DS: 20 PIN SSOP (7.2 x 5.3 x 1.75 mm) **DM0015.B**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	-----
A_2	1.65	1.75	1.85
b	0.22	0.30	0.38
c	0.09	-----	0.25
D	6.90	7.20	7.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
L_1		0.125 REF	
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AE. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

IMPORTANT NOTICE

Wolfson Microelectronics plc (WM) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current. All products are sold subject to the WM terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

WM warrants performance of its products to the specifications applicable at the time of sale in accordance with WM's standard warranty. Testing and other quality control techniques are utilised to the extent WM deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

In order to minimise risks associated with customer applications, adequate design and operating safeguards must be used by the customer to minimise inherent or procedural hazards. Wolfson products are not authorised for use as critical components in life support devices or systems without the express written approval of an officer of the company. Life support devices or systems are devices or systems that are intended for surgical implant into the body, or support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided, can be reasonably expected to result in a significant injury to the user. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

WM assumes no liability for applications assistance or customer product design. WM does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of WM covering or relating to any combination, machine, or process in which such products or services might be or are used. WM's publication of information regarding any third party's products or services does not constitute WM's approval, license, warranty or endorsement thereof.

Reproduction of information from the WM web site or datasheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

Resale of WM's products or services with statements different from or beyond the parameters stated by WM for that product or service voids all express and any implied warranties for the associated WM product or service, is an unfair and deceptive business practice, and WM is not responsible nor liable for any such use.

ADDRESS:

Wolfson Microelectronics plc

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com