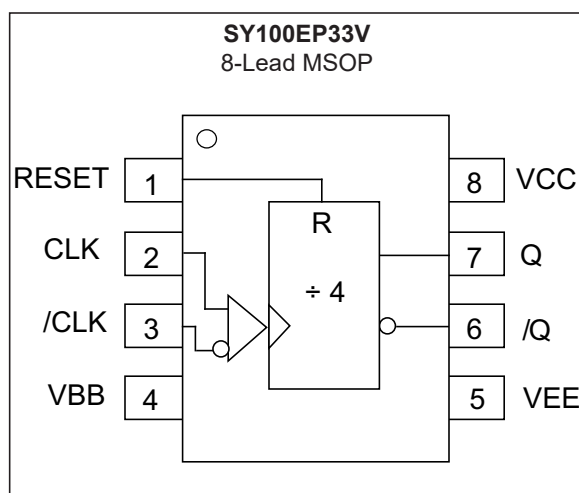


5V/3.3V, 4 GHz, ECL $\div 4$ Divider

Features

- Guaranteed Maximum Frequency >4 GHz
- 3.3V and 5V Power Supply Options
- Guaranteed Propagation Delay CLK to Q <460 ps over Temperature
- Open Input Default State
- Wide Operating Temperature Range: -40°C to $+85^{\circ}\text{C}$
- Available in 8-Pin MSOP Package

Package Type



General Description

The SY100EP33V is an integrated $\div 4$ divider with differential clock inputs.

The VBB pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. VBB may also rebias AC-coupled inputs. When used, decouple VBB and VCC via a $0.01\ \mu\text{F}$ capacitor and limit current sourcing or sinking to 0.5 mA. When not used, VBB should be left open.

The RESET pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the RESET allows for the synchronous use of multiple EP33 in a system.

Under open input conditions, the CLK input and the RESET input will be pulled to GND. The /CLK input will be biased at half of the supply voltage. The 100K series includes internal temperature compensation circuitry.

SY100EP33V

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

PECL Power Supply Voltage (V_{CC}) (Note 1).....	+6V
NECL Power Supply Voltage (V_{EE}) (Note 2).....	–6V
PECL Mode Input Voltage (V_{IN}) (Note 3).....	+6V
NECL Mode Input Voltage (V_{IN}) (Note 4).....	–6V
Continuous Output Current (I_{OUT}).....	50 mA
Surge Output Current (I_{OUT}).....	100 mA
VBB Sink/Source Current (I_{BB}) (Note 5).....	±0.5 mA

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: $V_{CC} = 0V$.

2: $V_{EE} = 0V$.

3: $V_{EE} = 0V$, $V_{IN} \leq V_{CC}$.

4: $V_{CC} = 0V$, $V_{IN} \geq V_{EE}$.

5: Due to the limited drive capability, the VBB reference should only be used for the input of the same package device (i.e., do not use for other devices).

PECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics PECL: $V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. (Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{EE}	—	—	36	mA	$T_A = -40^{\circ}C$
		—	30	36		$T_A = +25^{\circ}C$
		—	—	40		$T_A = +85^{\circ}C$
Output High Voltage (Note 2)	V_{OH}	$V_{CC} - 1.145$	$V_{CC} - 1.020$	$V_{CC} - 0.895$	V	—
Output Low Voltage (Note 2)	V_{OL}	$V_{CC} - 1.945$	$V_{CC} - 1.820$	$V_{CC} - 1.695$	V	—
Input High Voltage (Single Ended)	V_{IH}	$V_{CC} - 1.225$	—	$V_{CC} - 0.880$	V	—
Input Low Voltage (Single Ended)	V_{IL}	$V_{CC} - 1.945$	—	$V_{CC} - 1.625$	V	—
Common Mode Range (Note 3)	V_{IHCMR}	2.0	—	$V_{CC} - 0.4$	V	$T_A = -40^{\circ}C$
		1.9	—	$V_{CC} - 0.4$		$T_A = 0^{\circ}C$ to $+85^{\circ}C$
Output Voltage	V_{BB}	$V_{CC} - 1.525$	$V_{CC} - 1.425$	$V_{CC} - 1.325$	V	—
Input High Current	I_{IH}	—	—	150	μA	—
Input Low Current RESET, CLK	I_{IL}	0.5	—	—	μA	$V_{IN} = V_{IL(MIN)}$
Input Low Current /CLK		–150	—	—		

Note 1: Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

2: Outputs are terminated through a 50Ω resistor to $V_{CC} - 2.0V$.

3: The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1.2V.

NECL DC ELECTRICAL CHARACTERISTICS

Electrical Characteristics NECL: $V_{EE} = -5.5V$ to $-3.0V$; $V_{CC} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated.
(Note 1)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Current	I_{EE}	—	—	36	mA	$T_A = -40^{\circ}C$
		—	30	36		$T_A = +25^{\circ}C$
		—	—	40		$T_A = +85^{\circ}C$
Output High Voltage (Note 2)	V_{OH}	-1.145	-1.020	-0.895	V	—
Output Low Voltage (Note 2)	V_{OL}	-1.945	-1.820	-1.695	V	—
Input High Voltage	V_{IH}	-1.225	—	-0.880	V	—
Input Low Voltage	V_{IL}	-1.945	—	-1.625	V	—
Common Mode Range (Note 3)	V_{IHCMR}	$V_{EE} + 2.0$	—	-0.4	V	$T_A = -40^{\circ}C$
		$V_{EE} + 1.9$	—	-0.4		$T_A = 0^{\circ}C$ to $+85^{\circ}C$
Output Voltage	V_{BB}	-1.525	-1.425	-1.325	V	—
Input High Current	I_{IH}	—	—	150	μA	—
Input Low Current CLK	I_{IL}	0.5	—	—	μA	$V_{IN} = V_{IL(MIN)}$
Input Low Current /CLK		-150	—	—		

- Note 1:** Devices are designed to meet the DC specifications shown in the above table after thermal equilibration has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
- 2:** Outputs are terminated through a 50 Ω resistor to $V_{CC} - 2.0V$.
- 3:** The CMR range is referenced to the most positive side of the differential input voltage. Normal operation is obtained if the high level falls within the specified range and the peak-to-peak voltage lies between 150 mV and 1.2V.

SY100EP33V

AC ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{CC} = 3.0V$ to $5.5V$; $V_{EE} = 0V$ or $V_{EE} = -5.5V$ to $-3.0V$; $V_{CC} = 0V$; $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise stated. All loading with a 50Ω resistor to $V_{CC} - 2.0V$. (Note 1, Note 2)

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Maximum Toggle Frequency (Note 3)	f_{MAX}	4	—	—	GHz	—
Propagation Delay to Differential Output CLK $\rightarrow$ Q, /Q	t_{PLH}, t_{PHL}	300	380	440	ps	$T_A = -40^{\circ}C, +25^{\circ}C$
		320	400	460		$T_A = +85^{\circ}C$
Propagation Delay to Differential Output RESET $\rightarrow$ Q, /Q	t_{PLH}, t_{PHL}	310	420	470	ps	$T_A = -40^{\circ}C, +25^{\circ}C$
		320	450	500		$T_A = +85^{\circ}C$
Reset Recovery Time	t_{RR}	200	100	—	ps	$T_A = +25^{\circ}C$
		200	—	—		$T_A = -40^{\circ}C, +85^{\circ}C$
Minimum Pulse Width Reset	t_{PW}	550	200	—	ps	$T_A = +25^{\circ}C$
		550	—	—		$T_A = -40^{\circ}C, +85^{\circ}C$
Cycle-to-Cycle RMS Jitter	t_{JITTER}	—	0.2	<1	ps _{RMS}	—
Input Voltage Swing (Differential Configuration, Note 4)	V_{PP}	150	800	1200	mV	—
Output Rise/Fall Time Q (20% to 80%)	t_r/t_f	90	170	200	ps	$T_A = -40^{\circ}C$
		100	180	220		$T_A = +25^{\circ}C$
		120	200	240		$T_A = +85^{\circ}C$

- Note 1:** Measured with 750 mV input signal, 50% duty cycle clock source.
- 2:** Specifications for packaged product only.
- 3:** f_{MAX} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
- 4:** Input swing for which AC parameters are ensured.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+85	°C	—
Storage Temperature Range	T_S	-65	—	+150	°C	—
Lead Temperature	T_{LEAD}	—	—	+260	°C	Soldering, 20 sec.
Package Thermal Resistance (MSOP)						
Junction-to-Ambient	θ_{JA}	—	206	—	°C/W	Still-Air
		—	155	—		500 lfpm
Junction-to-Case	θ_{JC}	—	39	—	°C/W	—

SY100EP33V

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 2-1](#).

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	RESET	ECL Asynchronous Reset (with 75 k Ω resistor pull-down resistor to GND).
2, 3	CLK, /CLK	ECL, Clock Inputs (CLK input with 75 k Ω resistor pull-down resistor to GND, /CLK input with 75 k Ω resistor divider).
4	VBB	Reference Voltage Output.
5	VEE	Negative Supply Voltage.
6, 7	/Q, Q	ECL Outputs.
8	VCC	Positive Supply Voltage.

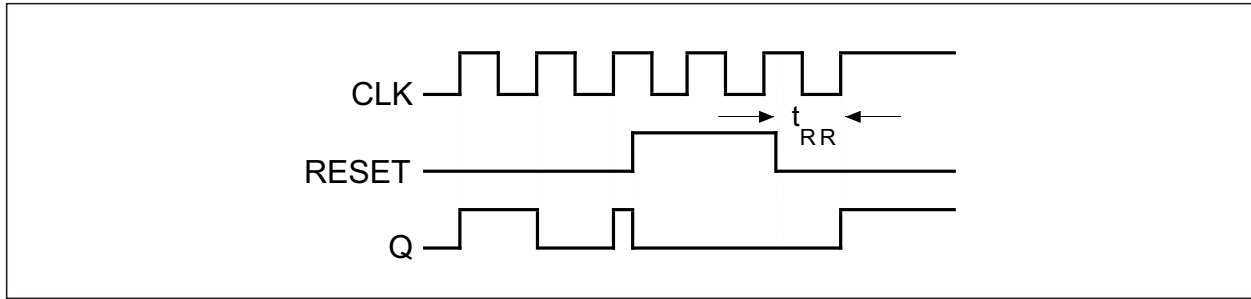
2.1 Truth Table

TABLE 2-2: TRUTH TABLE (Note 1)

CLK	/CLK	RESET	Q	/Q
X	X	H	L	H
Z	/Z	L	F	F

Note 1: Z = Low-to-High Transition
/Z = High-to-Low Transition
F = Divide by 4 Function

3.0 TIMING DIAGRAM



3.1 Input Waveform

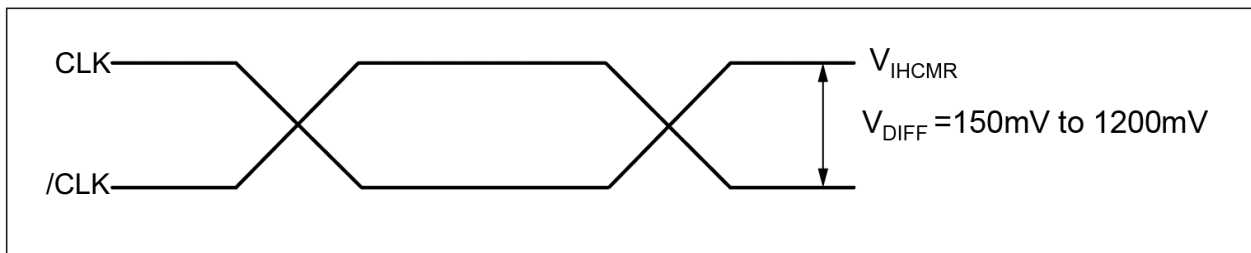


FIGURE 3-1: Input Waveform.

4.0 TERMINATION RECOMMENDATIONS

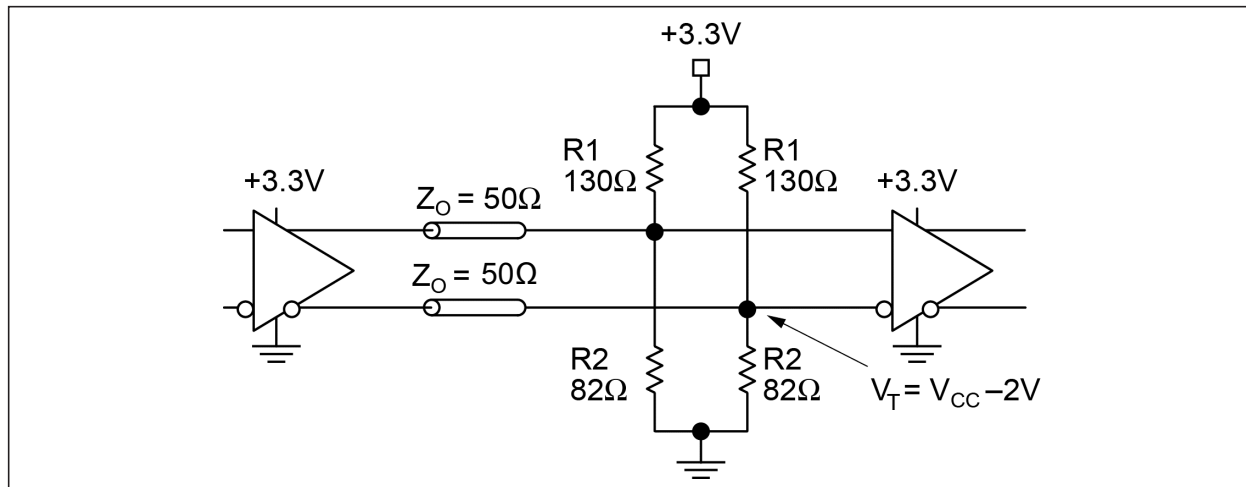


FIGURE 4-1: Parallel Termination - Thevenin Equivalent.

Note: For +5.0V systems: R1 = 82Ω, R2 = 130Ω

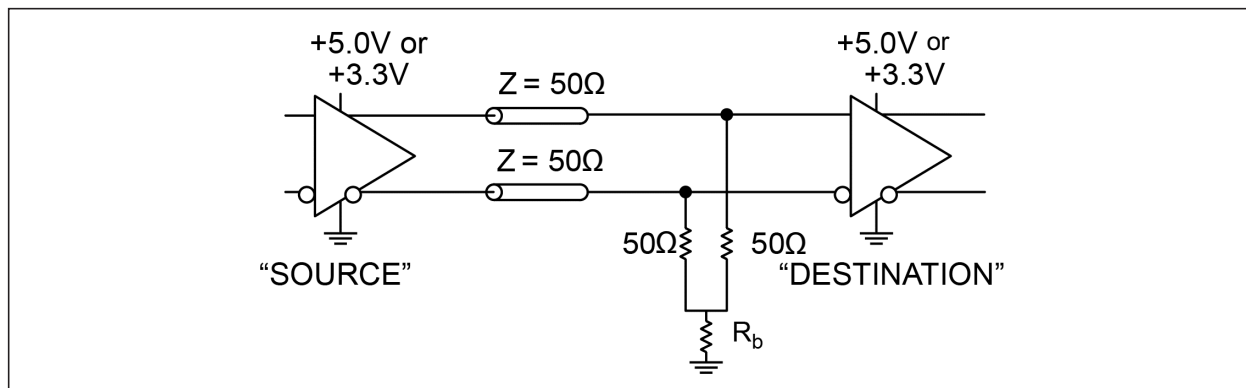


FIGURE 4-2: Three-Resistor Y-Termination.

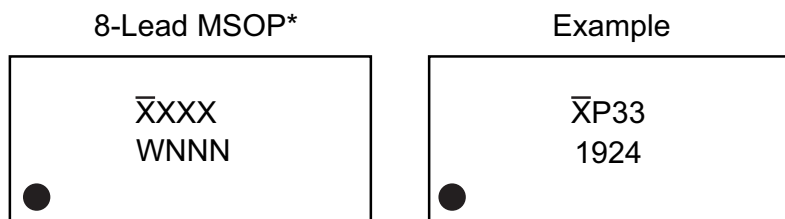
Note: Power-saving alternative to Thevenin termination.

Note: Place termination resistors as close to destination inputs as possible.

Note: R_b resistor sets the DC bias voltage equal to V_T . For +3.3V systems $R_b = 46\Omega$ to 50Ω . For +5V systems, $R_b = 110\Omega$.

5.0 PACKAGING INFORMATION

5.1 Package Marking Information



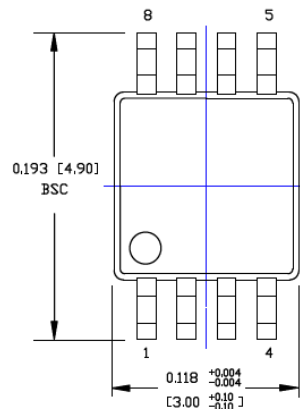
Legend:	XX...X Product code or customer-specific information Y Year code (last digit of calendar year) YY Year code (last 2 digits of calendar year) WW Week code (week of January 1 is week '01') NNN Alphanumeric traceability code (e3) Pb-free JEDEC® designator for Matte Tin (Sn) * This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. •, ▲, ▼ Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. Underbar ($\bar{}$) and/or Overbar ($\bar{}$) symbol may not be to scale.

SY100EP33V

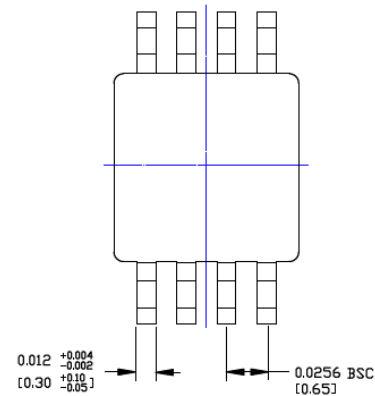
TITLE

8 LEAD MSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

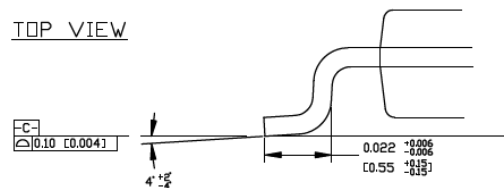
DRAWING #	MSOP-8LD-PL-1	UNIT	INCH	[MM]
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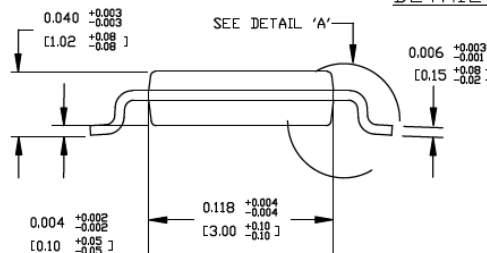
TOP VIEW



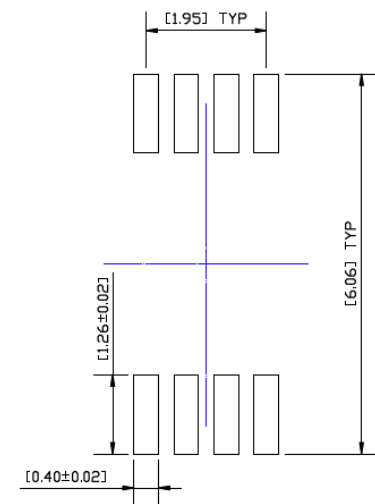
BOTTOM VIEW



DETAIL A



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTES:

1. DIMENSIONS ARE IN INCHES [MM].
2. CONTROLLING DIMENSION: MM
3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.20] PER SIDE.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision A (February 2019)

- Converted Micrel document SY100EP33V to Microchip data sheet DS20006166A.
- Minor text changes throughout.
- Removed all reference to the EOL SY10EP33V version.
- Revised [Section 1.0, Electrical Characteristics](#) section with updated Electrical tables.

Revision B (August 2019)

- Updated minimum values for Common Mode Range voltage in [PECL DC Electrical Characteristics](#) table and [NECL DC Electrical Characteristics](#) table.
- Minor stylistic updates to align data sheet with current style.

SY100EP33V

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

<u>PART NO.</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-XX</u>
Device	Supply Voltage	Package	Temperature Range	Special Processing
Device:	SY100EP33: ECL +4 Divider			
Supply Voltage Range:	V	=	3.3V/5V	
Package:	K	=	8-Lead MSOP (NiPdAu, Pb-Free)	
Temperature Range:	G	=	-40°C to +85°C	
Special Processing:	<blank>	=	100/Tube	
	TR	=	1,000/Reel	

Examples:

a) SY100EP33VKG: ECL +4 Divider, 3.3V/5V Supply Voltage, 8-Lead MSOP (NiPdAu, Pb-Free), -40°C to +85°C Temp. Range, 100/Tube

b) SY100EP33VKG-TR: ECL +4 Divider, 3.3V/5V Supply Voltage, 8-Lead MSOP (NiPdAu, Pb-Free), -40°C to +85°C Temp. Range, 1,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

SY100EP33V

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