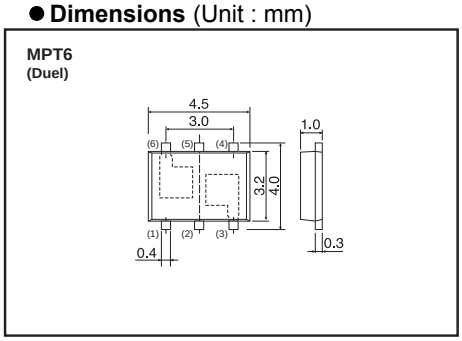
4V Drive Nch + Nch MOSFET

MP6K14

● Structure
Silicon N-channel MOSFET

● Features
1) Low on-resistance.
2) High power package(MPT6).
3) Low voltage drive(4V drive).

● Dimensions (Unit : mm)

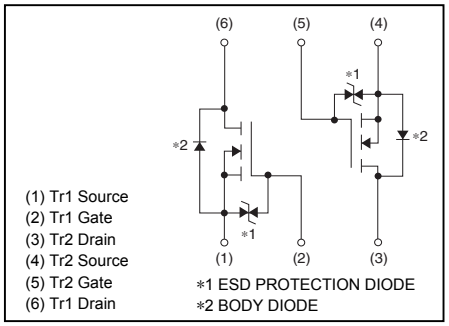


● Application
Switching

● Packaging specifications

Type	Package	Taping
	Code	TCR
	Basic ordering unit (pieces)	1000
MP6K14		O

● Inner circuit



● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	±8.0	A
	Pulsed	I_{DP} *1	±18	A
Source current (Body Diode)	Continuous	I_s	1.6	A
	Pulsed	I_{sp} *1	18	A
Power dissipation		P_D *2	2.0	W / TOTAL
			1.4	W / ELEMENT
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	−55 to +150	°C

*1 Pw≤10μs, Duty cycle≤1%

*2 Mounted on a ceramic board.

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● **Electrical characteristics** (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gatesource leakage	I_{GSS}	–	–	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drainsource breakdown voltage	$V_{(BR)DSS}$	30	–	–	V	I_D=1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	–	–	1	μA	V_{DS}=30V, V_{GS}=0V
Gate threshold voltage	$V_{GS(th)}$	1.0	–	2.5	V	V_{DS}=10V, I_D=1mA
Static drainsource onstate resistance	$R_{DS(on)}$*	–	18	25	mΩ	I_D=8.0A, V_{GS}=10V
		–	21	29		I_D=8.0A, V_{GS}=4.5V
		–	23	32		I_D=8.0A, V_{GS}=4.0V
Forward transfer admittance	$\|Y_{fs}\|$*	4.5	–	–	S	I_D=8.0A, V_{DS}=10V
Input capacitance	C_{iss}	–	470	–	pF	V_{DS}=10V
Output capacitance	C_{oss}	–	170	–	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	–	80	–	pF	f=1MHz
Turnon delay time	$t_{d(on)}$*	–	8	–	ns	I_D=4.0A, V_{DD}≒ 15V
Rise time	t_r *	–	30	–	ns	V_{GS}=10V
Turnoff delay time	$t_{d(off)}$*	–	39	–	ns	R_L=3.75Ω
Fall time	t_f *	–	9	–	ns	R_G=10Ω
Total gate charge	Q_g *	–	7.3	–	nC	I_D=8.0A, V_{DD}≒15V
Gatesource charge	Q_{gs} *	–	1.5	–	nC	V_{GS}=5V
Gatedrain charge	Q_{gd} *	–	2.9	–	nC	

*Pulsed

●**Body diode characteristics** (Source-Drain) (Ta = 25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD} *	–	–	1.2	V	Is=8.0A, V_{GS}=0V

*Pulsed

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●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical Output Characteristics (Ⅰ)

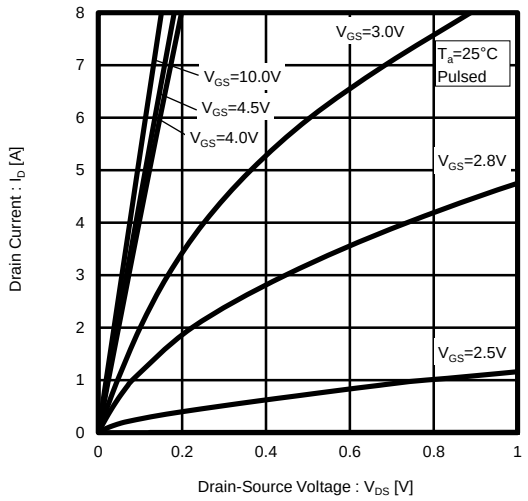


Fig.2 Typical Output Characteristics (Ⅱ)

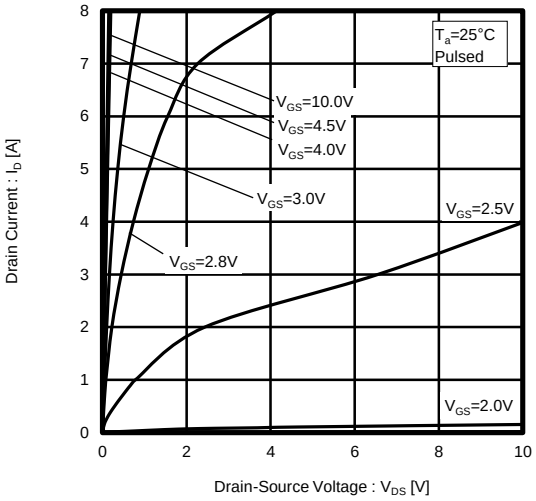


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

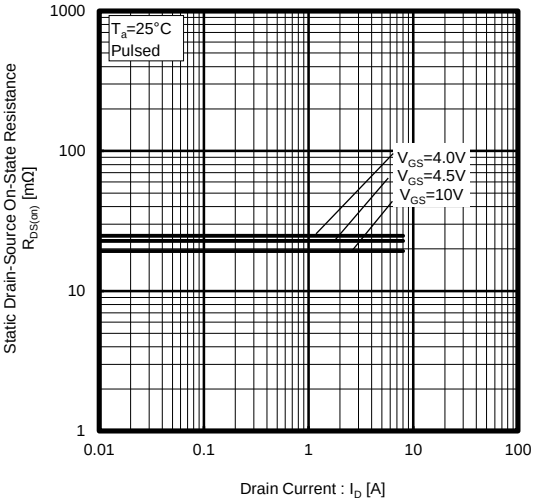


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

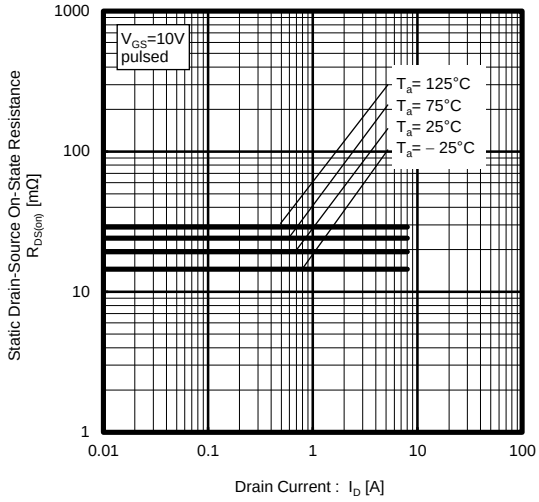


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

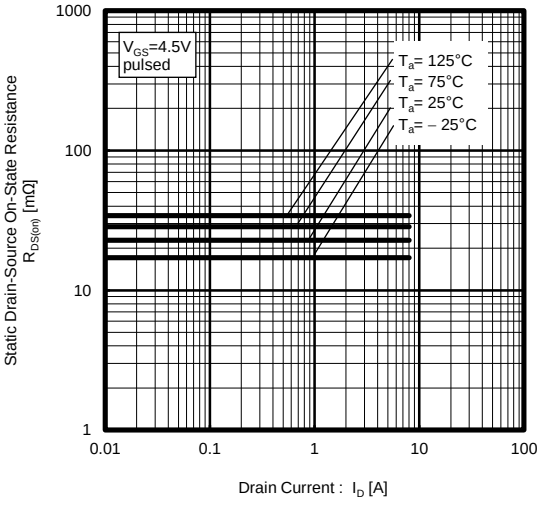
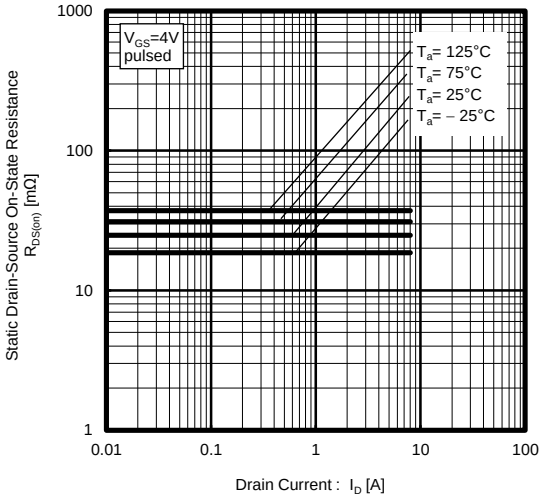


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current



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Fig.7 Forward Transfer Admittance vs. Drain Current

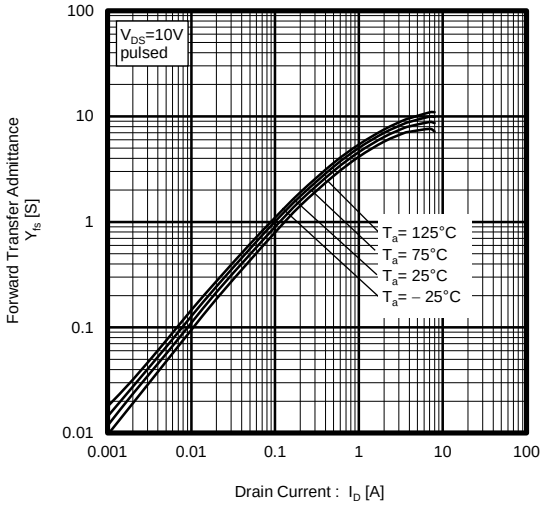


Fig.8 Typical Transfer Characteristics

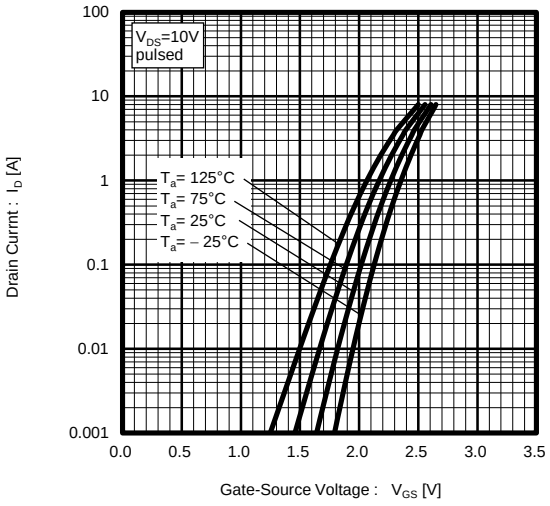


Fig.9 Source Current vs. Source-Drain Voltage

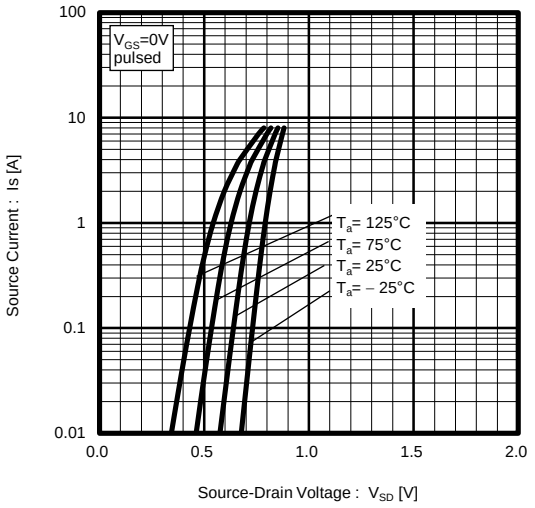


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

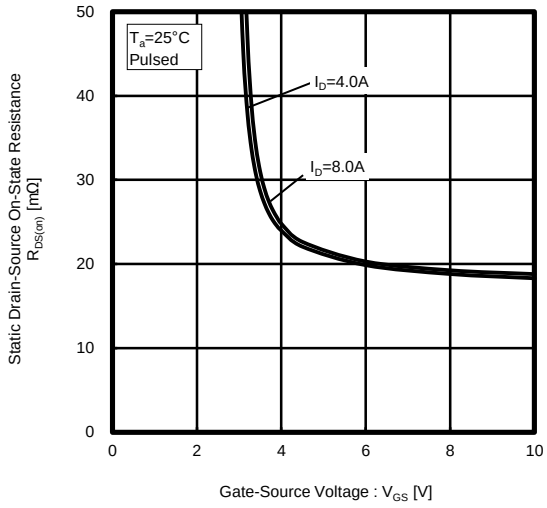


Fig.11 Switching Characteristics

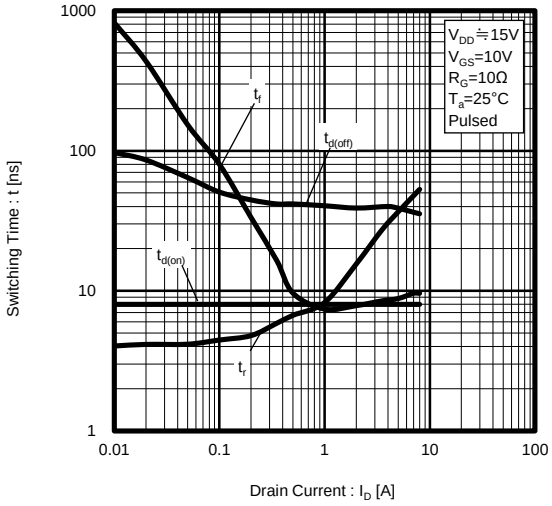
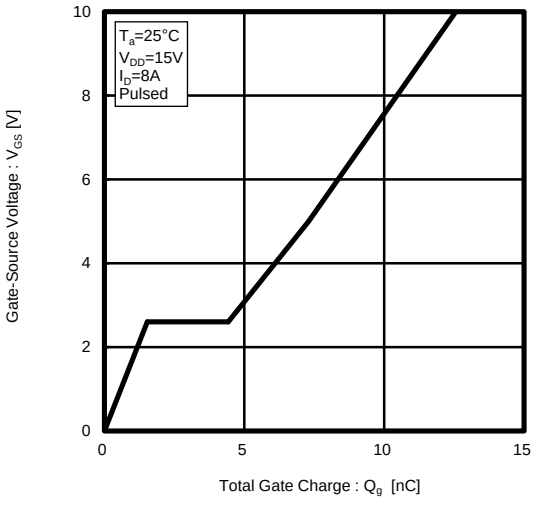


Fig.12 Dynamic Input Characteristics



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Fig.13 Typical Capacitance vs. Drain-Source Voltage

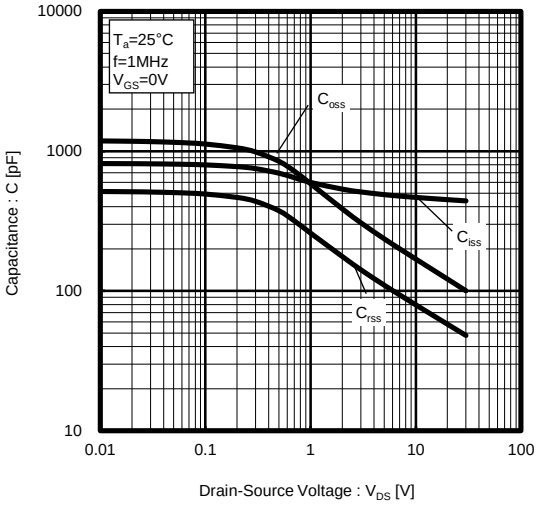


Fig.14 Maximum Safe Operating Area

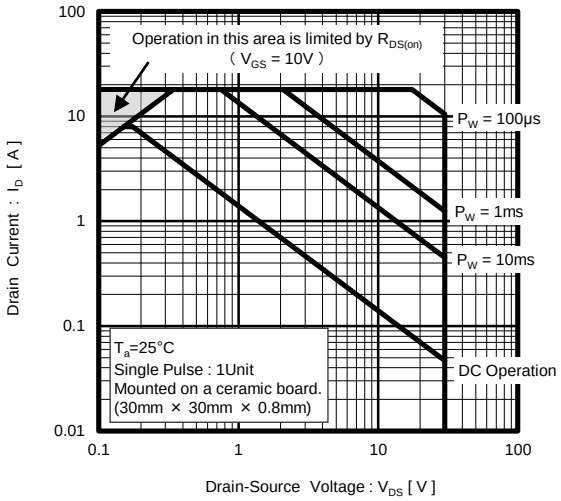
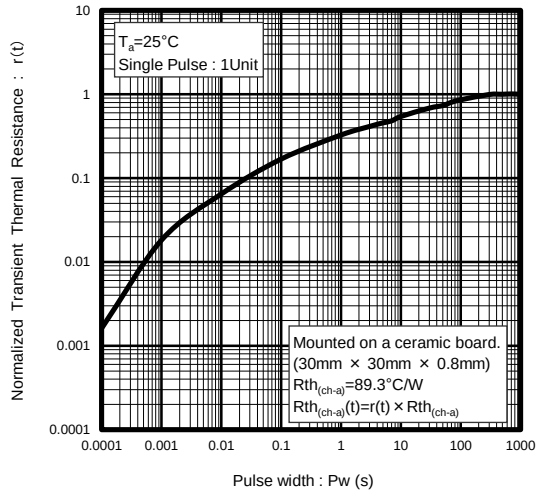


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width



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● **Measurement circuits**

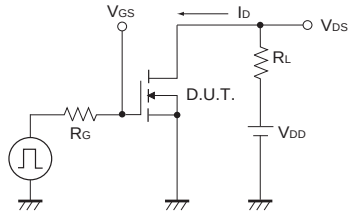


Fig.1-1 Switching Time Measurement Circuit

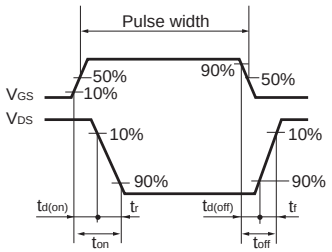


Fig.1-2 Switching Waveforms

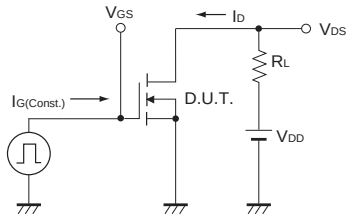


Fig.2-1 Gate Charge Measurement Circuit

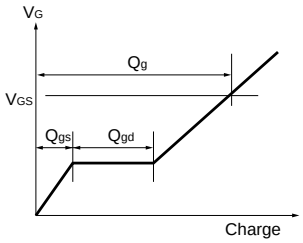


Fig.2-2 Gate Charge Waveform

● **Notice**

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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