GIGABIT ETHERNET TRANSCEIVER S2060

FEATURES

- Operating rate
- 1250 MHz (Gigabit Ethernet) line rates
- Half and full VCO output rates
- Functionally compliant IEEE 802.3z Gigabit Ethernet standard
- Transmitter incorporating Phase-Locked Loop (PLL) clock synthesis from low speed reference
- Receiver PLL provides clock and data recovery
- 10-bit parallel TTL compatible interface
- Low-jitter serial LVPECL compatible interface
- Local loopback
- Single +3.3 V supply, 620 mW power dissipation
- 64 PQFP or TQFP package
- Continuous downstream clocking from receiver
- Drives 30 m of Twinax cable directly

APPLICATIONS

- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

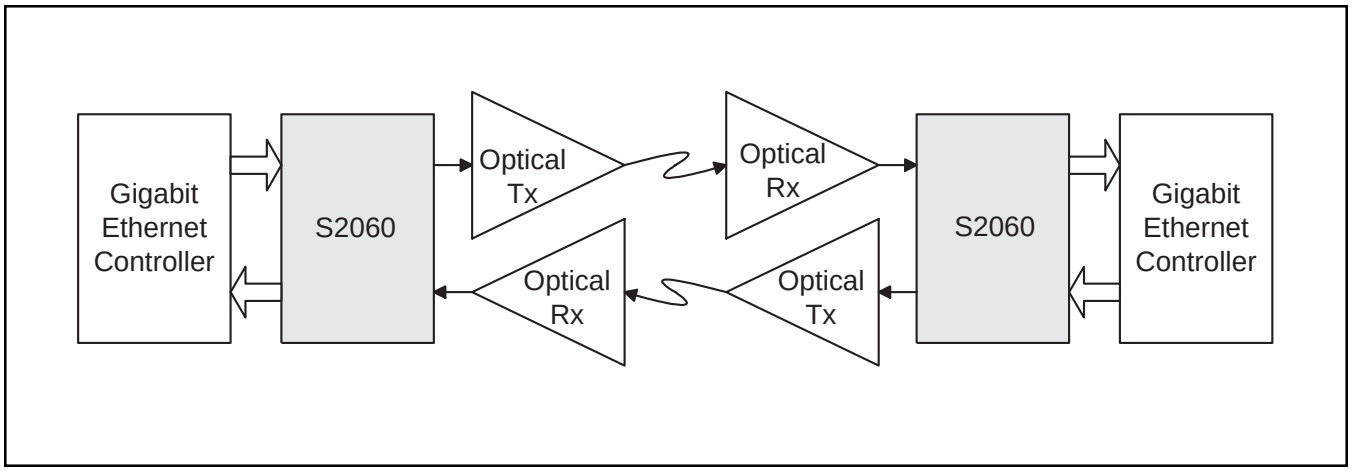
GENERAL DESCRIPTION

The S2060 transmitter and receiver chip facilitates high speed serial transmission of data over fiber optic, coax, or twinax interfaces. The device conforms to the requirements of the IEEE 802.3z Gigabit Ethernet specification, and runs at 1250.0 Mbps data rates with an associated 10-bit data word.

The chip provides parallel-to-serial and serial-to-parallel conversion, clock generation/recovery, and framing for block encoded data. The on-chip transmit PLL synthesizes the high-speed clock from a low-speed reference. The on-chip receive PLL performs clock recovery and data re-timing on the serial bit stream. The transmitter and receiver each support differential LVPECL compatible I/O for copper or fiber optic component interfaces with excellent signal integrity. Local loopback mode allows for system diagnostics. The chip requires a +3.3 V power supply and dissipates typically 620 mW.

The S2060 can be used for a variety of applications including Gigabit Ethernet, serial backplanes, and proprietary point-to-point links. Figure 1 shows a typical configuration incorporating the chip.

Figure 1. System Block Diagram



S2060 OVERVIEW

The S2060 transmitter and receiver provide serialization and deserialization functions for block encoded data to implement a Gigabit Ethernet interface. The S2060 functional block diagram is depicted in Figure 2. The sequence of operations is as follows:

Transmitter

1.10-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver

1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10-bit parallel output

The 10-bit parallel data input to the S2060 should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters[1]. For reference, Table 1 shows the mapping of the parallel data to the 8B/10B codes.

Loop Back

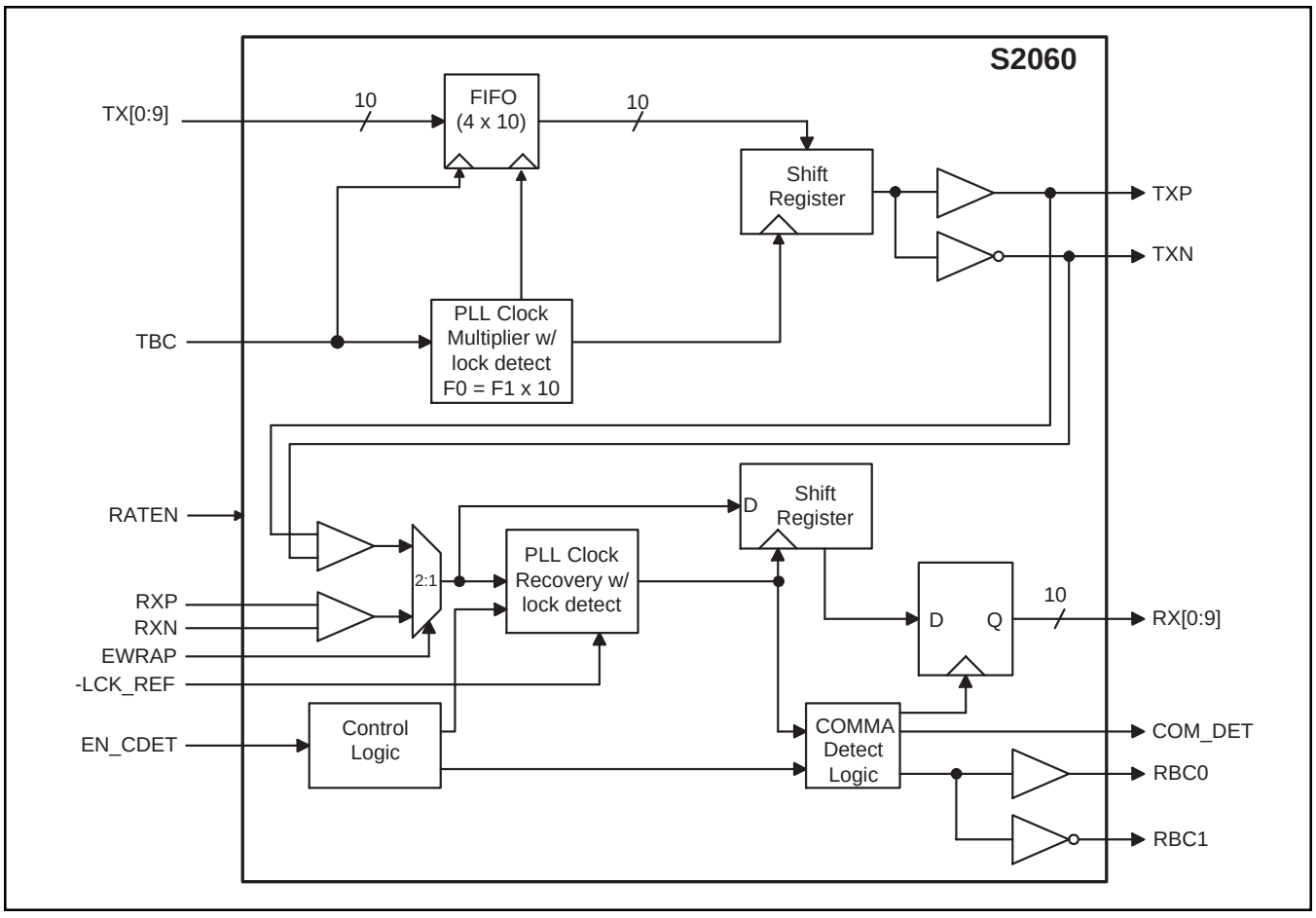
Local loopback provides a capability for performing off-line testing. This is useful for ensuring the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

1. A.X. Widmer and P.A. Franaszek, "A Byte Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC 9391, May 1982.

Table 1. Data Mapping to 8B/10B Alphabetic Representation

	Data Byte									
TX[0:9] or RX[0:9]	0	1	2	3	4	5	6	7	8	9
8B/10B Alphabetic Representation	a	b	c	d	e	i	f	g	h	j

Figure 2. Functional Block Diagram



TRANSMITTER DESCRIPTION

The S2060 transmitter accepts 10-bit parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The chip is fully compatible with the IEEE 802.3z Gigabit Ethernet standard, and supports the Gigabit Ethernet data rate of 1250.0 Mbps. The S2060 uses a PLL to generate the serial rate transmit clock. The transmitter runs at 10 times the TBC input clock, and operates in either full rate or half rate mode. At the full VCO rate the transmitter runs at 1.25 GHz, while in half rate mode it operates at 625 MHz.

Parallel-to-Serial Conversion

The parallel-to-serial converter takes in 10-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter on the positive going edge of TBC. The data is then clocked into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10x the TBC input frequency. TX[0] is transmitted first.

Transmit Byte Clock (TBC)

The Transmit Byte Clock input (TBC) must be supplied from a clock source with 100 ppm tolerance to assure that the transmitted data meets the Gigabit Ethernet frequency limits. The internal serial clock is frequency locked to TBC (125.00 MHz).

TBC may be 62.5 MHz or 125 MHz, determined by the state of the RATEN input. Operating rates are shown in Table 2.

Transmit Latency

The average transmit latency is 4 byte times.

Table 2. Operating Rates

RATEN	Parallel Input Rate (Mbps)	TBC Frequency (MHz)	Serial Output Rate (Gbps)
0	125	125	1.25
1	62.5	62.5	0.625

RECEIVER DESCRIPTION

Whenever a signal is present, the receiver attempts to recover the serial clock from the received data stream. The S2060 searches the serial bit stream for the occurrence of a positive polarity COMMA sync pattern (0011111xxx positive running disparity) to perform word synchronization. Once synchronization on both bit and word boundaries is achieved, the receiver provides the decoded data on its parallel outputs.

Clock Recovery Function

Clock recovery is performed on the input data stream. A simple state machine in the clock recovery macro decides whether to acquire lock from the serial data input or from the reference clock. The decision is based upon the frequency and run length of the input serial data.

The lock to reference frequency criteria ensure that the S2060 will respond to variations in the serial data input frequency (as compared to the reference frequency). The new lock state is dependent upon the current lock state, as shown in Table 3. The run-length criteria ensure that the S2060 will respond appropriately and quickly to a loss of signal. The run-length checker flags a condition of consecutive ones or zeros across 12 parallel words. Thus, 119 or less consecutive ones or zeros does not cause signal loss, 129 or more causes signal loss, and 120 – 128 may or may not, depending on how the data aligns across byte boundaries. If both the off-frequency detect test and the run-length test is satisfied, the CRU will attempt to lock to the incoming data.

Table 3. Lock to Reference Frequency Criteria

Current Lock State	PLL Frequency (vs. TBC)	New Lock State
Locked	< 488 ppm	Locked
	488 to 732 ppm	Undetermined
	> 732 ppm	Unlocked
Unlocked	< 244 ppm	Locked
	244 to 366 ppm	Undetermined
	> 366 ppm	Unlocked

In any transfer of PLL control between the serial data and the reference clock, the RBC0 and RBC1 remain phase continuous and glitch free, assuring the integrity of downstream clocking.

Reference Clock Input

The reference clock must be provided from a low jitter clock source. The frequency of the received data stream must be within 400 ppm of the reference clock to ensure reliable locking of the receiver PLL. A single reference clock is provided to both the transmit and receive PLL's.

Data Output

The S2060 provides either framed or unframed parallel output data, determined by the state of EN_CDET. With EN_CDET held ACTIVE, the S2060 will detect and align to the 8B/10B COMMA codeword anywhere in the data stream. When EN_CDET is INACTIVE, no attempt is made to synchronize on any particular incoming character. The S2060 will achieve bit synchronization within 250 bit times and begin to deliver unframed parallel output data words whenever it has received full transmission words. Upon change of state of the EN_CDET input, the COM_DET output response will be delayed by a maximum of 3 byte times.

The COM_DET output signal is ACTIVE whenever EN_CDET is active and the COMMA control character is present on the RX[0:9] parallel data outputs. The COM_DET output signal will be INACTIVE at all other times.

Parallel Output Clock Rate and Data Stretching

The S2060 supports both full rate and half rate outputs, selected via the RATEN input. Table 4 shows the operating rate scenarios. When RATEN is INACTIVE, a data clock is provided on RBC1 at the data rate. Data should be clocked on the rising edge of RBC1. When RATEN is ACTIVE the device is in full rate mode, and complementary TTL clocks are provided on the RBC0 and RBC1 outputs at 1/2 the data rate as required by the Gigabit Ethernet Standard. Data is clocked on the rising edges of both RBC0 and RBC1. See Figures 11 and 12.

Table 4. Operating Rates

RATEN	Serial Input Rate (Gbps)	RBC0 (MHz)	RCB1 (MHz)	Parallel Output Rate (Mbps)
0	1.25	62.5	62.5	125
1	.625	N/A	62.5	62.5

Fibre Channel and Gigabit Ethernet Standards require that the COMMA sync character appears on the rising edge of the RBC1 signal. In full rate mode the phase of the data is adjusted such that this requirement is met. No alignment is necessary when the S2060 is operating in half rate mode since the output clock frequency is equal to the parallel word rate (RATEN INACTIVE).

In ethernet applications it is illegal for multiple consecutive COMMA characters to be generated. However, multiple consecutive COMMA characters can occur in serial backplane applications. The S2060 is able to operate properly when multiple consecutive COMMA characters are received: after the first COMMA is detected and aligned, the RBC0/RBC1 clock operates without glitches or loss of cycles. Additionally, COM_DET stays high while multiple COMMAS are being output.

Receive Latency

The average receive latency is 8 byte times.

Table 5. Pin Description and Assignment

Pin Name	Level	I/O	Pin #	Description
TX[9] TX[8] TX[7] TX[6] TX[5] TX[4] TX[3] TX[2] TX[1] TX[0]	LVTTL	I	13 12 11 9 8 7 6 4 3 2	Transmit Data. Parallel data on this bus is clocked in on the rising edge of TBC. TX[0] is transmitted first.
TBC	LVTTL	I	22	Transmit Byte Clock. Reference clock input to the PLL clock multiplier. The frequency of TBC is the bit rate divided by 10. When TESTEN is active, TBC replaces the VCO clock to facilitate factory test. TBC should be supplied by a crystal controlled reference since jitter on this line directly translates to jitter on the output data.
RATEN	LVTTL	I	14	Rate Select. Active Low. This signal configures the PLL's for the appropriate TBC frequency. When inactive, the device is in 1/2 rate mode. When active, the device is in full rate mode. See Tables 2 and 4.
EN_CDET	LVTTL	I	24	Enable Comma Detect. Active High. When active, enables detection of the COMMA sync pattern to set the word frame boundary for the data to follow. When inactive, data is treated as unframed.
EWRAP	LVTTL	I	19	Enable Wrap. When active, the transmitter serial data outputs are internally routed to the receiver serial data inputs. TXP/N are static (logic 1) in this state. When inactive, the RXP/N serial inputs are selected (normal operation).
RXP RXN	Diff. LVPECL	I	54 52	(Externally Capacitively Coupled.) LVPECL Receive Serial Data Inputs. RXP is the positive differential input, RXN is negative. Internally biased to VCC -1.3 V.
-LCK_REF	LVTTL	I	27	Active Low. Lock to Reference Input. When inactive or open, the receive PLL will lock to the incoming data (normal operation). When active, the receive PLL is forced to lock to the TBC input.

Table 5. Pin Description and Assignment (Continued)

Pin Name	Level	I/O	Pin #	Description
RX[9] RX[8] RX[7] RX[6] RX[5] RX[4] RX[3] RX[2] RX[1] RX[0]	LVTTL	O	34 35 36 38 39 40 41 43 44 45	Receive Data Outputs. For full rate output, parallel data on this bus is valid on the rising edges of RBC0 and RBC1. RX[0] is the first bit received.
RBC1 RBC0	LVTTL	O	30 31	Complementary Receive Byte Clocks. In full rate mode, parallel receive data is valid on the rising edges of RBC0 and RBC1 (see Figure 8, timing diagram). For half rate, output data is valid on the rising edge of RBC1. See Table 4.
COM_DET	LVTTL	O	47	Comma Detect. Active High. When EN_CDET is active, COM_DET indicates that the sync character is present on the parallel bus bits RX[0:9]. Upon detection of the COMMA sync character (0011111xxx positive polarity) this output data is valid on the rising edge of RBC1 and remains active for one RBC1 clock period. When EN_CDET is inactive, COM_DET is held inactive (logic 0). Upon change of state of the EN_CDET input, the COM_DET output response will be delayed by a maximum of 3 byte times.
TXP TXN	Diff. LVPECL	O	62 61	Transmit Serial Data. These lines are static (TXN HIGH, TXP HIGH) when EWRAP is active. These lines are static (TXN HIGH, TXP LOW) when TXRST is active. Upon startup, these outputs are held static (TXN HIGH, TXP LOW) until the TXPLL has locked to the reference clock. Each output can drive 150 Ω to ground.

S2060A, S2060B, S2060D Specific Pins

DNC			16, 17, 48, 49	Not connected. Note that pin 48 cannot be tied high. It must be open or held low.

S2060C Specific Pins

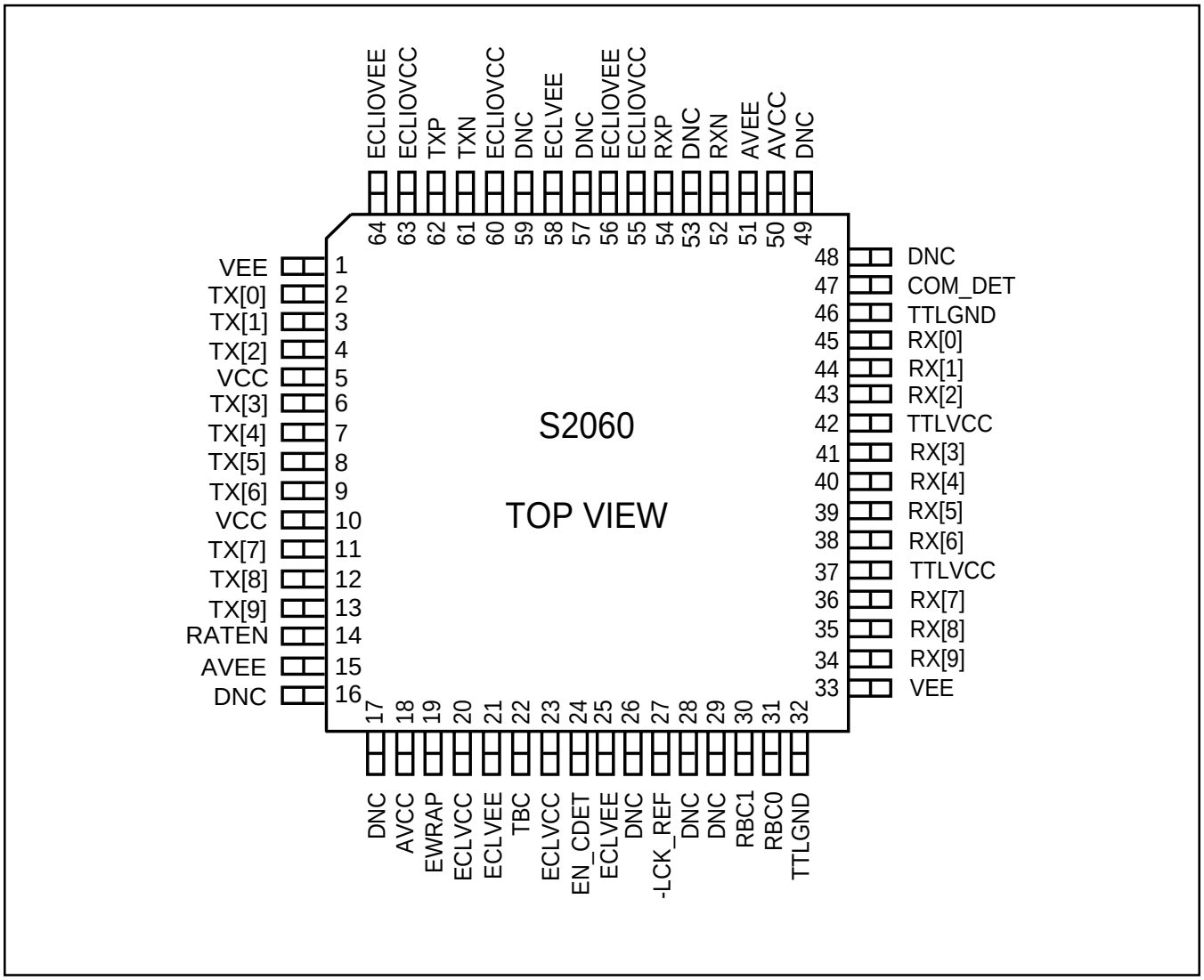
TC1 TC0			16 17	Transmit Capacitor. External capacitor connections for transmitter internal PLL filter. The recommended valueof this external capacitor is 2 nF (a value of 1 nF can also be used). If desired, the external capacitor may be omitted with no loss in performance.
RC0 RC1			48 49	Receiver Capacitor. External capacitor connections for receiver internal PLL filter. The recommended value of this external capacitor is 2 nF (a value of 1 nF can also be used). If desired, the external capacitor may be omitted with no loss in performance. Note that pin 48 cannot be tied high. It must be open (as recommended with external capacitor) or held low.

Note: All TTL inputs have internal 15 KΩ pull-up networks.

Table 6. Power and Ground Signals

Pin Name	Level	Pin #	Description
ECLVCC	+3.3 V	20, 23	Core Power Supply
ECLVEE	GND	21, 25, 58	Core Ground
ECLIOVCC	+3.3 V	55, 60, 63	LVPECL I/O Power Supply
ECLIOVEE	GND	56, 64	LVPECL I/O Ground
TTLVCC	+3.3 V	37, 42	LVTTL Power Supply
TTLGND	GND	32, 46	LVTTL Ground
AVCC	+3.3 V	18, 50	Analog Power Supply
AVEE	GND	15, 51	Analog Ground
VCC	+3.3 V	5, 10	Power
VEE	GND	1, 33	Ground
DNC		48	This pin cannot be tied Low. It should be floated or tied High.
DNC		26, 28, 29, 53, 57, 59	Not connected.

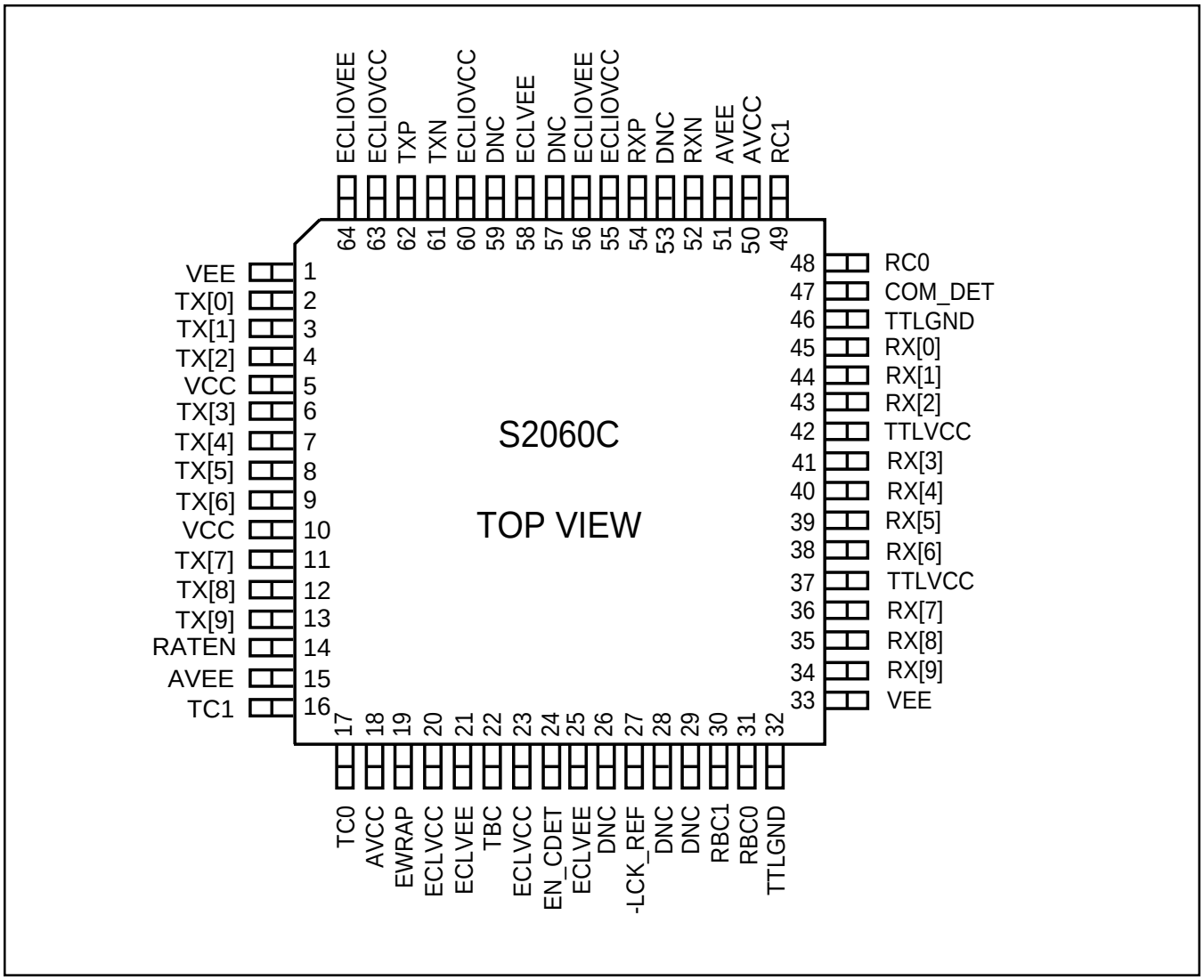
Figure 3. S2060 Pinout (S2060A, S2060B, S2060D)



Thermal Management

Device	Package Max Power	Θja (Still Air)	Θjc
S2060A (10mm 64 PQFP/HS package)	1.333 W	45˚ C/W	15˚ C/W
S2060B (14mm 64 PQFP package)	1.333 W	45˚ C/W	15˚ C/W
S2060D (14mm 64 PQFP package with heat spreader)	1.125 W	40˚ C/W	15˚ C/W

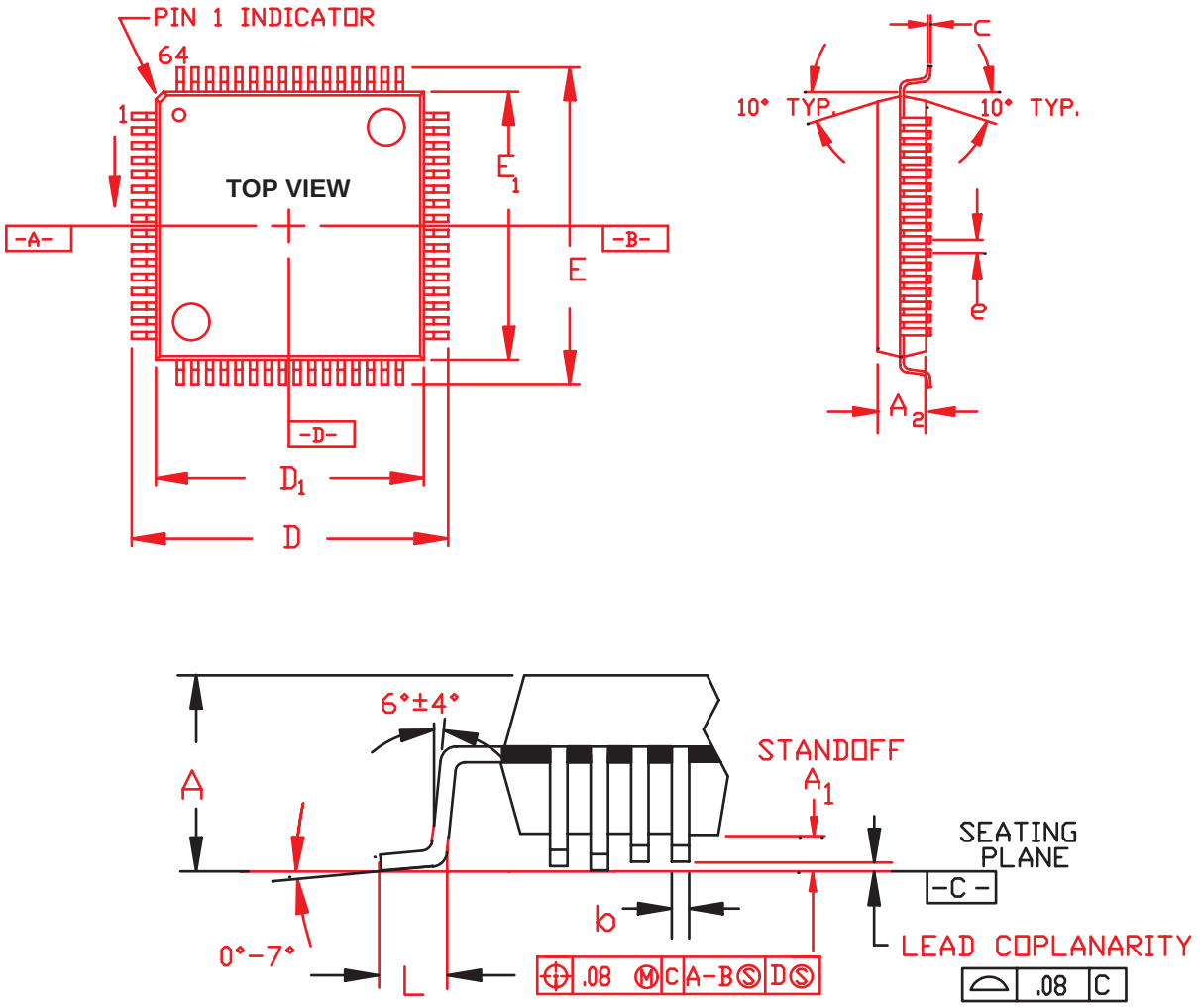
Figure 4. S2060 Pinout (S2060C)



Thermal Management

Device	Package Max Power	Θja (Still Air)	Θjc
S2060C (10mm 64 TQFP package)	1.154 W	52˚ C/W	18˚ C/W

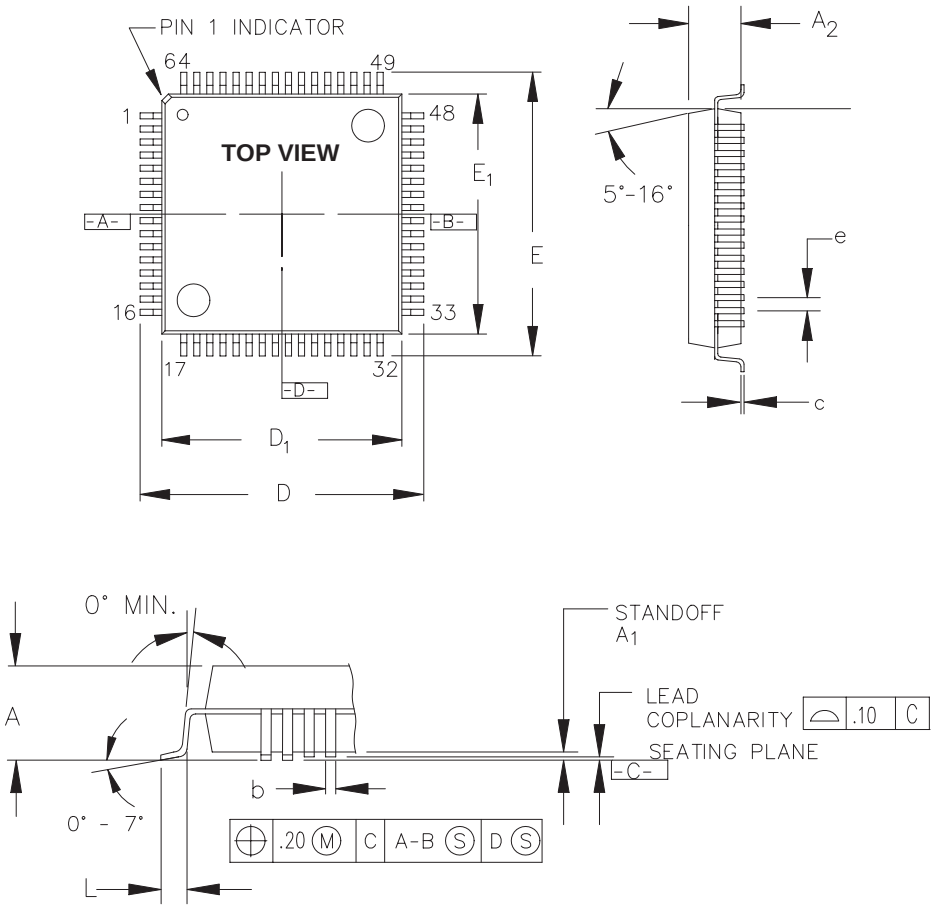
Figure 5. 10mm x 10mm 64 PQFP Package (S2060A)



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.25	1.95	13.00	9.90	13.00	9.90	0.78	0.50 BSC.	0.17	
NOM			2.00	13.20	10.00	13.20	10.00	0.88		0.22	
MAX	2.45	0.50	2.10	13.40	10.10	13.40	10.10	1.03		0.27	0.17

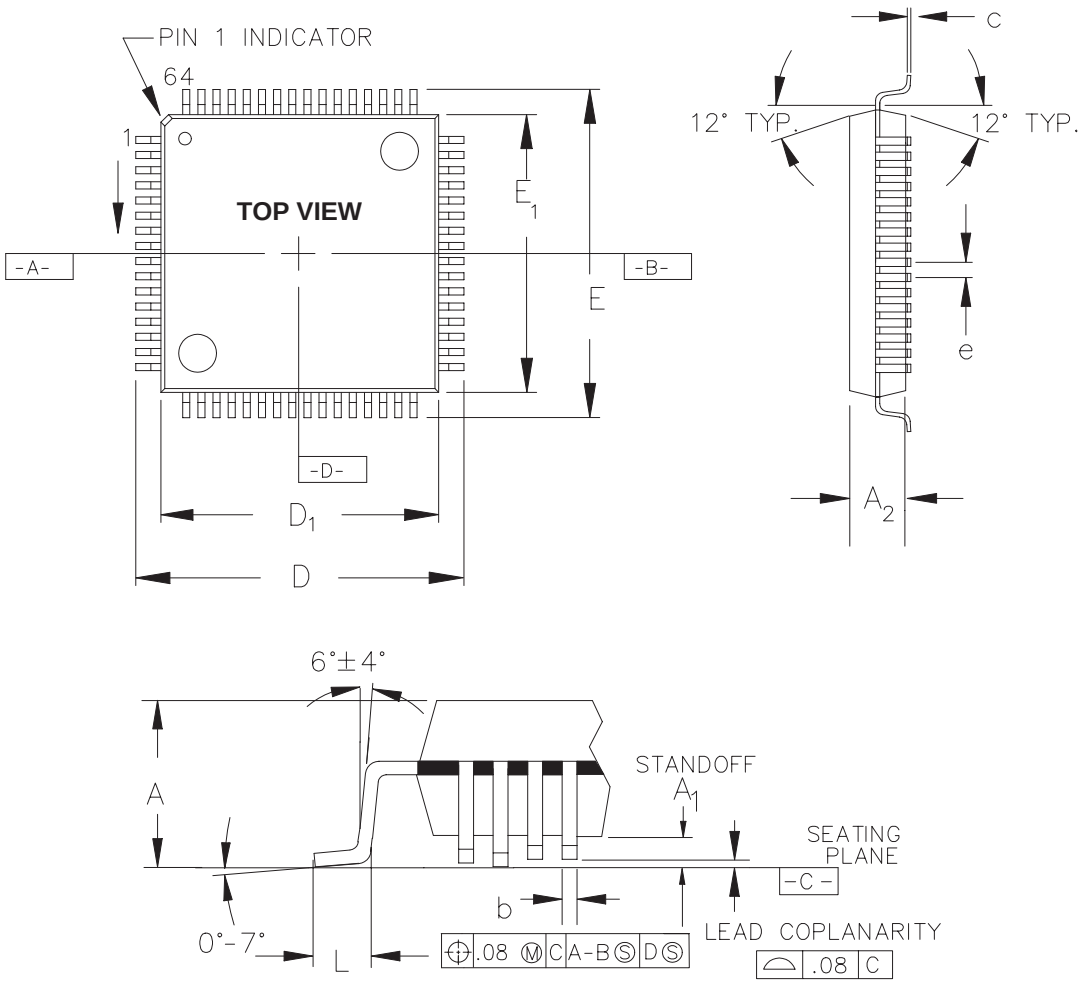
Figure 6. 14 mm x 14 mm 64 PQFP Package (S2060B)



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e	c
MIN			1.95	16.95	13.90	16.95	13.90	0.78	0.30	0.80 BSC.	
NOM			2.00	17.20	14.00	17.20	14.00	0.88	0.35		
MAX	2.35	0.25	2.10	17.45	14.10	17.45	14.10	1.03	0.45		0.17

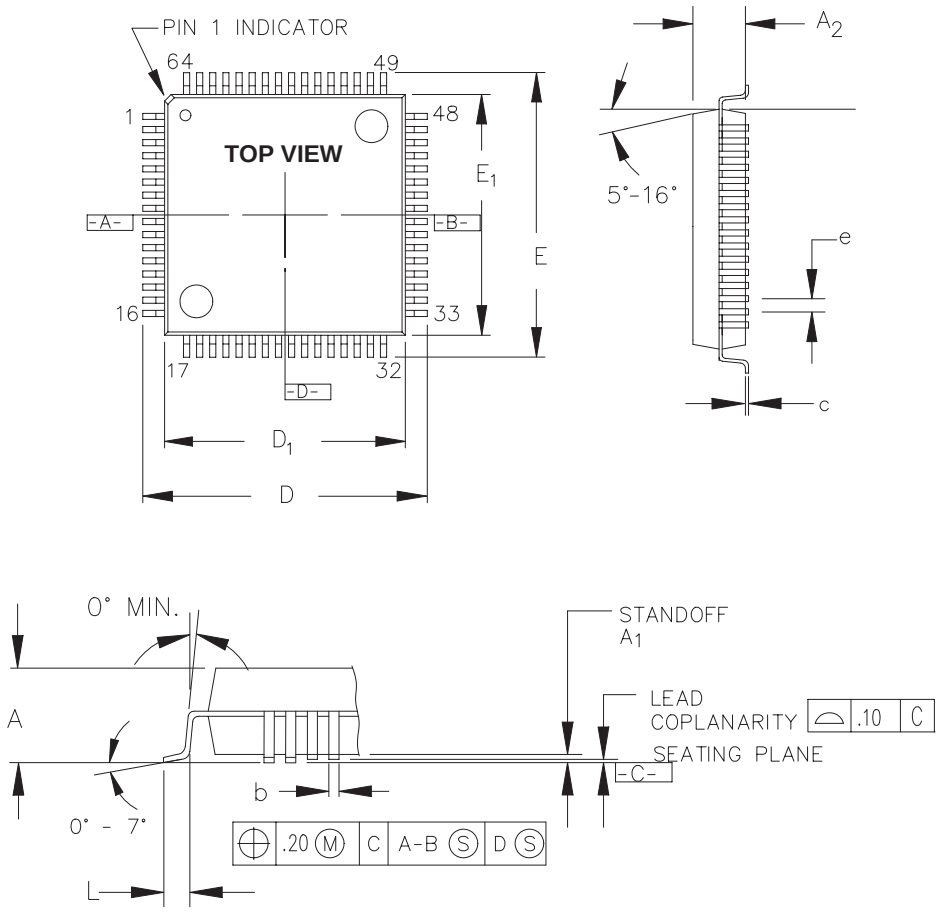
Figure 7. 10mm x 10mm 64 TQFP Package (S2060C)



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	11.80	9.90	11.80	9.90	0.50	0.50 BSC.	0.17	0.127
NOM			1.40	12.00	10.00	12.00	10.00	0.60		0.22	
MAX	1.60	0.15	1.45	12.20	10.10	12.20	10.10	0.75		0.27	0.17

Figure 8. 14 mm x 14 mm 64 PQFP Package (S2060D)



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	b	e	c
MIN			1.95	16.95	13.90	16.95	13.90	0.78	0.30	0.80 BSC.	
NOM			2.00	17.20	14.00	17.20	14.00	0.88	0.35		
MAX	2.35	0.25	2.10	17.45	14.10	17.45	14.10	1.03	0.45		0.17

Table 7. Power and Ground Application Information

Function	Pin Names	Instructions
ANALOG	AVCC	Connect to low noise or filtered +3.3 V supply through a ferrite bead (600 Ω at 100 MHz: Murrata BLM31B601S or equivalent). Provide dual local HF bypassing to AVEE (0.1 µF, 100 pF) for low inductance and resistance. A single low inductance 0.1 µF capacitor can be substituted for the pair (Vishay VJ0612 or equivalent, <0.5 nH max inductance).
	AVEE	Connect to ground plane.
LVPECL I/O	ECLIOVCC	Provide low impedance connection to +3.3 V. Provide dual local bypassing to GND plane (0.1 µF and 100 pF in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µF capacitor).
	ECLIOVEE	Connect to ground plane.
CORE	ECLVCC	Provide low impedance connection to +3.3 V. Provide dual local bypassing to GND plane (0.1 µF and 100 pF in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µf capacitor).
	ECLVEE	Connect to ground plane.
LVTTL I/O	TTLVCC	Provide low impedance connection to +3.3 V. Provide dual local bypassing to GND plane (0.1 µF and 100 pF in parallel, or a single low inductance Vishay VJ0612 or equivalent 0.1 µF capacitor).
	TTLVEE	Connect to ground plane.

Figure 9. Power and Ground Connection Diagram

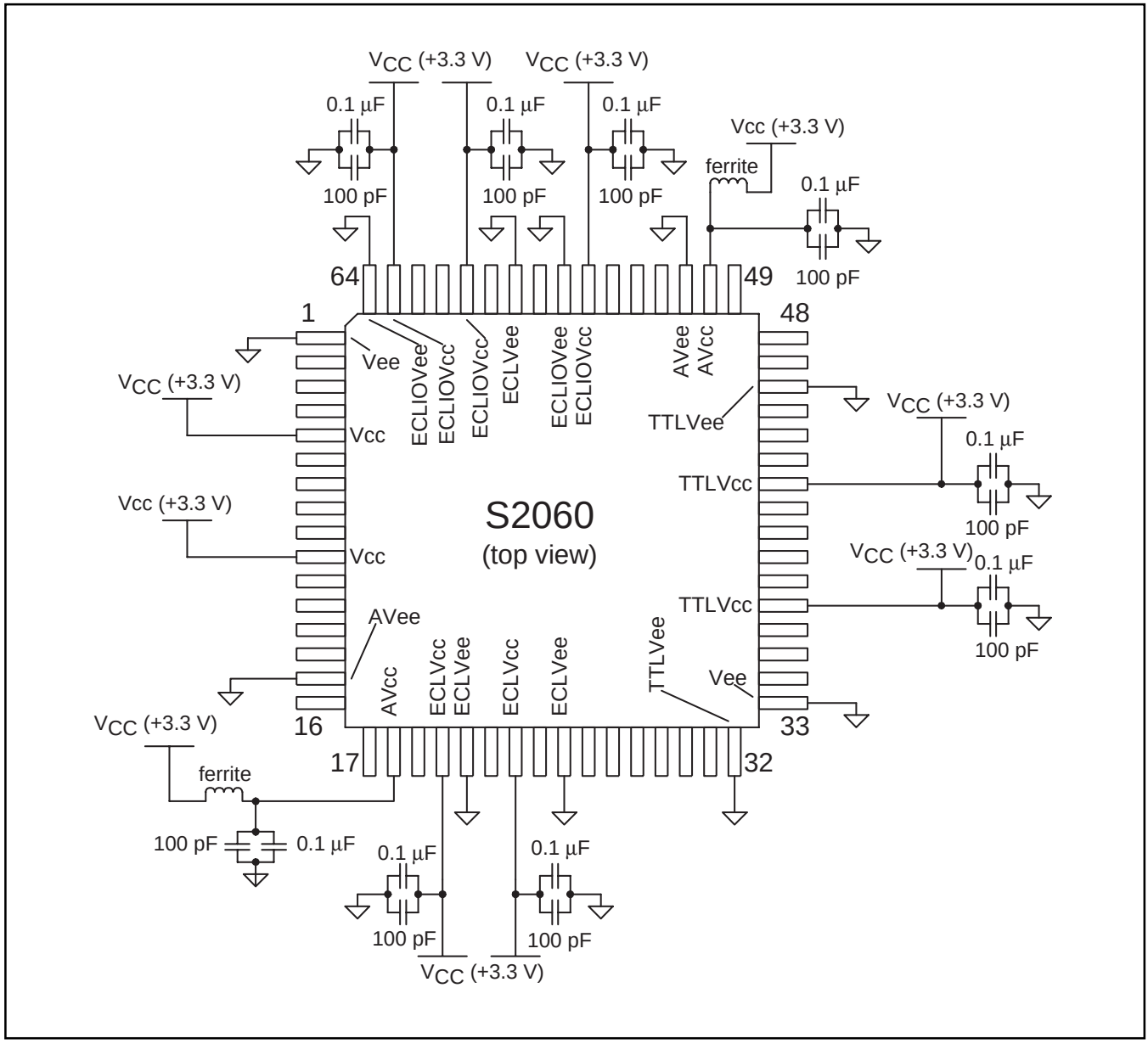


Figure 10. Transmitter Timing

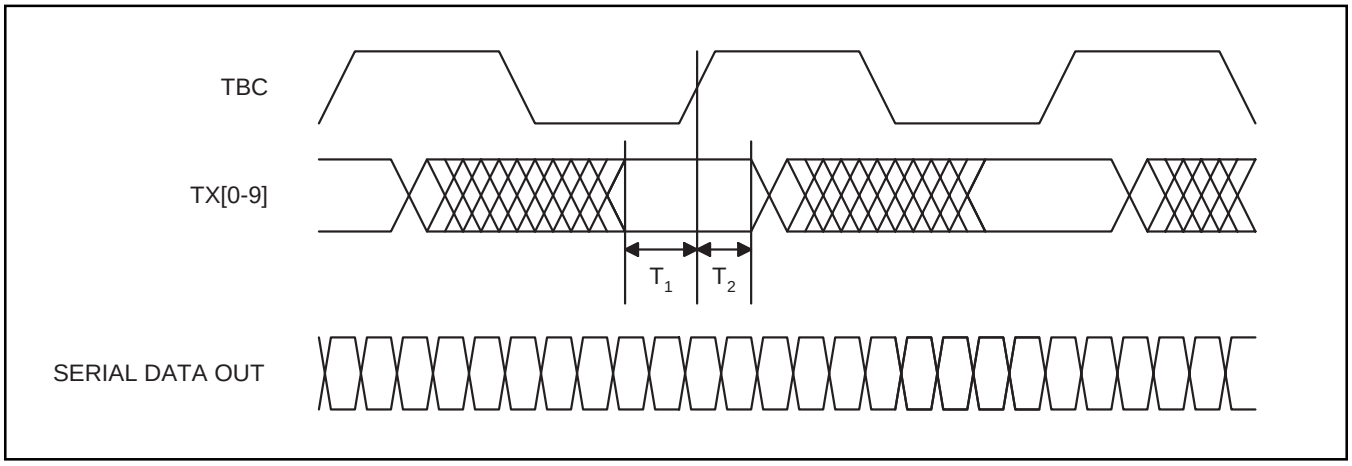


Table 8. S2060 Transmitter Timing

Parameters	Description	Min	Max	Units	Conditions
T_1	Data Setup w.r.t. ↑ TBC	1.2	-	ns	See Note 1.
T_2	Data Hold w.r.t. ↑ TBC	0.25	-	ns	
T_{SDR}, T_{SDF}	Serial Data Rise and Fall	-	270	ps	20% - 80%, tested on sample basis.
T_J	Serial Data Output total jitter (p-p)	-	192	ps	Peak-to-peak, measured on sample basis. Measured with ±K28.5 or 2^7-1 pattern at 1.25 GHz.
T_{DJ}	Serial Data Output deterministic jitter (p-p)	-	80	ps	Peak-to-peak, tested on a sample basis. Measured with ±K28.5 pattern at 1.25 GHz.

1. All AC measurements are made from the reference voltage level of the clock (+1.4 V) to the valid input or output data levels (+.8 V or +2.0 V).

Figure 11. Receiver Timing Full Rate Mode (RATEN Active)

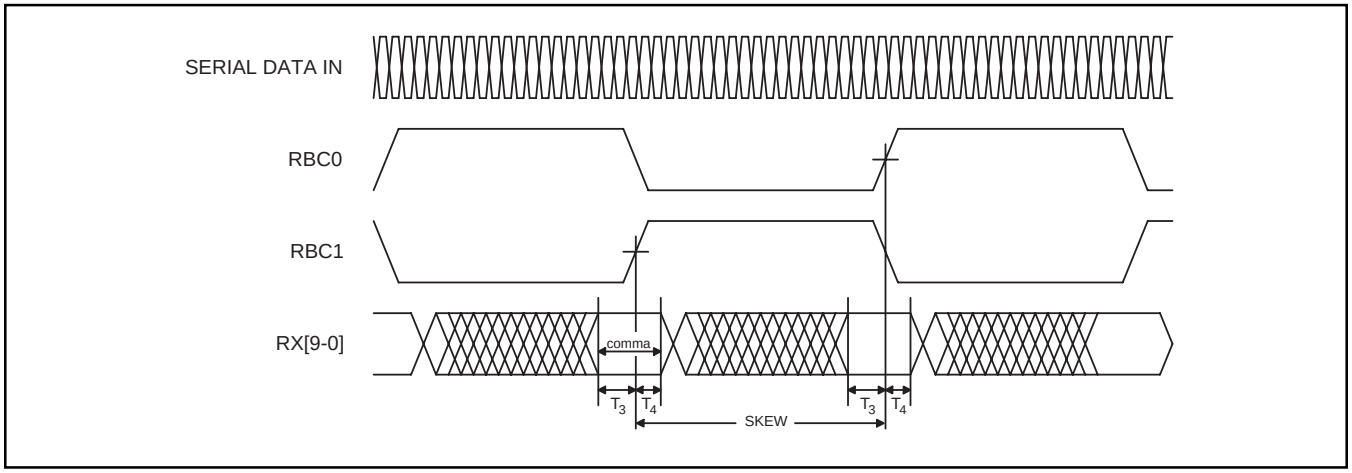


Figure 12. Receiver Timing Half Rate Mode (RATEN Inactive)

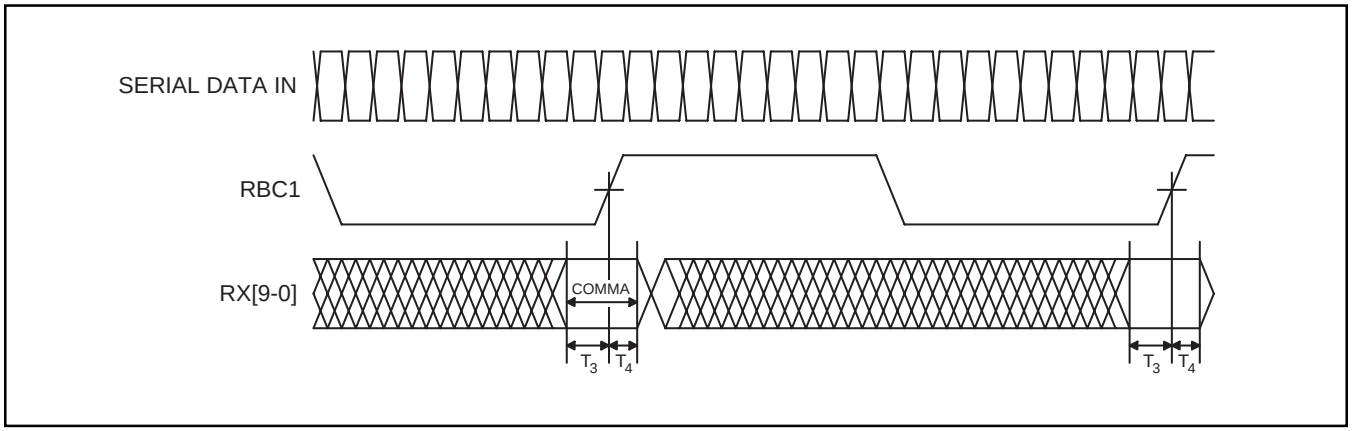


Table 9. S2060 Receiver Timing

Parameters	Description	Min	Max	Units	Conditions
T_3	Data valid before ↑ RBC1 (RBC0)	3.0	-	ns	See Note 1.
T_4	Data valid after ↑ RBC1 (RBC0)	2.0	-	ns	
T_{RCR}, T_{RCF}	RBC1, RBC0 Rise and Fall Time	-	2.4	ns	Measured +.8 V to +2.0 V.
Skew	RBC1 to RBC0 Skew	7.5	8.5	ns	Rising edge to rising edge.
T_{DR}, T_{DF}	Data Output Rise and Fall Time	-	2.4	ns	Measured +.8 V to +2.0 V.
T_{LOCK} (startup)	Startup acquision lock time (1.25G)	-	2.5	µs	
T_{LOCK} (reacquire)	Data Acquisition Lock Time (1.25G)	-	100	ns	90% input data eye (see Figure 19).
		-	250	ns	24% input data eye.
Duty Cycle	RBC1 (RBC0)	40	60	%	
T_J	Total Input Jitter Tolerance	599	-	ps	As specified in IEEE 802.3z.
T_{DJ}	Deterministic Input Jitter Tolerance	370	-	ps	As specified in IEEE 802.3z.

1. All AC measurements are made from the reference voltage level of the clock (+1.4 V) to the valid input or output data levels (+.8 V or +2.0 V).

OTHER OPERATING MODES

Loopback Mode

The S2060 supports internal loopback mode in which the serial data from the transmitter replaces external serial data. The loopback function is enabled when the loopback enable signal, EWRAP, is set ACTIVE.

The loopback mode provides the ability to perform system diagnostics and to perform off-line testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. Figure 13 shows the basic loopback operation.

Figure 13. Loopback Operation

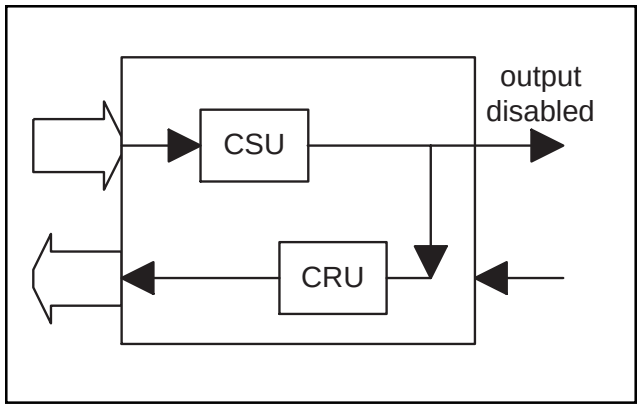


Table 10. Absolute Maximum Ratings

The following are the absolute maximum stress ratings for the S2060 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only and operation of the device at the maximums stated or any other conditions beyond those indicated in the "Recommended Operating Conditions" of the document are not inferred. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Min	Typ	Max	Units
Case Temperature Under Bias	-40		125	˚C
Junction Temperature Under Bias	-55		130	˚C
Storage Temperature	-65		150	˚C
Voltage on VCC with Respect to GND	-0.5		+4.0	V
Voltage on any TTL Input Pin except TBC	-0.5		5.0	V
Voltage on TBC	0		V_{CC}	V
Voltage on any LVPECL Input Pin	0		V_{CC}	V
TTL Output Sink Current			8	mA
TTL Output Source Current			8	mA

Table 11. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	0[1] -40[2]		70[1] 85[2]	˚C
Junction Temperature Under Bias			130	˚C
Voltage on TTLVCC, ECLVCC, ECLIOVCC, and AVCC with respect to GND/VEE	3.135	3.3	3.465	V
Voltage on any TTL Input Pin except TBC	0	V_{CC}	5.0	V
Voltage on any LVPECL Input Pin	V_{CC} -2.0		V_{CC}	V
Voltage on TBC	0		V_{CC}	V

1. Commercial temperature range S2060A, S2060B, S2060C.
2. Industrial temperature range S2060D.

Table 12. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time		2	ns	20% - 80%.
J_R	Random Jitter		100	ps	Peak to Peak.

Table 13. DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Comments
V_{OH}	Output High Voltage (TTL)	2.4	2.8	V_{CC}	V	V_{CC} = min, I_{OH} = 4 mA
V_{OL}	Output Low Voltage (TTL)	GND	0.1	0.4	V	V_{CC} = min, I_{OL} = 1 mA
V_{IH}	Input High Voltage (TTL)	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage (TTL)	GND		0.8	V	
I_{IH}	Input High Current (TTL)			40	µA	V_{IN} = 2.4 V, V_{CC} = Max
I_{IL}	Input High Current (TTL)			600	µA	V_{IN} = 0.0 V, V_{CC} = Max
I_{CC}	Supply Current		187	235	mA	Outputs open, square pattern.
P_D	Power Dissipation		620	820	mW	Outputs open, square pattern.
V_{DIFF}	Min. differential input voltage swing for differential LVPECL inputs	100		2200	mV	
ΔV_{OUT}	Serial Output Differential Voltage Swing	1200	2000	2200	mV	150 Ω to ground.
C_{IN}	Input Capacitance			3	pF	

OUTPUT LOAD

The S2060 serial outputs require a resistive load to set the output current. The recommended resistor value is 150 Ω to ground. This value can be varied to adjust drive current, signal voltage swing, and power usage on the board.

ACQUISITION TIME

With the input eye diagram shown in Figure 19, the S2060 will recover data with a 10E-9 BER within the time specified by T_{LOCK} in Table 9 after an instantaneous phase shift of the incoming data.

Figure 14. Serial Input Rise and Fall Time

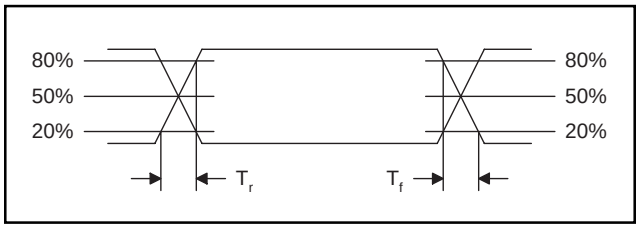


Figure 15. TTL Input/Output Rise and Fall Time

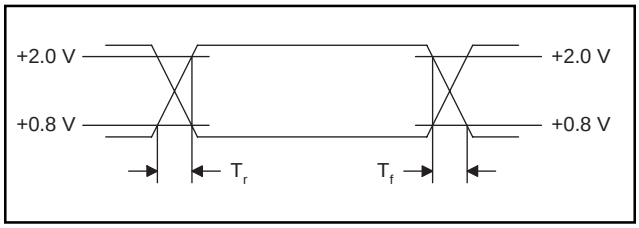


Figure 16. Serial Output Load

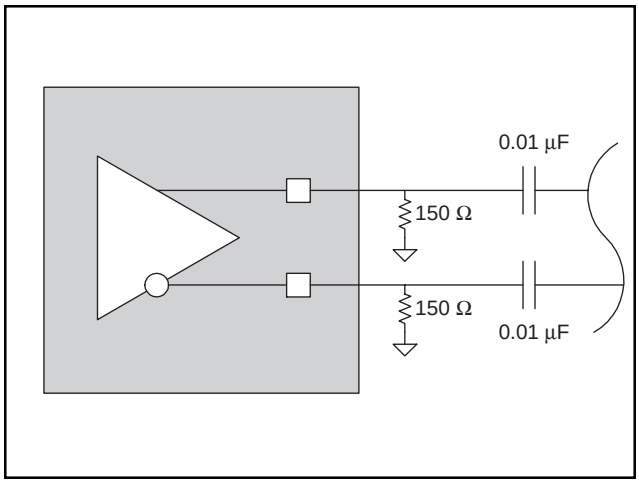


Figure 17. High Speed Differential Inputs

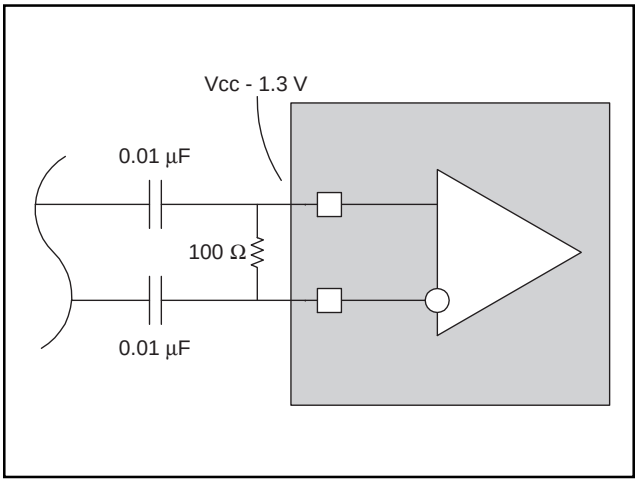


Figure 18. Receiver Input Eye Diagram Jitter Mask

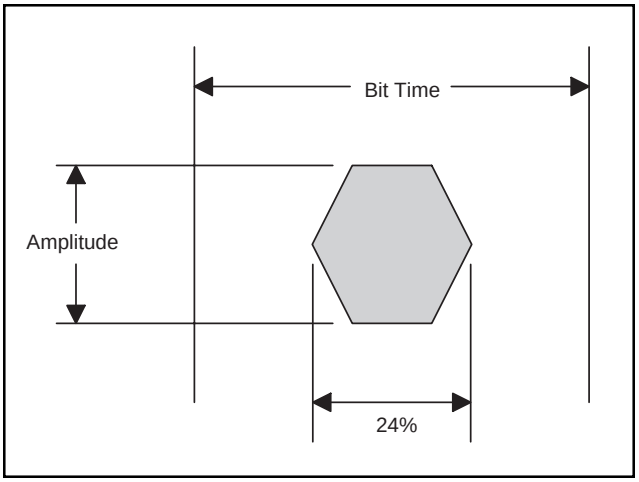
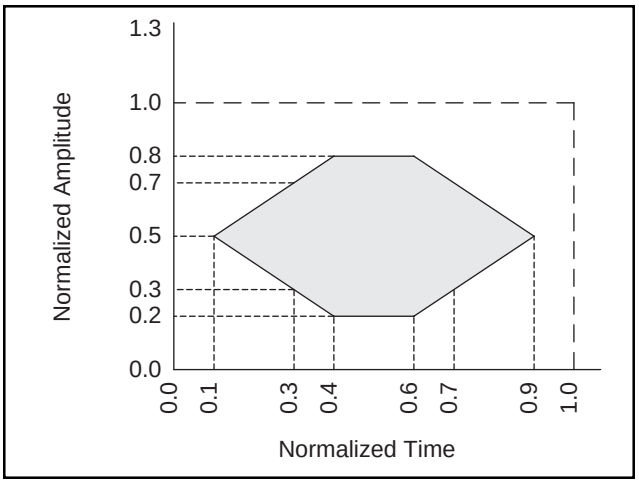
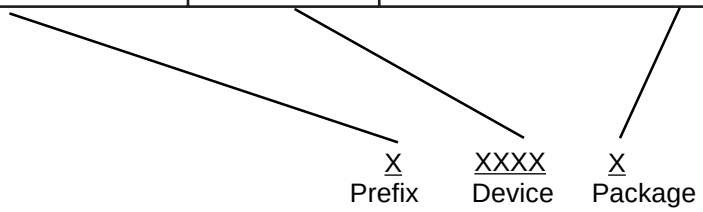


Figure 19. Acquisition Time Eye Diagram



Ordering Information

PREFIX	DEVICE	PACKAGE
S- Integrated Circuit	2060	A–(64 PQFP 10mm) Commercial Temp Range B–(64 PQFP 14mm) Commercial Temp Range C–(64 TQFP 10mm) Commercial Temp Range, loop filter pins option D–(64 PQFP 14mm) Industrial Temp Range



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