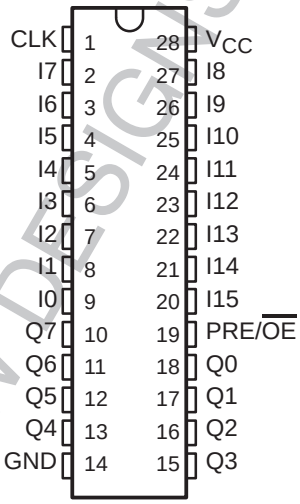
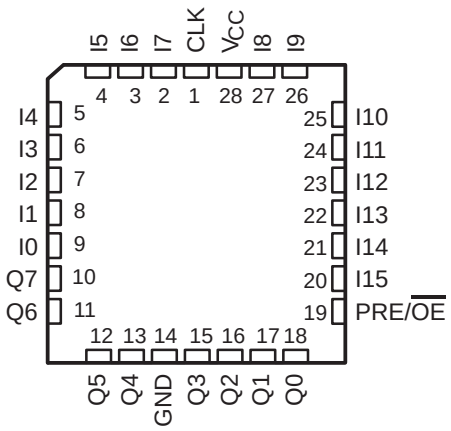
- **50-MHz Clock Rate**
- **Power-On Preset of All Flip-Flops**
- **6-Bit Internal State Register With 8-Bit Output Register**
- **Power Dissipation . . . 600 mW Typical**
- **Programmable Asynchronous Preset or Output Control**
- **Functionally Equivalent to, but Faster Than 82S105A†**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

The TIB82S105BC is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 14 pairs of sum terms (OR terms). The product and sum terms are used to control the 6-bit internal state register and the 8-bit output register.

The outputs of the internal state register (P0–P5) are fed back and combined with the 16 inputs (I0–I15) to form the AND array. In addition a single sum term is complemented and fed back to the AND array, which allows any of the product terms to be summed, complemented, and used as an input to the AND array.

The state and output registers are positive-edge-triggered S/R flip-flops. These registers are unconditionally preset high during power up. Pin19 can be used to preset both registers or, by blowing the proper fuse, be converted to an output control function.

The TIB82S105BC is characterized for operation from 0°C to 75°C.

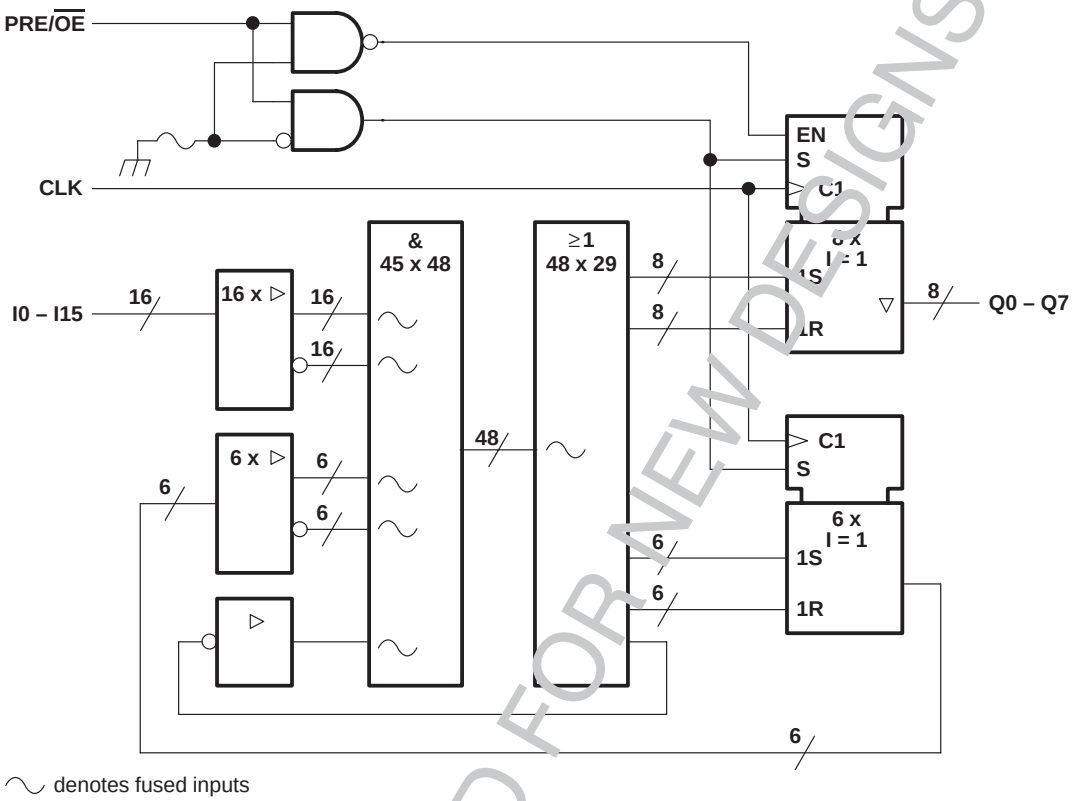
NOT RECOMMENDED FOR NEW DESIGNS

† Power-up preset and asynchronous preset functions are not identical to 82S105A. See Recommended Operating Conditions.

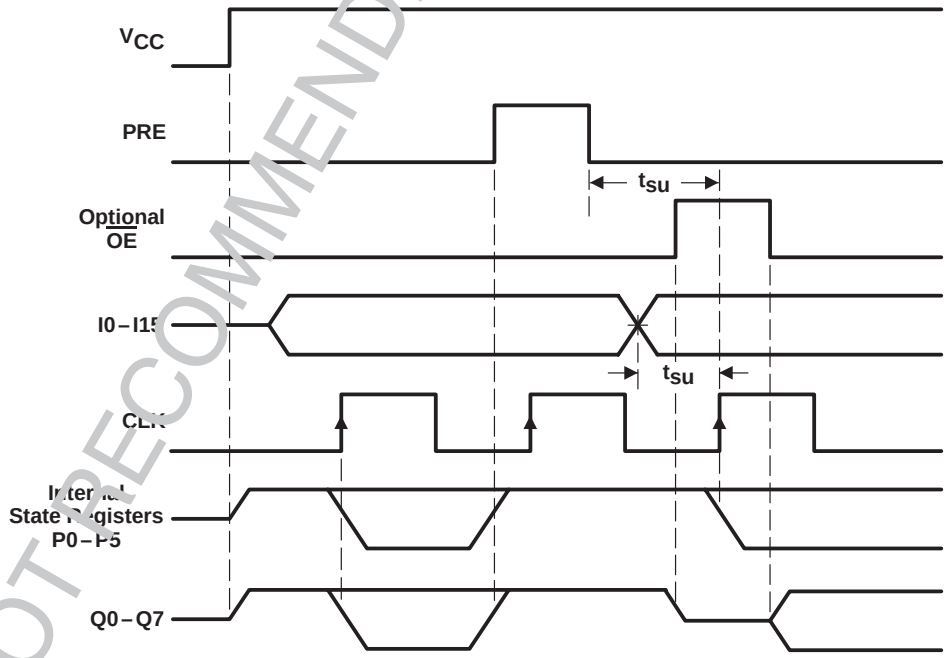
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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functional block diagram (positive logic)

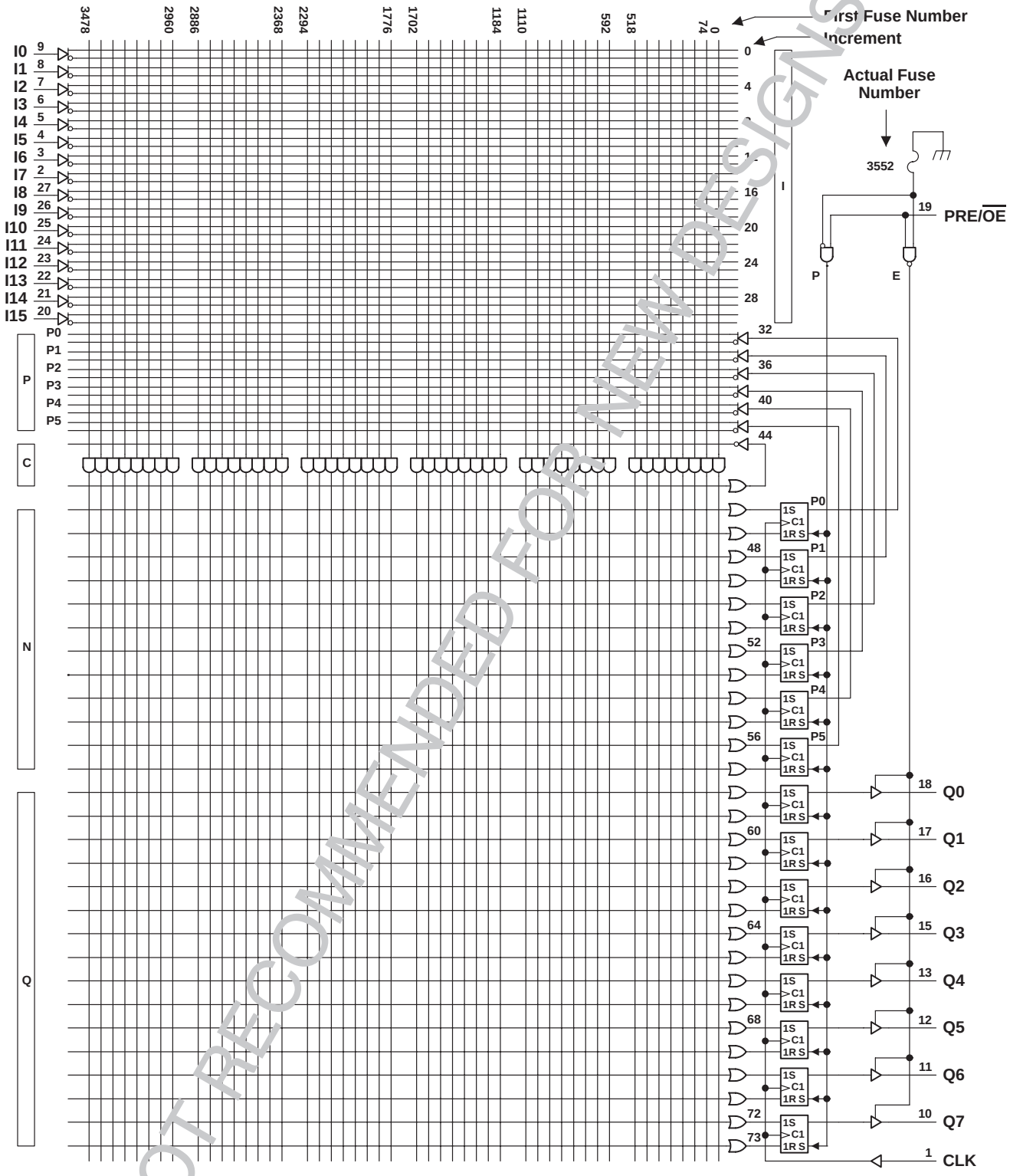


timing diagram



NOT RECOMMENDED FOR NEW DESIGNS

logic diagram (positive logic)



NOT RECOMMENDED FOR NEW DESIGNS

NOTES: 1. All AND gate inputs with a blown link float to the high level.
2. All OR gate inputs with a blown link float to the low level.
3. Fuse numbers = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) . . . . . 7 V
Input voltage (see Note 4) . . . . . 5.5 V
Voltage applied to disabled output (see Note 4) . . . . . 5.5 V
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 4: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array ‡	0		50	MHz
		1 thru 48 product terms with C-array	0		30	
t_w	Pluse duration	Clock high or low	10			ns
		Preset	15			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	15			ns
		With C-array	30			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		8			ns
t_h	Hold time, input after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

† The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡ The C-array is the single sum term that is complemented and fed back to the AND array.
§ After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

NOT RECOMMENDED FOR NEW DESIGNS

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA	2.4	3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.37	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V			20	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V			–20	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V			25	µA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V			–0.25	mA
I_O‡	V_{CC} = 5.25 V,	V_O = 2.25 V	–30		–112	mA
I_{CC}	V_{CC} = 5.25 V, PRE/$\overline{OE}$ at GND,	V_I = 4.7 V, Outputs open		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§	Without C array			50	70		MHz
	With C array			30	45		
t_{pd}	CLK↑	Q	R1 = 500 Ω,		8	15	ns
t_{pd}	PRE↑	Q	R2 = 500 Ω,		12	20	ns
t_{pd}	V_{CC}↑	Q	See Figure 5		0	10	ns
t_{en}	$\overline{OE}$↓	Q			10	20	ns
t_{dis}	$\overline{OE}$↑	Q			5	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions hace been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.
§ f_{max} is independent of the internal programmed configuration and the number of product terms used.

programming information

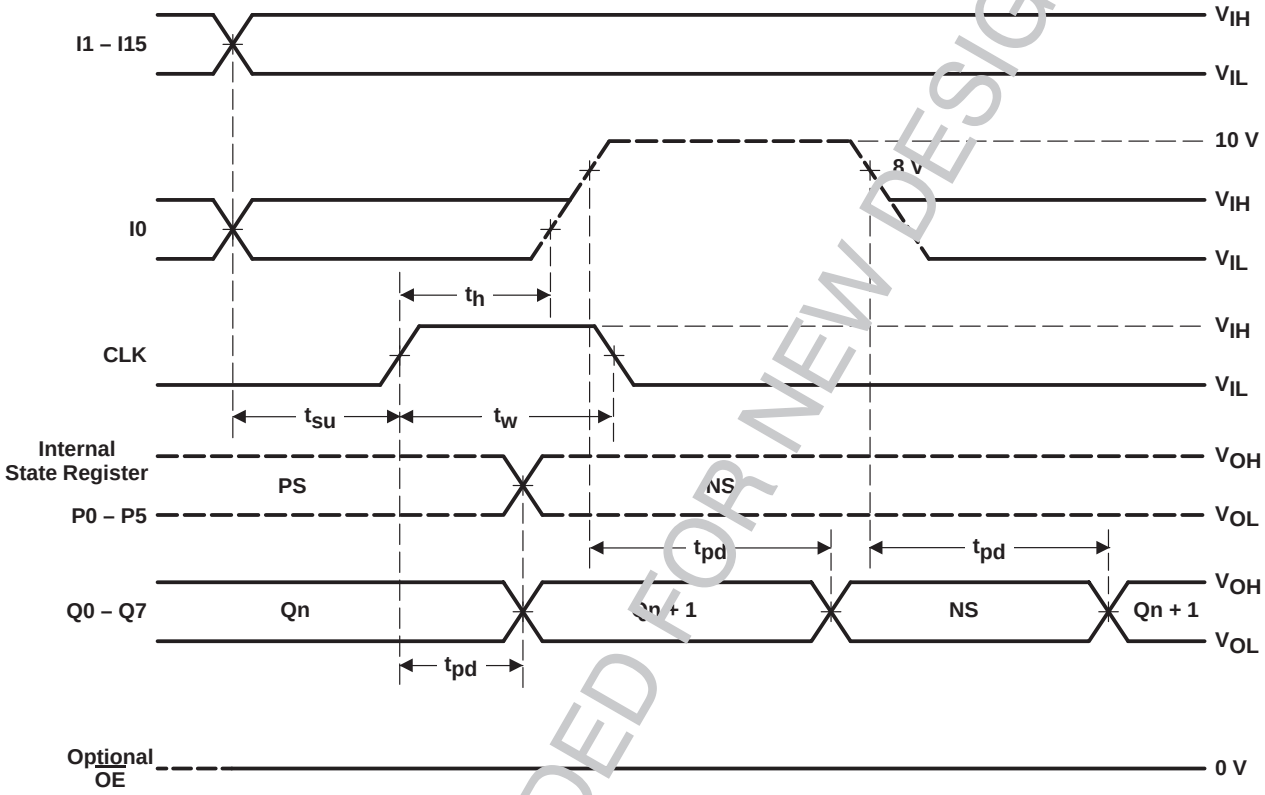
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NOT RECOMMENDED FOR NEW DESIGNS

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state register. When I0 (pin 9) is held at 10 V, the state register bits P0–P5 will appear at the Q0–Q5 outputs and Q6–Q7 will be high. The contents of the output register will remain unchanged.



PS = Present state, NS = Next state

Figure 1. Diagnostic Waveforms

NOT RECOMMENDED FOR NEW DESIGNS

test array

A test array that consists of product lines 48 and 49 has been added to these devices to allow testing prior to programming. The test array is factory programmed as shown in Table 1. Testing is accomplished by connecting Q0–Q7 to I8–I15, PRE/$\overline{OE}$ to GND, and applying the proper input signals as shown in Figure 2. Product lines 48 and 49 must be deleted during user programming to avoid interference with the programmed logic function.

Table 1. Test Array Program

PRODUCT LINE	AND																						OPTION PRE/$\overline{OE}$	H														
			INPUT (In)																PRESENT STATE (PS)						OR														
	C	$\overline{C}$	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	Q5	Q4	Q3	Q2	Q1	Q0	NEXT STATE (NS)						OUT (Qn)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	X	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
49	–	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H

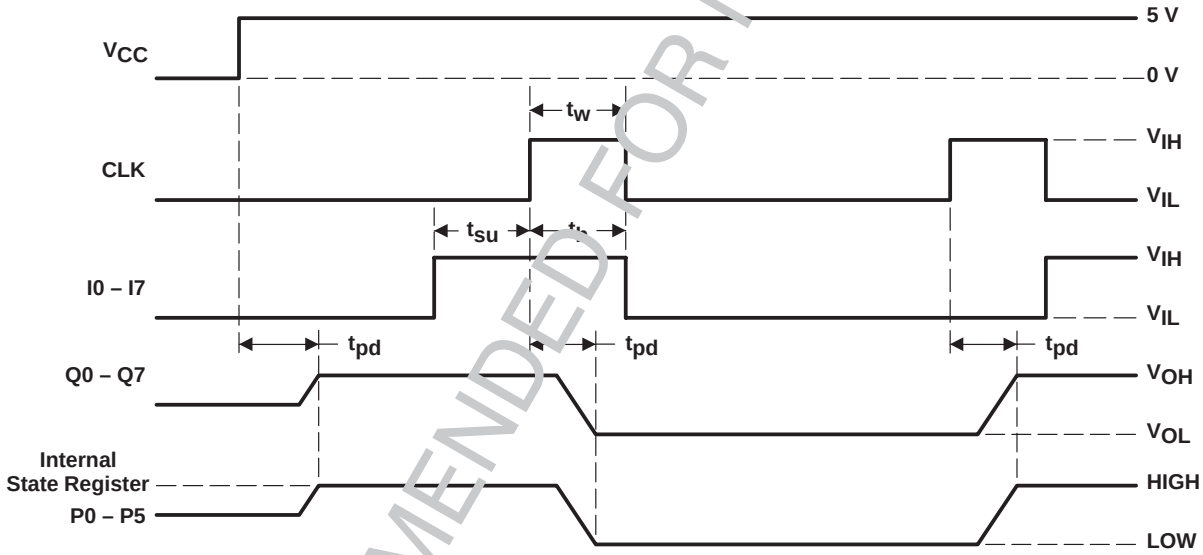


Figure 2. Test Array Waveforms

Table 2. Test Array Deleted

PRODUCT LINE	AND																						OPTION PRE/$\overline{OE}$	H														
			INPUT (In)																PRESENT STATE (PS)						OR														
	C	$\overline{C}$	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0	Q5	Q4	Q3	Q2	Q1	Q0	NEXT STATE (NS)						OUT (Qn)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	–	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
49	–	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	–	–	–	–	–	–	–	–	–	–	–	–	–	–

X = Fuse intact – = Fuse blown

NOT RECOMMENDED FOR NEW DESIGNS

TIB82S105B, 82S105A COMPARISON

The Texas Instruments TIB82S105B is a 16 × 48 × 8 Field-Programmable Logic Sequencer that is functionally equivalent to the Signetics 82S105A. However, the TIB82S105B is designed for a maximum speed of 50 MHz with the preset function being made conventional. As a result the TIB82S105B differs from the 82S105A in speed and in the preset recovery function.

The TIB82S105B is a high-speed version of the original 82S105A. The TIB82S105B features increased switching speeds with no increase in power. The maximum operating frequency is increased from 20 MHz to 50 MHz and does not decrease as more product terms are connected to each sum (OR) line. For instance, if all 48 product tems were connected to a sum line on the original 82S105A, the f_{max} would be about 15 MHz. The f_{max} for the TIB82S105B remains at 50 MHz regardless of the programmed configuration. In addition, the preset recovery sequence was changed to a conventional recovery sequence, providing quicker clock recovery times. This is explained in the following paragraph.

The TIB82S105B and the 82S105A are equipped with power-up preset and asynchronous preset functions. The power-up preset causes the registers to go high during power up. The asynchronous preset inhibits clocking and causes the registers to go high whenever the preset pin is taken high. After a power-up preset occurs, the minimum setup time from power up to the first clock pulse must be met in order to assure that clocking is not inhibited. In a similar manner after an asynchronous preset, the preset input must return low (inactive) for a given time, t_{su}, before clocking.

The Signetics 82S105A was designed in such a way that after both power-up preset and asynchronous preset it requires that a high-to-low clock transition occur before a clocking transition (low-to-high) will be recognized. This is shown in Figure 3. The Texas Instruments TIB82S105B does not require a high-to-low clock transition before clocking can be resumed, it only requires that the preset be inactive 8 ns (preset inactive-state setup time) before the clock rising edge. See Figure 4.

The TIB82S105B, with an f_{max} of 50 MHz, is ideal for systems in which the state machine must run several times faster than the system clock. It is recommended that the TIB82S105B be used in new designs. ***However, if the TIB82S105B is used to replace the 82S105A, then the customer must understand that clocking will begin with the first clock rising edge after preset.***

Table 3. Speed Differences

PARAMETER	82S105A SIGNETICS	TIB82S105B TI ONLY
f_{max}	20 MHz	50 MHz
t_{pd}, CLK to Q	20 ns	15 ns

NOT RECOMMENDED FOR NEW DESIGNS

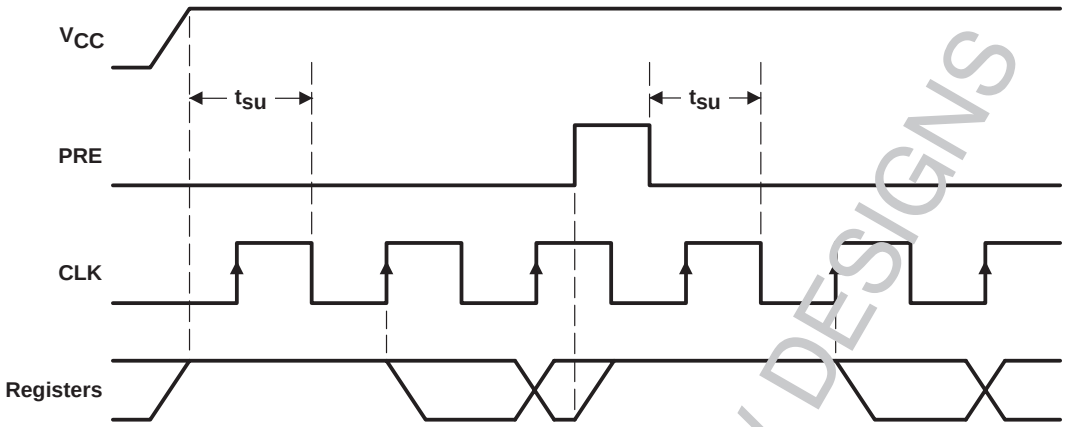


Figure 3. 82S105A Preset Recovery Operation

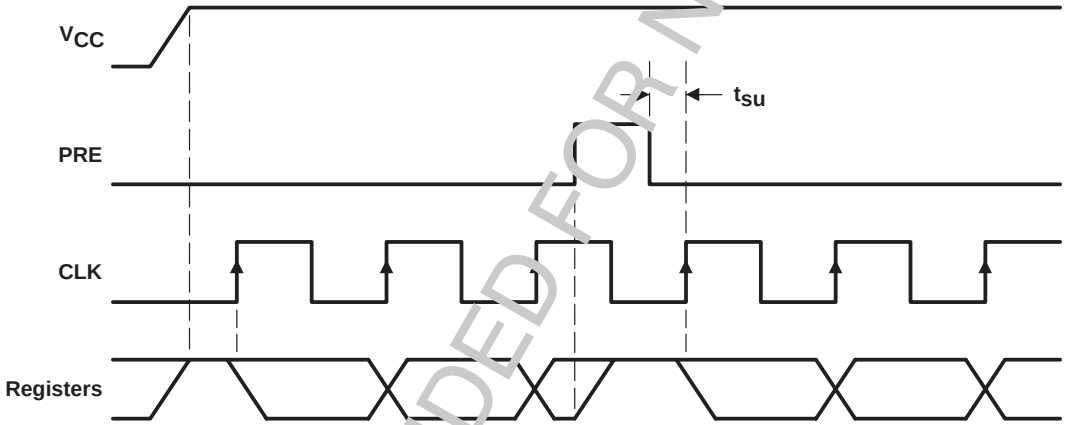
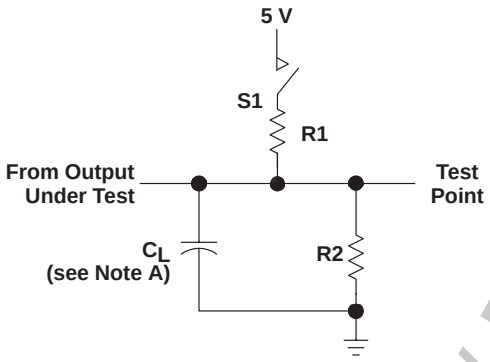


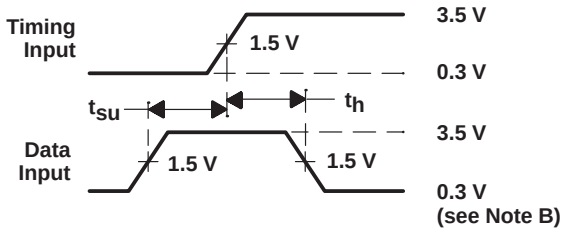
Figure 4. TIB82S105B Preset Recovery Operation

NOT RECOMMENDED FOR NEW DESIGNS

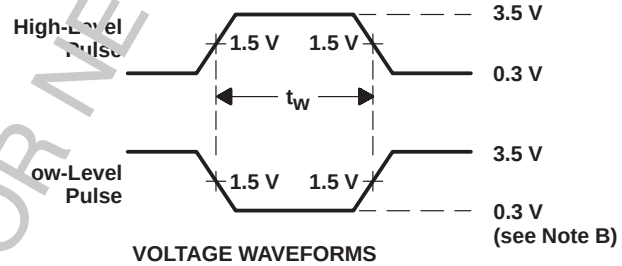
PARAMETER MEASUREMENT INFORMATION



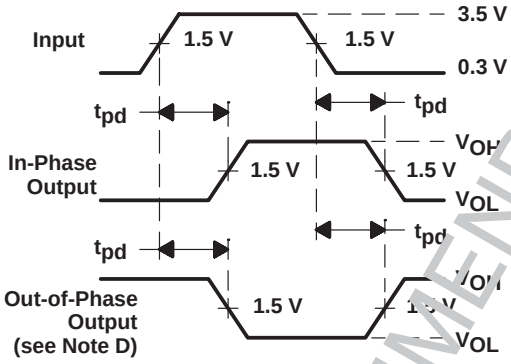
LOAD CIRCUIT FOR
3-STATE OUTPUTS



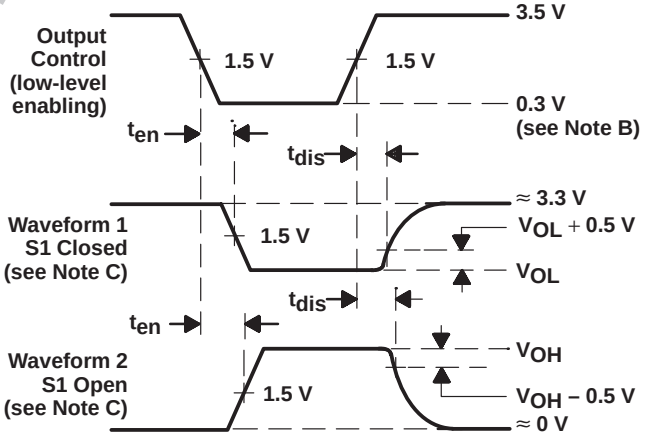
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 5. Load Circuit and Voltage Waveforms

NOT RECOMMENDED FOR NEW DESIGNS

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TIB82S105BCFN	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI
TIB82S105BCN	OBSOLETE	PDIP	N	28		TBD	Call TI	Call TI

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OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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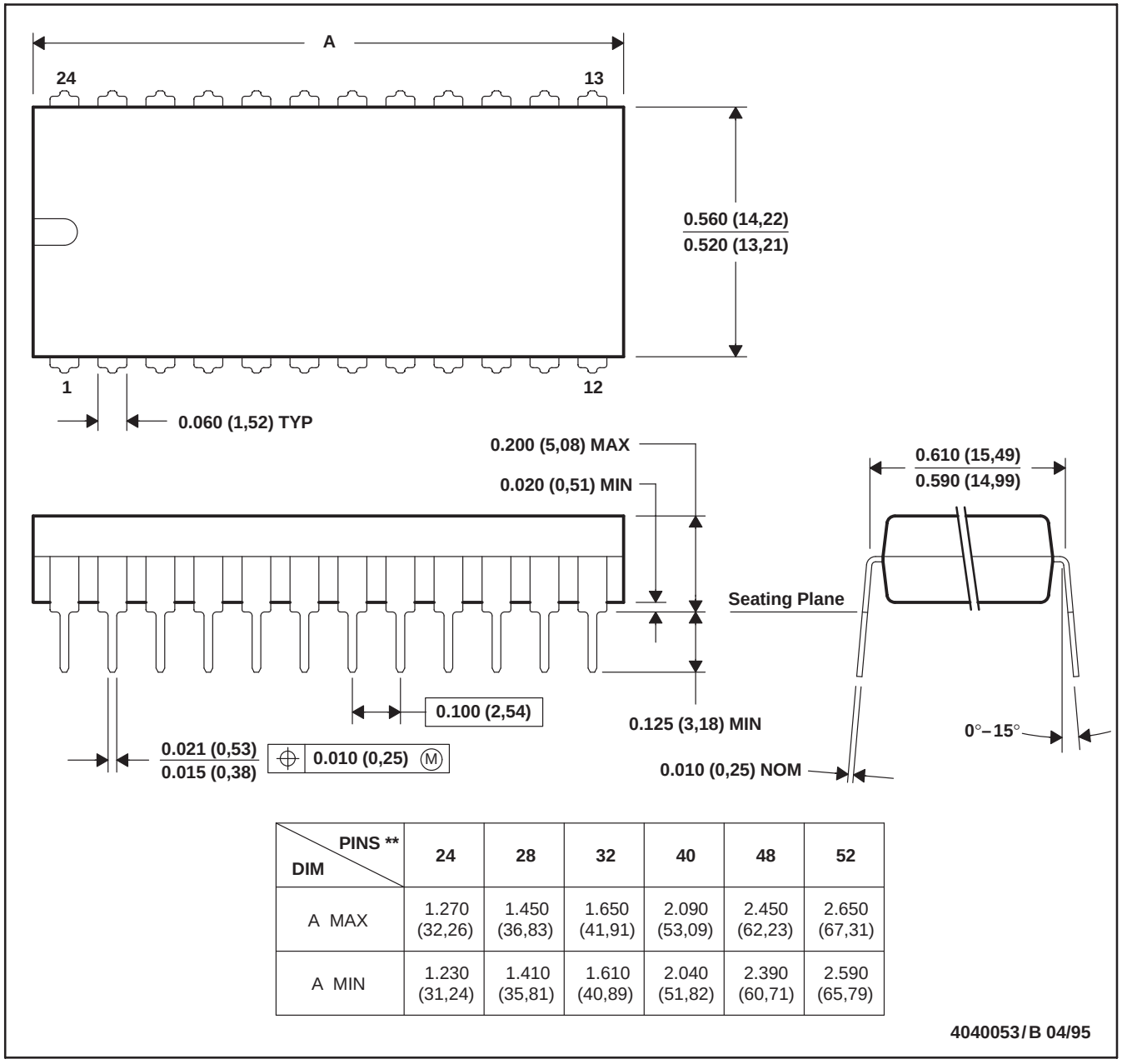
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MPDI008 – OCTOBER 1994

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B 04/95

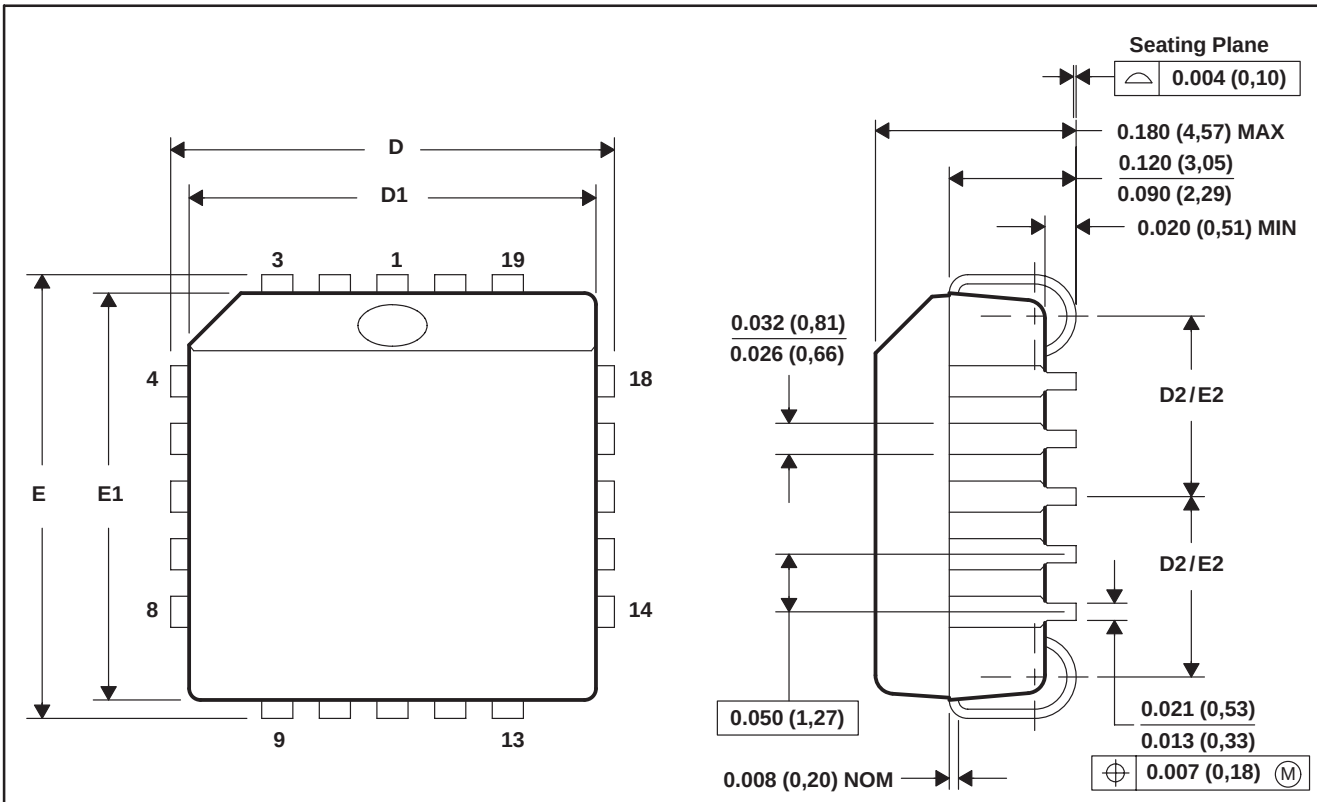
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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