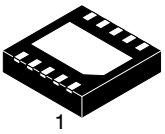
P1P8160A

Low Jitter Clock Generator and Peak EMI Reduction IC

ON Semiconductor®

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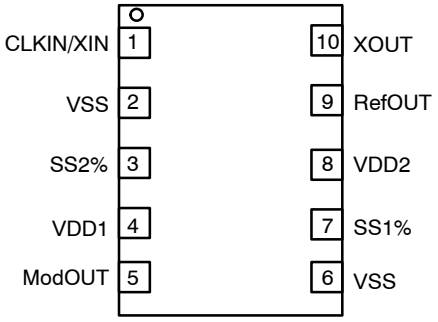
WDFN10
CASE 511BK

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONFIGURATION



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

Product Description

P1P8160A is a versatile low jitter clock generator and spread spectrum frequency modulator designed to reduce electromagnetic interference (EMI) at the clock source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The device allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

P1P8160A modulates the output of a PLL in order to “spread” the bandwidth of a synthesized clock, and more importantly, decreases the peak amplitudes of its harmonics. This results in significantly lower system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal’s bandwidth is called ‘spread spectrum clock generation’.

P1P8160A accepts an input from either a 27 MHz fundamental Crystal or from an external reference clock and generates a 100 MHz Spread Spectrum clock. The device also features a 27MHz reference clock output. Two Tri−level logic pins, SS1% and SS2% enables selecting one of the eight different frequency deviations along with SSOFF. Refer to *Frequency Deviation Selection table.* P1P8160A operates over a supply voltage range of 3.3 V ± 10%. P1P8160A is available in a 10 Pin WDFN (3 mm x 3 mm) package, over temperature range −10°C to +85°C.

Features

- LVCMOS Peak EMI Reduction
- Input clock Frequency:
  27 MHz: External Crystal or Reference Clock
- Output clock Frequencies:
  100 MHz Spread Spectrum Clock
  27 MHz Refout
- Two Tri−level Logic Pins for Selecting Eight Different Frequency Deviations Along with SSOFF
- Modulation Rate at 100 MHz: 32 kHz
- Low Cycle−Cycle Jitter, LT Jitter
- Supply voltage: 3.3 V ± 10%
- Temperature Range: −10°C to +85°C
- 10 Pin WDFN, 3 mm x 3 mm Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Application

- P1P8160A is targeted for use in a broad range of notebook, desktop and embedded digital applications.

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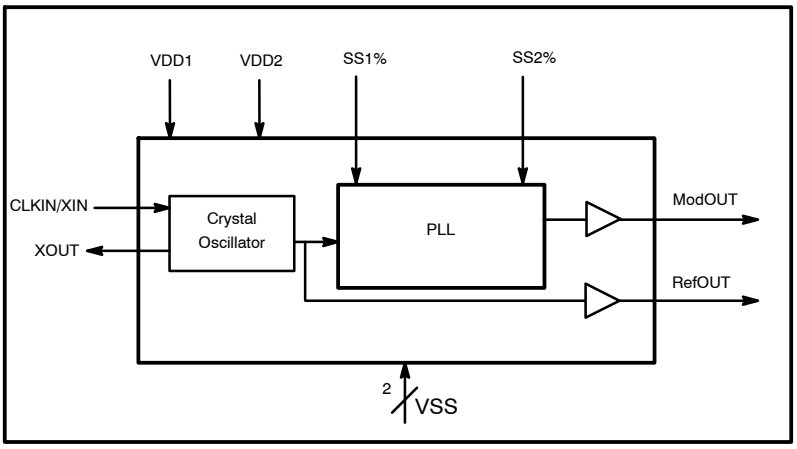


Figure 1. Block Diagram

Table 1. PIN DESCRIPTION

Pin#	Pin Name	Type	Description
1	CLKIN / XIN	I	Crystal connection or External Reference Clock Input.
2	VSS	P	Ground to entire chip
3	SS2%	I	Frequency Deviation Selection. Tri−level logic pin. Has an internal pull down resistor. Refer to *Frequency Deviation Selection table*
4	VDD1		Supply Voltage for 100 MHz ModOUT
5	ModOUT	O	Buffered 100MHz spread spectrum clock output
6	VSS	P	Ground to entire chip
7	SS1%	I	Frequency Deviation Selection. Tri−level logic pin. Has an internal pull down resistor. Refer to *Frequency Deviation Selection table*
8	VDD2	P	Supply Voltage for 27 MHz RefOUT
9	RefOUT	O	Buffered reference clock output
10	XOUT	O	Crystal connection. If using an external reference, this pin must be left unconnected.

3 Level Digital Logic

SS1% and SS2% digital inputs are designed to sense 3 different logic levels designated as High “1”, Low “0” and Middle “M”. With this 3−Level digital inputs, 9 different logic states can be detected.

Use 5k/5k resistor divider at SS1% and SS2% pins from V_{DD} to V_{SS} to obtain $V_{DD}/2$, Middle “M” logic level as shown:

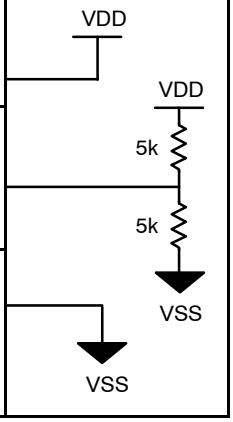
Logic	Control Pins	
1	SS1%, SS2% to V_{DD}	
M	SS1%, SS2%	
0	SS1%, SS2% to V_{SS} (UNCONNECTED)	

Table 2. FREQUENCY DEVIATION SELECTION TABLE

SS2% (Pin#3)	SS1% (Pin#7)	Deviation at 100 MHz (%) (Pin#5)	ModRate (kHz)
L	L	SSOFF	32
L	M	−0.5	
L	H	−2.5	
M	L	−0.25	
M	M	−0.75	
M	H	−1	
H	L	−1.5	
H	M	−2	
H	H	−3	

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Voltage on any pin with respect to VSS	2.97	3.63	V
T_A	Operating Temperature	−10	+85	°C
C_L	Load Capacitance		15	pF
C_{IN}	Input Capacitance		7	pF

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
V_{DD}, V_{IN}	Voltage on any pin with respect to Ground	−0.5 to +4.6	V
T_{STG}	Storage Temperature	−65 to +125	°C
T_s	Max. Soldering Temperature (10 sec)	260	°C
T_J	Junction Temperature	150	°C
T_{DV}	Static Discharge Voltage (As per JEDEC STD 22− A114−B)	2	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3 V ± 10%, Ambient Temperature Range: −10°C to +85°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Supply Voltage		2.97	3.3	3.63	V
V_{IL}	Input Low Voltage (CLKIN/XIN, SS1%, SS2% Inputs)		0		0.2	V
V_{IM}	Input Middle Voltage (SS1%, SS2% Inputs)		0.4 x V_{DD}		0.6 x V_{DD}	V
V_{IH}	Input High Voltage (CLKIN/XIN, SS1%, SS2% Inputs)		0.9 x V_{DD}		V_{DD}	V
V_{OL}	Output Low Voltage (ModOUT, RefOUT)	I_{OL} = 15 mA			0.4	V
V_{OH}	Output High Voltage (ModOUT, RefOUT)	I_{OH} = −15 mA	2.4			V
I_{DD}	Dynamic Supply Current (C_L = 15 pF, V_{DD} = 3.63 V, T = +85°C)				22	mA
C_{IN1}	Input Capacitance (XIN and XOUT)			6.0		pF
C_{IN2}	Input Capacitance (SS1%, SS2% Inputs)				7.0	pF
R_{PD}	Pull Down Resistor (SS1%, SS2% Inputs)		100	200	250	kΩ

NOTE: The voltage on any input or I/O pin cannot exceed the power pin during power up.

Table 6. AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3 V ± 10%, Ambient Temperature Range: −10°C to +85°C unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit
f_{IN}	Input Clock frequency (Tolerance: ±10ppm)			27		MHz
f_{OUT}	ModOUT Clock frequency (SS1% & SS2% = 0) (Tolerance: ±30ppm)			100		MHz
	RefOUT Clock frequency (Tolerance: ±30ppm)			27		
t_{LH}, t_{HL} (Note 2)	RefOUT Rise and Fall time (Measured between 20% to 80%)	C_L = 5 pF		0.75	1.5	ns
		C_L = 15 pF		1.25	2.0	
t_{LH}, t_{HL} (Note 2)	ModOUT Rise and Fall time (Measured between 20% to 80%)	C_L = 5 pF		0.75	1.0	ns
		C_L = 15 pF		1.25	1.75	
T_{DCOUT} (Notes 1, 2)	Output Clock Duty Cycle		45	50	55	%
T_{JC} (Notes 1, 2)	Cycle−Cycle Jitter (For ModOUT, RefOUT)			125	200	ps
T_{JL} (Notes 1, 2)	Long Term Jitter (10k cycles)	27 MHz, RefOUT		150	300	
		100 MHz ModOUT (SSOFF)		350	600	
t_{ON} (Notes 1, 2)	Power Up Time (Stable power supply, valid input clock to valid Clock on ModOUT).				5	ms
$t_{SS\%}$ (Notes 1, 2)	Spread Percentage Setting Time (Time from SS1%/SS2% change to stable ModOUT with change in spread %)				1	ms
MF (Notes 1, 2)	Modulation Frequency		31	32	33	kHz
FMTSR (Notes 1, 2)	Frequency Modulation Type and Slew Rate (Triangular Modulation Profile)				0.125	%/μs

1. Parameters are specified with 15 pF loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production

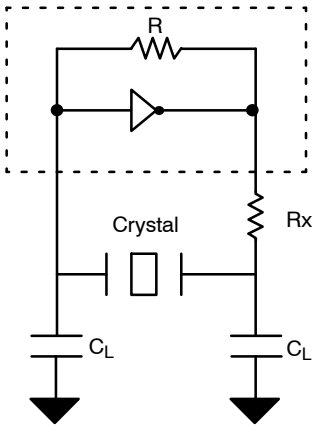


Figure 2. Typical Crystal Interface Circuit

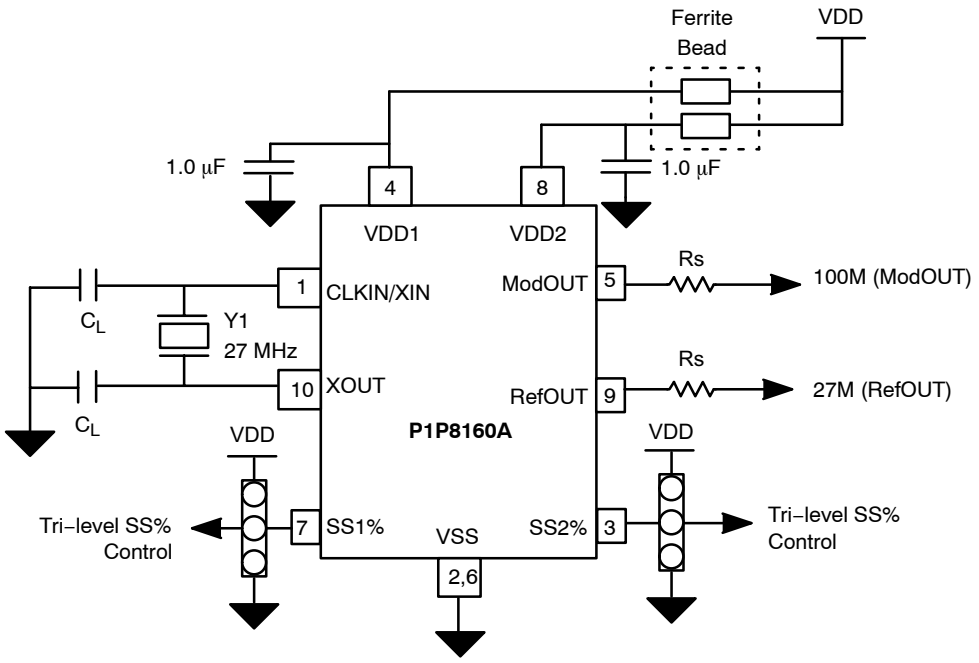
$C_L = 2 * (C_P - C_S)$,

Where C_P = Load capacitance of crystal specified in a Crystal Datasheet

C_S = Stray capacitance due to C_{IN}, PCB, Trace etc.

C_L = Load capacitance to be used

Rx is used to reduce power dissipation in the Crystal



NOTE: Refer Pin Description table for Functionality details

Figure 3. Typical Application Schematic

ORDERING INFORMATION

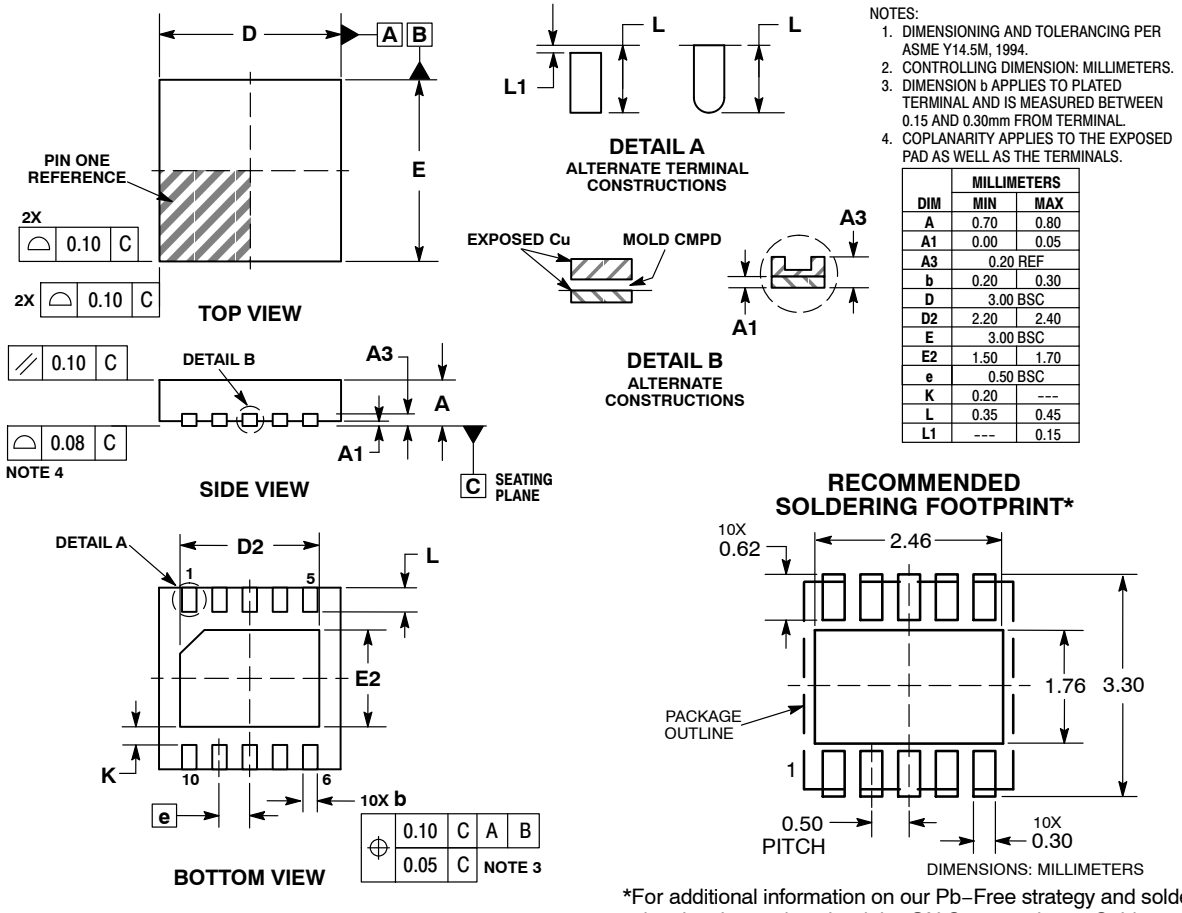
Part Number	Top Marking	Temperature	Package	Shipping†
P1P8160AG−10CR	1P 8160A	−10°C to +85°C	10 pin (3 mm x 3 mm) WDFN	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*A “microdot” placed at the end of last row of marking or just below the last row toward the center of package indicates Pb−Free.

PACKAGE DIMENSIONS

WDFN10 3x3, 0.5P
CASE 511BK−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	3.00 BSC	
D2	2.20	2.40
E	3.00 BSC	
E2	1.50	1.70
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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