23V, 3.5A, 340KHz Synchronous Step-Down DC/DC Converter

Description

The FR9888C is a synchronous step-down DC/DC converter that provides wide 4.5V to 23V input voltage range and 3.5A continuous load current capability.

The FR9888C fault protection includes cycle-by-cycle current limit, input UVLO, output over voltage protection and thermal shutdown. Besides, adjustable soft-start function prevents inrush current at turn-on. This device uses current mode control scheme which provides fast transient response. In shutdown mode, the supply current is less than 1μA.

The FR9888C is available in SOP-8 exposed pad package, provides a very compact system solution and good thermal conductance.

Features

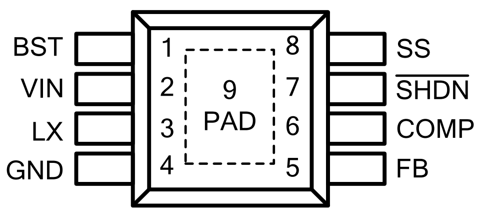
- High Efficiency up to 96%
- Low Rds(on) Integrated Power MOSFET (110mΩ/80mΩ)
- Wide Input Voltage Range: 4.5V to 23V
- Adjustable Output Voltage Range: 0.925V to 20V
- 3.5A Output Current
- Fixed 340kHz Switching Frequency
- Current Mode Operation
- External Compensation Function
- Adjustable Soft-Start
- Cycle-by-Cycle Current Limit
- Input Under Voltage Lockout
- Over-Temperature Protection with Auto Recovery
- <1μA Shutdown Current
- SOP-8 Exposed Pad Package

Applications

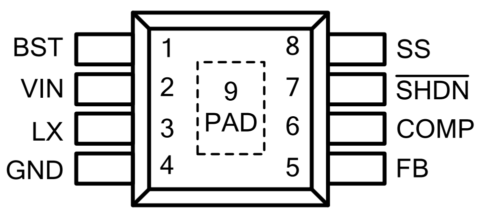
- Set-Top-Box (STB)
- LCD Displays, TV
- Distributed Power System
- XDSL Modem

Pin Assignments

SP Package (SOP-8 Exposed Pad)



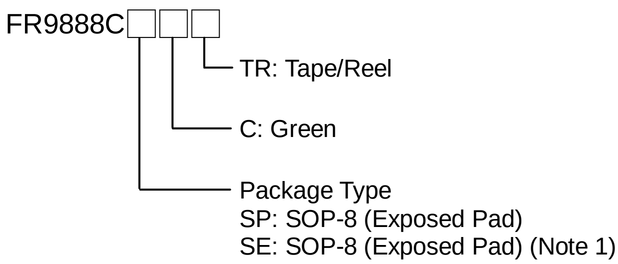
SE Package (SOP-8 Exposed Pad)



Note 1: Exposed pad is small pad.

Figure 1. Pin Assignment of FR9888C

Ordering Information



Typical Application Circuit

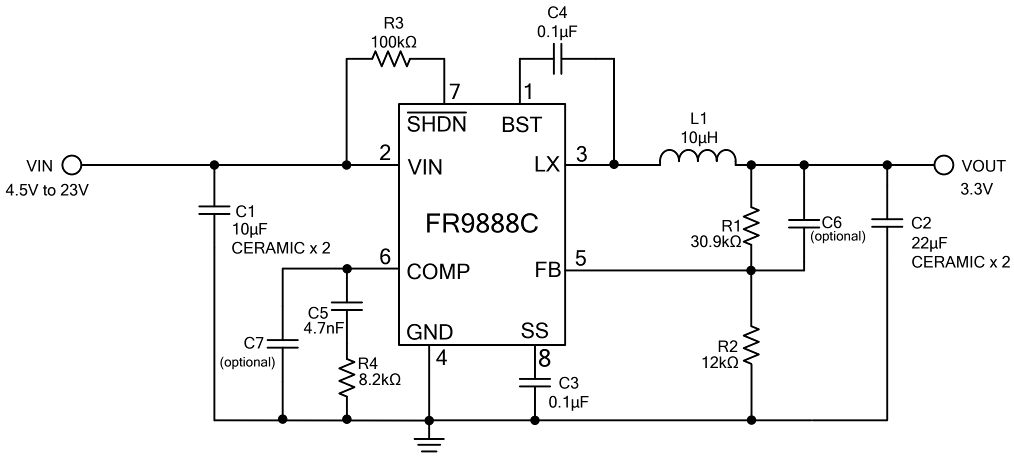


Figure 2. C_{IN} /C_{OUT} use Ceramic Capacitors Application Circuit

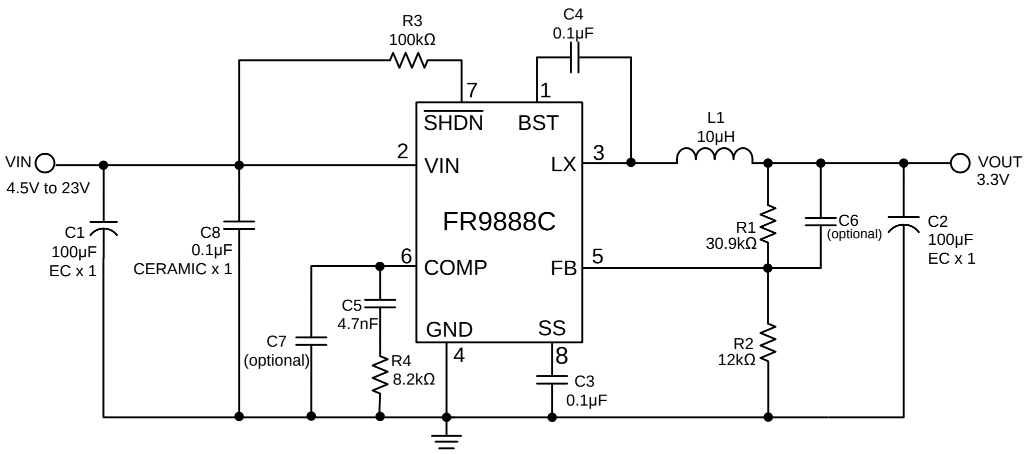


Figure 3. C_{IN} /C_{OUT} use Electrolytic Capacitors Application Circuit

V_{IN}=12V, the recommended BOM list is as below.

V_{OUT}	R1	R2	R4	C5	L1
1.2V	4.99kΩ	16.5kΩ	3.3kΩ	4.7nF	4.7μH
1.8V	4.99kΩ	5.23kΩ	5.6kΩ	4.7nF	6.8μH
3.3V	30.9kΩ	12kΩ	8.2kΩ	4.7nF	10μH
5V	30.9kΩ	6.98kΩ	10kΩ	4.7nF	10μH

Table 1. Recommended Component Values

Functional Pin Description

Pin Name	Pin No.	Pin Function
BST	**1**	High Side Gate Drive Boost Pin. A capacitance between 10nF~100nF must be connected from this pin to LX. It can boost the gate drive to fully turn on the internal high side NMOS.
VIN	**2**	Power Supply Input Pin. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
LX	**3**	Power Switching Node. Connect an external inductor to this switching node.
GND	**4**	Ground Pin. Connect this pin to exposed pad.
FB	**5**	Voltage Feedback Input Pin. Connect FB and V_{OUT} with a resistive voltage divider. This IC senses feedback voltage via FB and regulates it at 0.925V.
COMP	**6**	Compensation Pin. This pin is used to compensate the regulation control loop. Connect a series RC network from COMP pin to GND.
$\overline{\text{SHDN}}$	**7**	Enable input pin. Pull high to turn on IC, and pull low to turn off IC. Connect VIN with a 100kΩ resistor for self-startup.
SS	**8**	Soft-Start Pin. This pin controls the soft-start period. Connect a capacitor from SS to GND to set the soft start period.
Exposed Pad	**9**	Ground pin. The exposed pad must be soldered to a large PCB area and connected to GND for maximum power dissipation

Block Diagram

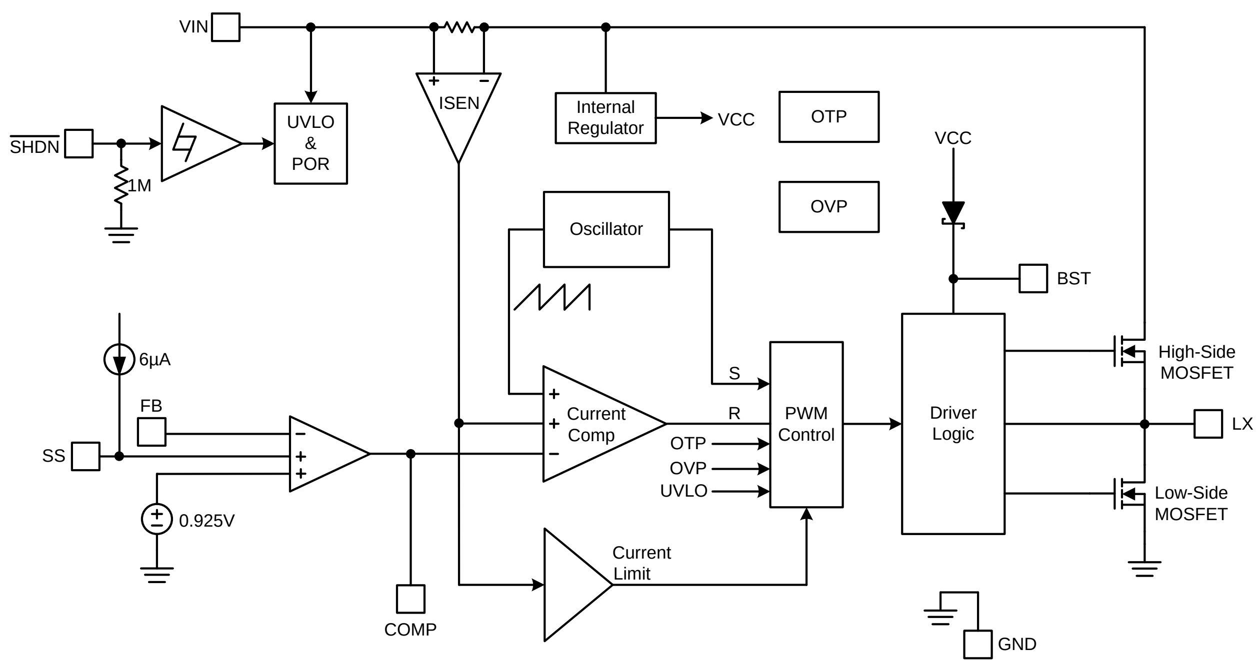


Figure 4. Block Diagram of FR9888C

Absolute Maximum Ratings (Note 2)

- Supply Voltage V_{IN} ---------- -0.3V to +25V
- Enable Voltage $V_{\overline{SHDN}}$ ---------- -0.3V to +25V
- LX Voltage V_{LX} ---------- -1V to V_{IN}+0.3V
- BST Voltage V_{BST} ---------- V_{LX}-0.3V to V_{LX}+6V
- All Other Pins Voltage ---------- -0.3V to +6V
- Maximum Junction Temperature (T_J) ---------- +150°C
- Storage Temperature (T_S) ---------- -65°C to +150°C
- Lead Temperature (Soldering, 10sec.) ---------- +260°C
- Power Dissipation @T_A=25°C, (P_D) (Note 3)
  SOP-8 (Exposed Pad) ---------- 2.08W
- Package Thermal Resistance, (θ_{JA})
  SOP-8 (Exposed Pad) ---------- 60°C/W
- Package Thermal Resistance, (θ_{JC})
  SOP-8 (Exposed Pad) ---------- 15°C/W

Note 2: Stresses beyond this listed under “Absolute Maximum Ratings" may cause permanent damage to the device.
Note 3: PCB heat sink copper area=10mm^2.

Recommended Operating Conditions

- Supply Voltage V_{IN} ---------- +4.5V to +23V
- Operation Temperature Range ---------- -40°C to + 85°C

Electrical Characteristics

(V_{IN}=12V, T_A=25°C, unless otherwise specified.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
V_{IN} Input Supply Voltage	V_{IN}		4.5		23	V
V_{IN} Quiescent Current	I_{DDQ}	$V_{\overline{SHDN}}$=2V, V_{FB}=1.0V		2.5		mA
V_{IN} Shutdown Supply Current	I_{SD}	$V_{\overline{SHDN}}$=0V			1	μA
Feedback Voltage	V_{FB}	4.5V≦V_{IN}≦23V	0.9	0.925	0.95	V
Feedback OVP Threshold Voltage	V_{OVP}			1.5		V
High-Side MOSFET R_{DS}(ON) (Note 4)	$R_{DS(ON)}$			110		mΩ
Low-Side MOSFET R_{DS}(ON) (Note 4)	$R_{DS(ON)}$			80		mΩ
High-Side MOSFET Leakage Current	$I_{LX(leak)}$	$V_{\overline{SHDN}}$=0V, V_{LX}=0V			10	μA
High-Side MOSFET Current Limit (Note 4)	$I_{LIMIT(HS)}$	Minimum Duty	4	5		A
Low-Side MOSFET Current Limit (Note 4)	$I_{LIMIT(LS)}$	From Drain to Source		1.5		A
Current sense to COMP Transconductance (Note 4)				3.5		A/V
Error Amplifier Transconductance (Note 4)		Δ I_{COMP} = ±10μA		1600		μA/V
Error Amplifier Voltage Gain (Note 4)				400		V/V
Oscillation frequency	F_{OSC}		290	340	420	kHz
Short Circuit Oscillation Frequency	$F_{OSC(short)}$	V_{FB}=0V		110		kHz
Maximum Duty Cycle	D_{MAX}	V_{FB}=0.8V		90		%
Minimum On Time (Note 4)	T_{MIN}			100		ns
Input UVLO Threshold	$V_{UVLO(Vth)}$	V_{IN} Rising		4.3		V
Under Voltage Lockout Threshold Hysteresis	$V_{UVLO(HYS)}$			400		mV
Soft-Start Current	I_{SS}	V_{SS}=0V		6		μA
Soft-Start Period	T_{SS}	C_{SS}=0.1μF		15		ms
$\overline{SHDN}$ Input Low Voltage	$V_{\overline{SHDN}(L)}$				0.4	V
$\overline{SHDN}$ Input High Voltage	$V_{\overline{SHDN}(H)}$		2			V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$	$V_{\overline{SHDN}}$=2V		2		μA
Thermal Shutdown Threshold (Note 4)	T_{SD}			170		°C

Note 4: Not production tested.

Typical Performance Curves

V_{IN}=12V, V_{OUT}=3.3V, C1=10μF× 2, C2=22μF×2, L1=10μH, TA=+25°C, unless otherwise noted.

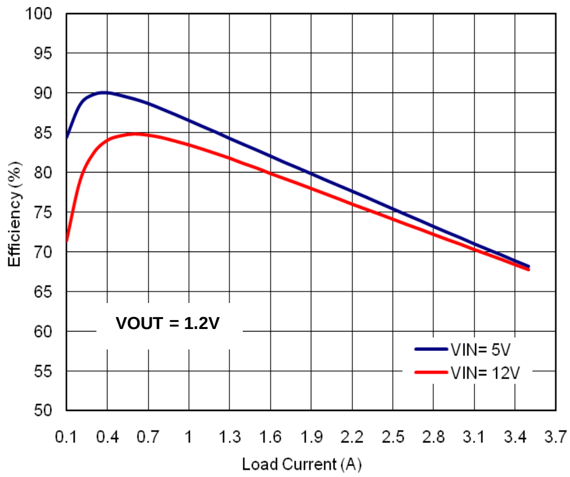


Figure 5. Efficiency vs. Load Current

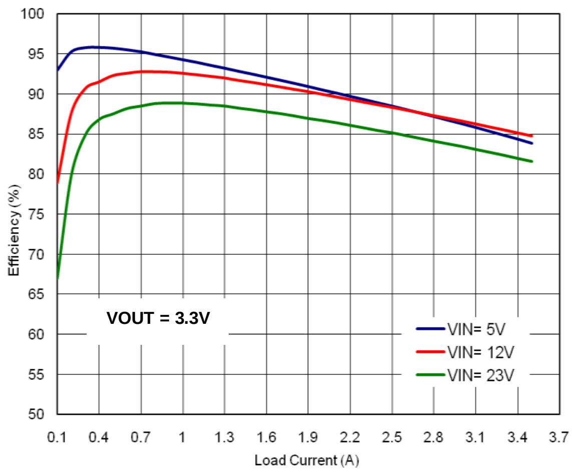


Figure 6. Efficiency vs. Load Current

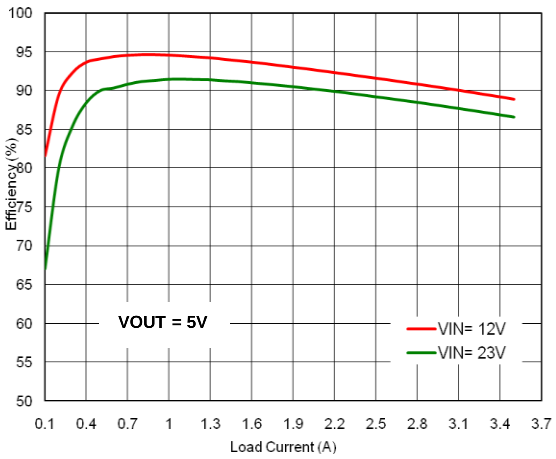


Figure 7. Efficiency vs. Load Current

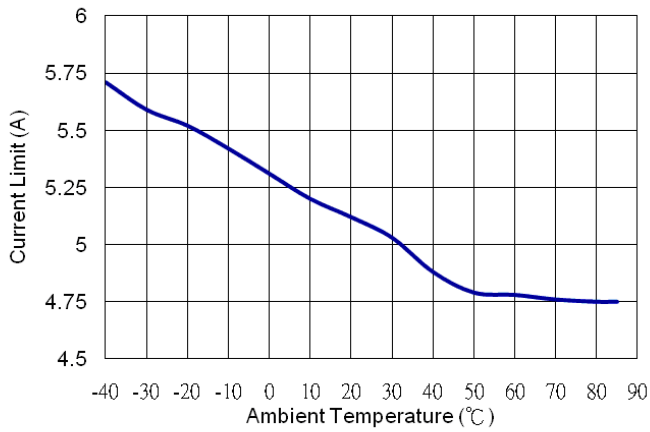


Figure 8. Current Limit vs. Temperature

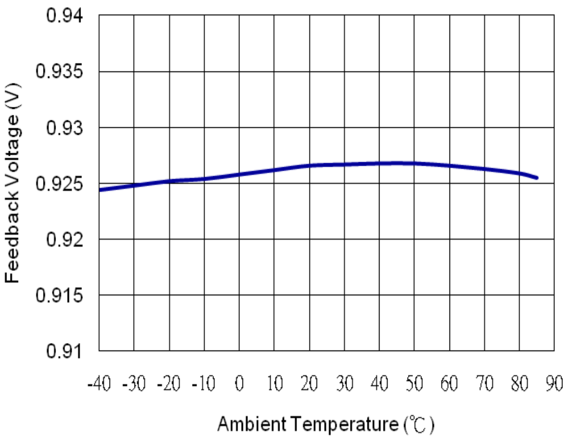


Figure 9. Feedback Voltage vs. Temperature

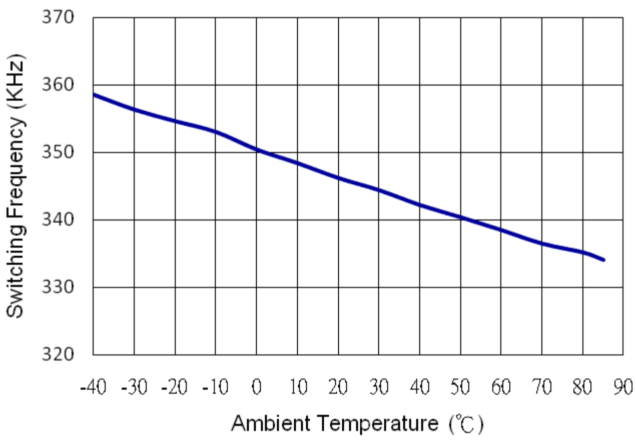
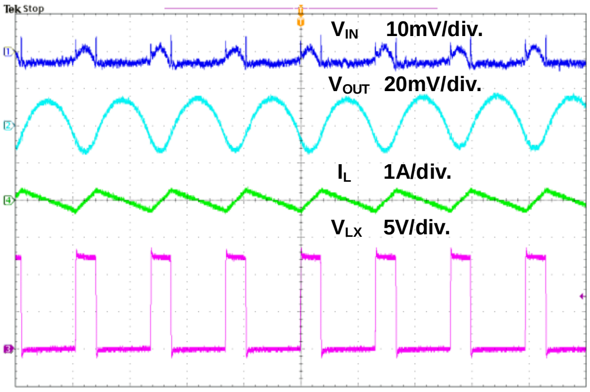


Figure 10. Switching Frequency vs. Temperature

Typical Performance Curves (Continued)

V_{IN}=12V, V_{OUT}=3.3V, C1=10μFx2, C2=22μFx2, L1=10μH, TA=+25°C, unless otherwise noted.

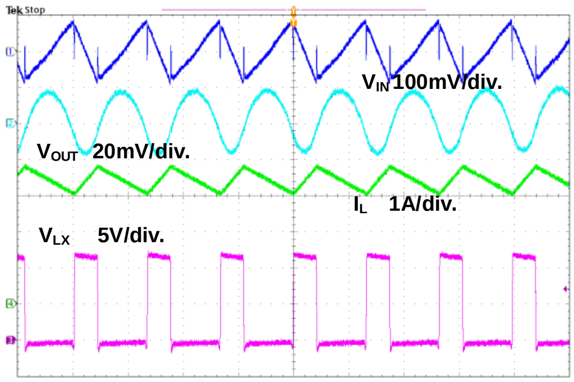
I_{OUT}=0A



2μs/div.

Figure 11. Steady State Waveform

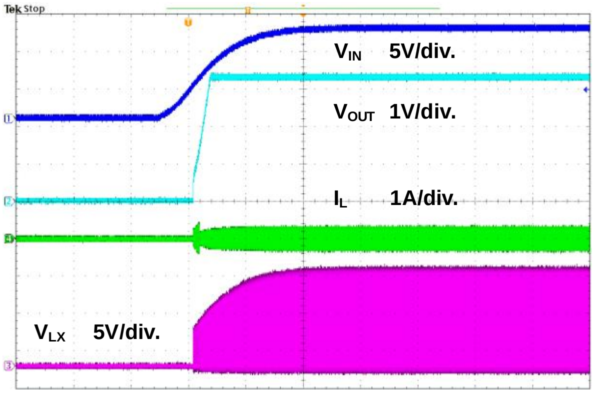
I_{OUT}=3.5A



2μs/div.

Figure 12. Steady State Waveform

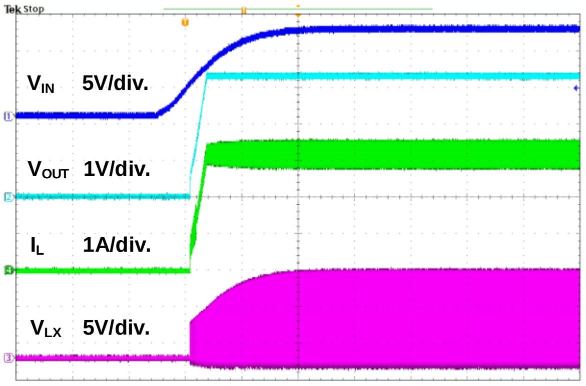
I_{OUT}=0A



40ms/div.

Figure 13. Power On through VIN Waveform

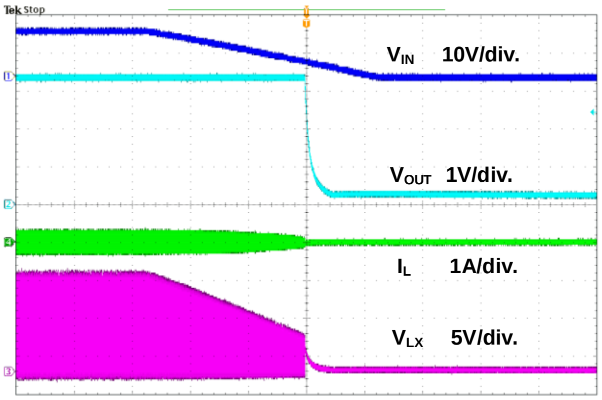
I_{OUT}=3.5A



40ms/div.

Figure 14. Power On through VIN Waveform

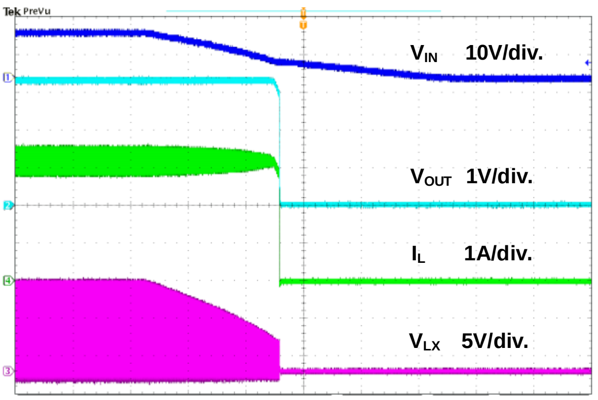
I_{OUT}=0A



20ms/div.

Figure 15. Power Off through VIN Waveform

I_{OUT}=3.5A



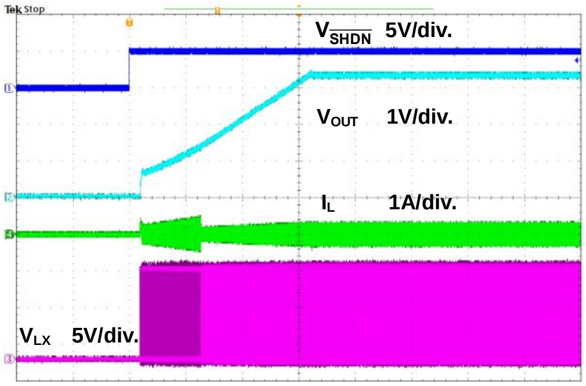
10ms/div.

Figure 16. Power Off through VIN Waveform

Typical Performance Curves (Continued)

V_{IN}=12V, V_{OUT}=3.3V, C1=10µF×2, C2=22µF×2, L1=10µH, TA=+25°C, unless otherwise noted.

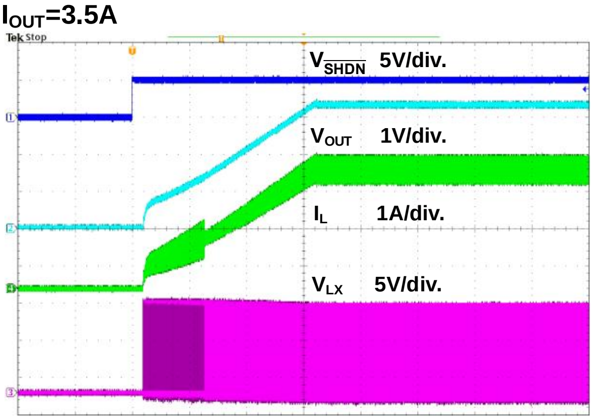
I_{OUT}=0A



4ms/div.

Figure 17. Power On through $\overline{SHDN}$ Waveform

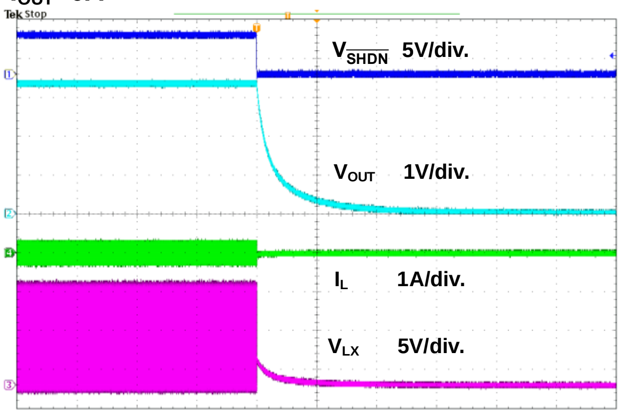
I_{OUT}=3.5A



4ms/div.

Figure 18. Power On through $\overline{SHDN}$ Waveform

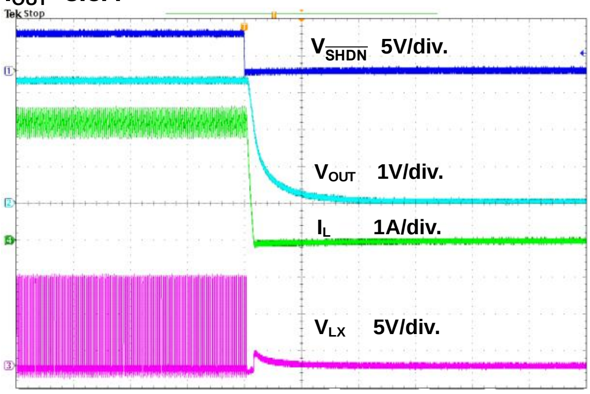
I_{OUT}=0A



4ms/div.

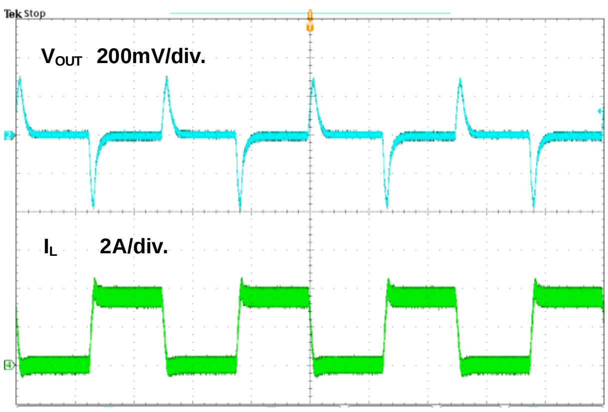
Figure 19. Power Off through $\overline{SHDN}$ Waveform

I_{OUT}=3.5A



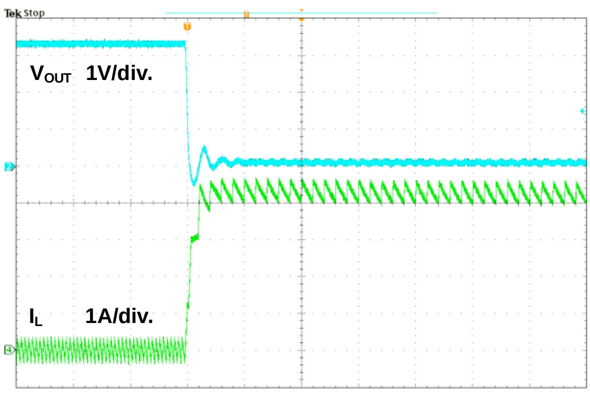
80µs/div.

Figure 20. Power Off through $\overline{SHDN}$ Waveform



400µs/div.

Figure 21. Load Transient Waveform



400µs/div.

Figure 22. Short Circuit Test

Function Description

The FR9888C is a high efficiency and constant frequency current mode step-down synchronous DC/DC converter. It has integrated high-side (110mΩ, typ) and low-side (80mΩ, typ) power switches, and provides 3.5A continuous load current. It regulates input voltage from 4.5V to 23V, and down to an output voltage as low as 0.925V.

Control Loop

During normal operation, the output voltage is sensed at FB pin by a resistive voltage divider and amplified through the error amplifier. The voltage of error amplifier output pin -- COMP is compared to the switch current to control the RS latch. At each cycle, the high side NMOS will be turned on when the oscillator sets the RS latch and turned off when current comparator resets the RS latch. When the load current increases, the FB pin voltage will drop below 0.925V, and it will cause the COMP voltage increasing until average inductor current arrives at new load current.

Enable

The FR9888C $\overline{\text{SHDN}}$ pin provides digital control to turn on/turn off the regulator. When the voltage of $\overline{\text{SHDN}}$ exceeds the threshold voltage, the regulator will start the soft start function. If the $\overline{\text{SHDN}}$ pin voltage is below the shutdown threshold voltage, the regulator will turn into shutdown mode and shutdown current will be smaller than 1μA. For auto start-up operation, connect $\overline{\text{SHDN}}$ to VIN through a 100KΩ resistor.

Soft Start

The FR9888C employs adjustable soft start function to reduce input inrush current during start up. When the device turns on, a 6μA current will begin to charge the capacitor which is connected from SS pin to GND. The equation for the soft start time is shown as below:

$$T_{SS}(ms)=\frac{C_{SS}(nF)\times V_{FB}}{I_{SS}(\mu A)}$$

The V_{FB} voltage is 0.925V and the I_{SS} current is 6μA. If a 0.1μF capacitor is connected from SS pin to GND, the soft start time will be 15ms.

Output Over Voltage Protection

When the FB pin voltage exceeds 1.5V, the output over voltage protection function will be triggered and turn off the high-side/low-side MOSFET.

Input Under Voltage Lockout

When the FR9888C is power on, the internal circuits will be inactive until V_{IN} voltage exceeds the input UVLO threshold voltage. And the regulator will be disabled when V_{IN} is below the input UVLO threshold voltage. The hysteretic of the UVLO comparator is 250mV (typ).

Short Circuit Protection

The FR9888C provides short circuit protection function to prevent the device damage from short condition. When the short condition occurs and the feedback voltage drops lower than 0.4V, the oscillator frequency will be reduced to 110kHz to prevent the inductor current increasing beyond the current limit. In the meantime, the current limit will also be reduced to lower the short current. Once the short condition is removed, the frequency and current limit will return to normal.

Over Current Protection

The FR9888C over current protection function is implemented by using cycle-by-cycle current limit architecture. The inductor current is monitored by measuring the high-side MOSFET series sense resistor voltage. When the load current increases, the inductor current will also increase. When the peak inductor current reaches the current limit threshold, the output voltage will start to drop. When the over current condition is removed, the output voltage will return to the regulated value.

Over Temperature Protection

The FR9888C incorporates an over temperature protection circuit to protect itself from overheating. When the junction temperature exceeds the thermal shutdown threshold temperature, the regulator will be shutdown. And the hysteretic of the over temperature protection is 60°C (typ).

Compensation

The stability of the feedback circuit is controlled by COMP pin. The compensation value of the application circuit is optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability.

Application Information

Output Voltage Setting

The output voltage V_{OUT} is set by using a resistive divider from the output to FB. The FB pin regulated voltage is 0.925V. Thus the output voltage is:

$$V_{OUT}=0.925V\times\left(1+\frac{R1}{R2}\right)$$

Table 2 lists recommended values of R1 and R2 for most used output voltage.

Table 2 Recommended Resistance Values

V_{OUT}	R1	R2
5V	30.9kΩ	6.98kΩ
3.3V	30.9kΩ	12kΩ
1.8V	4.99kΩ	5.23kΩ
1.2V	4.99kΩ	16.5kΩ

Place resistors R1 and R2 close to FB pin to prevent stray pickup.

Input Capacitor Selection

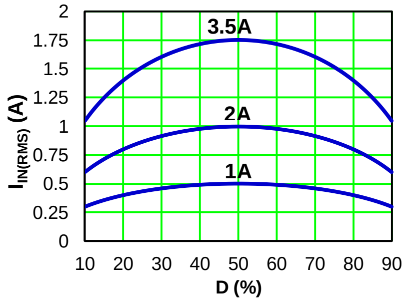
The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step-down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)}$$

$$D=\frac{V_{OUT}}{V_{IN}}$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$. The following diagram is the graphical representation of above equation.



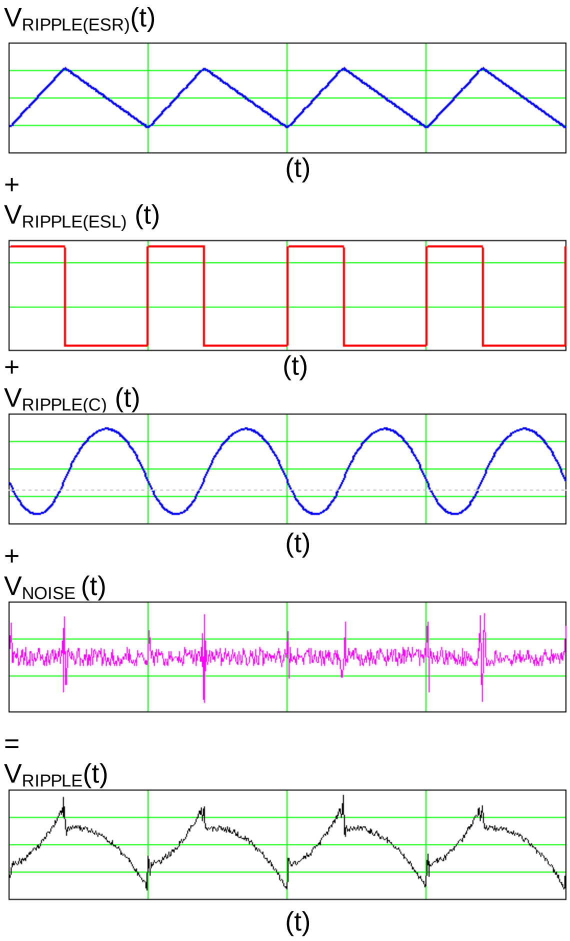
A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice. When using tantalum or electrolytic capacitors, a 0.1μF ceramic capacitor should be placed as close to the IC as possible.

Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t)=V_{RIPPLE(C)}(t)+V_{RIPPLE(ESR)}(t)+V_{RIPPLE(ESL)}(t)+V_{NOISE}(t)$$

The following figures show the form of the ripple contributions.



Application Information (Continued)

$$V_{RIPPLE(ESR,\ p\text{-}p)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR$$

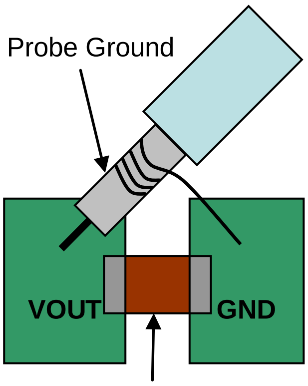
$$V_{RIPPLE(ESL,\ p\text{-}p)}=\frac{ESL}{L+ESL}\times V_{IN}$$

$$V_{RIPPLE(C,\ p\text{-}p)}=\frac{V_{OUT}}{8\times F_{OSC}{}^{2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor.

Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirements. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Removing the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminates noise.



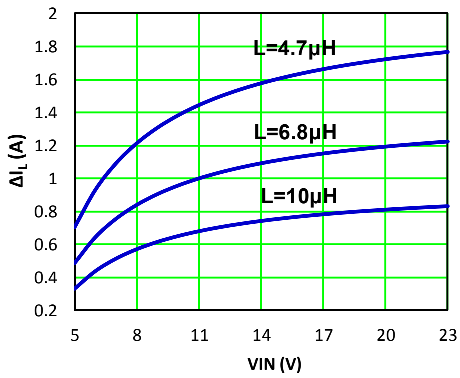
Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode.

That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to-peak ripple current:

$$\Delta I_L=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

The following diagram is an example to graphical represent ΔI_L equation.



V_{OUT}=3.3V, F_{OSC}=340kHz

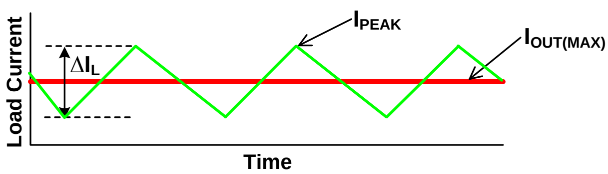
A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L=0.3\times I_{OUT(MAX)}$$

$$L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{V_{IN}\times F_{OSC}\times\Delta I_L}$$

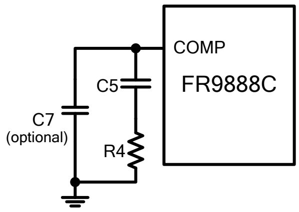
To guarantee sufficient output current, peak inductor current must be lower than the FR9888C high-side MOSFET current limit. The peak inductor current is as below:

$$I_{PEAK}=I_{OUT(MAX)}+\frac{\Delta I_L}{2}$$



Application Information (Continued)

Compensation Components Selection



Select the appropriate compensation value by following procedure:

- Calculate the R4 value with the following equation:

$$R4 < \frac{2\pi \times C_{OUT} \times 0.1 \times F_{OSC} \times V_{OUT}}{G_{EA} \times G_{CS} \times V_{REF}}$$

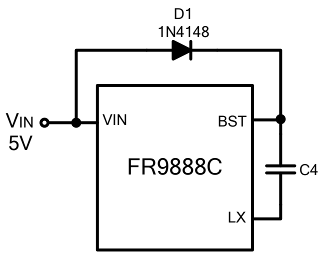
where G_{EA} is the error amplifier voltage gain, and G_{CS} is the current sense gain.

- Calculate the C5 value with the following equation:

$$C5 > \frac{4}{2\pi \times R4 \times 0.1 \times F_{OSC}}$$

External Diode Selection

For 5V input applications, it is recommended to add an external boost diode. This helps improving the efficiency. The boost diode can be a low cost one, such as 1N4148.



PCB Layout Recommendation

The device's performance and stability are dramatically affected by PCB layout. It is recommended to follow these general guidelines shown as below:

1. Place the input capacitors and output capacitors as close to the device as possible. The traces which connect to these capacitors should be as short and wide as possible to minimize parasitic inductance and resistance.
2. Place feedback resistors close to the FB pin.
3. Keep the sensitive signal (FB) away from the switching signal (LX).
4. The exposed pad of the package should be soldered to an equivalent area of metal on the PCB. This area should connect to the GND plane and have multiple via connections to the back of the PCB as well as connections to intermediate PCB layers. The GND plane area connecting to the exposed pad should be maximized to improve thermal performance.
5. Multi-layer PCB design is recommended.

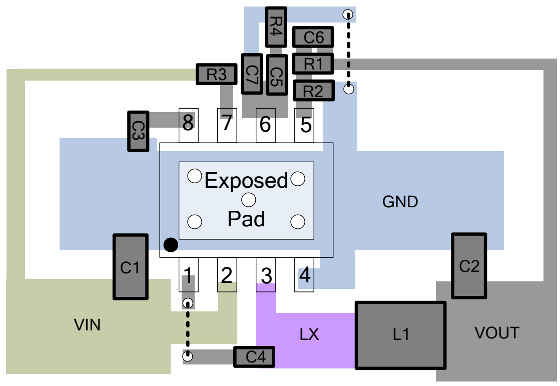
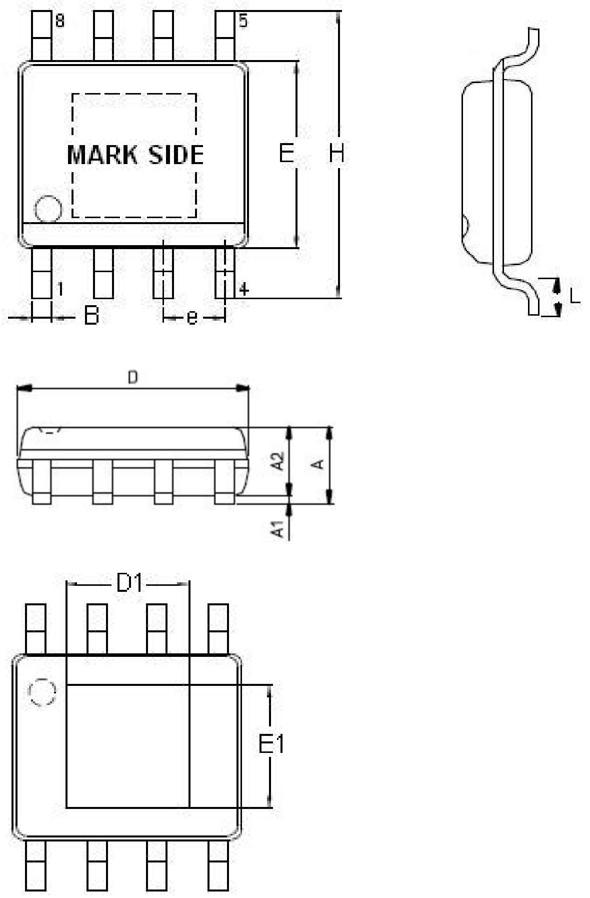


Figure 23. Recommended Layout Diagram

Outline Information

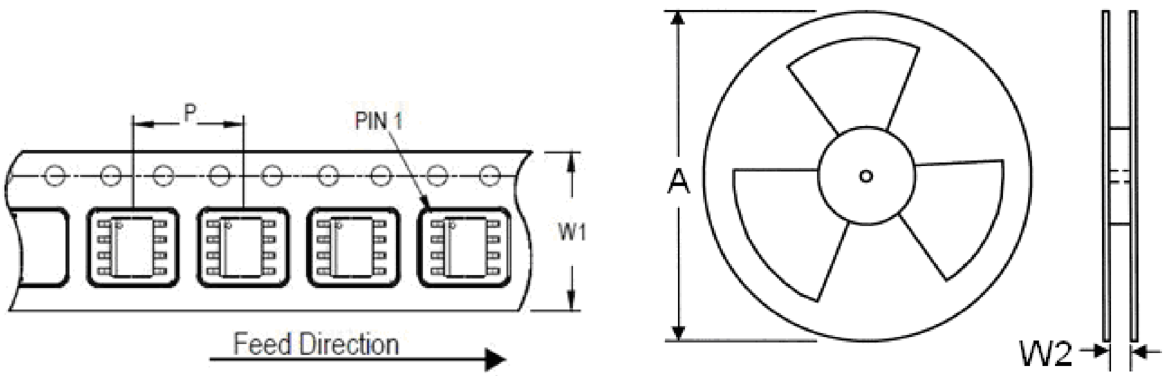
SOP-8 (Exposed Pad) Package (Unit: mm)



SYMBOLS UNIT	DIMENSION IN MILLIMETER			
	SP		SE	
	MIN	MAX	MIN	MAX
A	1.25	1.70	1.25	1.70
A1	0.00	0.15	0.00	0.15
A2	1.25	1.55	1.25	1.55
B	0.31	0.51	0.31	0.51
D	4.80	5.00	4.80	5.00
D1	3.04	3.50	1.80	2.40
E	3.80	4.00	3.80	4.00
E1	2.15	2.41	1.80	2.40
e	1.20	1.34	1.20	1.34
H	5.80	6.20	5.80	6.20
L	0.40	1.27	0.40	1.27

Note：Followed From JEDEC MO-012-E.

Carrier Dimensions



Tape Size (W1) mm	Pocket Pitch (P) mm	Reel Size (A)		Reel Width (W2) mm	Empty Cavity Length mm	Units per Reel
		in	mm			
12	8	13	330	12.4	400~1000	2,500