

Low-Noise, Very Low Drift, Precision VOLTAGE REFERENCE

FEATURES

- **LOW TEMPERATURE DRIFT:**
 - High-Grade: 3ppm/°C (max)
 - Standard-Grade: 8ppm/°C (max)
- **HIGH ACCURACY:**
 - High-Grade: 0.05% (max)
 - Standard-Grade: 0.1% (max)
- **LOW NOISE:** 3μV_{pp}/V
- **HIGH OUTPUT CURRENT:** ±10mA
- **TEMPERATURE RANGE:** –40°C to +125°C

APPLICATIONS

- 16-BIT DATA ACQUISITION SYSTEMS
- ATE EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- MEDICAL INSTRUMENTATION
- OPTICAL CONTROL SYSTEMS
- PRECISION INSTRUMENTATION

DESCRIPTION

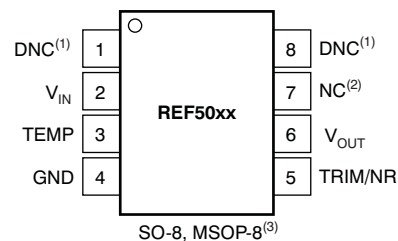
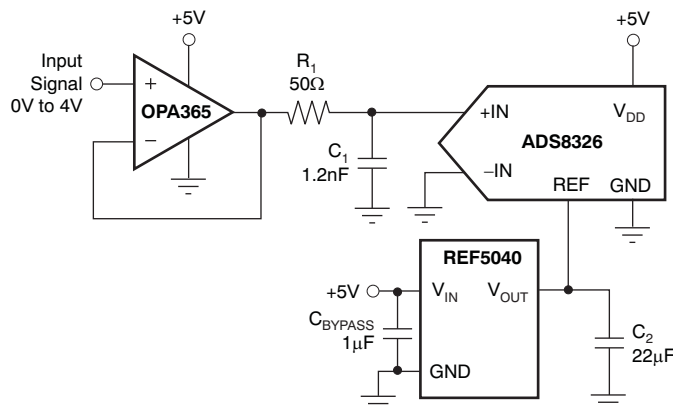
The REF50xx is a family of low-noise, low-drift, very high precision voltage references. These references are capable of both sinking and sourcing, and are very robust with regard to line and load changes.

Excellent temperature drift (3ppm/°C) and high accuracy (0.05%) are achieved using proprietary design techniques. These features, combined with very-low noise make the REF50xx family ideal for use in high-precision data acquisition systems.

Each reference voltage is available in both standard- and high-grade versions. They are offered in MSOP-8⁽³⁾ and SO-8 packages, and are specified from –40°C to +125°C.

REF50xx Family

MODEL	OUTPUT VOLTAGE
REF5020	2.048V
REF5025	2.5V
REF5030	3.0V
REF5040	4.096V
REF5045	4.5V
REF5050	5.0V
REF5010	10.0V



- NOTES: (1) DNC = Do not connect.
(2) NC = No internal connection.
(3) Contact a TI sales representative for information regarding MSOP-8 (DGK) package availability.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	OUTPUT VOLTAGE	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
STANDARD GRADE (8ppm, 0.1%)				
REF5020A	2.048V	SO-8	D	REF5020
		MSOP-8 ⁽²⁾	DGK	R50A
REF5025A	2.5V	SO-8	D	REF5025
		MSOP-8 ⁽²⁾	DGK	R50B
REF5030A	3.0V	SO-8	D	REF5030
		MSOP-8 ⁽²⁾	DGK	R50C
REF5040A	4.096V	SO-8	D	REF5040
		MSOP-8 ⁽²⁾	DGK	R50D
REF5045A	4.5V	SO-8	D	REF5045
		MSOP-8 ⁽²⁾	DGK	R50E
REF5050A	5.0V	SO-8	D	REF5050
		MSOP-8 ⁽²⁾	DGK	R50F
REF5010A	10.0V	SO-8	D	REF5010
		MSOP-8 ⁽²⁾	DGK	R50G
HIGH GRADE (3ppm, 0.05%)				
REF5020I	2.048V	SO-8	D	REF5020
		MSOP-8 ⁽²⁾	DGK	R50A
REF5025I	2.5V	SO-8	D	REF5025
		MSOP-8 ⁽²⁾	DGK	R50B
REF5030I	3.0V	SO-8	D	REF5030
		MSOP-8 ⁽²⁾	DGK	R50C
REF5040I	4.096V	SO-8	D	REF5040
		MSOP-8 ⁽²⁾	DGK	R50D
REF5045I	4.5V	SO-8	D	REF5045
		MSOP-8 ⁽²⁾	DGK	R50E
REF5050I	5.0V	SO-8	D	REF5050
		MSOP-8 ⁽²⁾	DGK	R50F
REF5010I	10.0V	SO-8	D	REF5010
		MSOP-8 ⁽²⁾	DGK	R50G

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Contact a TI sales representative for information regarding MSOP-8 (DGK) package availability.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

PARAMETER		REF50xx	UNIT
Input Voltage		+18	V
Output Short-Circuit		30	mA
Operating Temperature Range		–55 to +125	°C
Storage Temperature Range		–55 to +150	°C
Junction Temperature (T _J max)		+150	°C
ESD Rating	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS: PER DEVICE

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

At $T_A = +25^{\circ}\text{C}$, $I_{\text{LOAD}} = 0$, $C_L = 1\mu\text{F}$, and $V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$ to 18V, unless otherwise noted.

PARAMETER	CONDITIONS	PER DEVICE			UNIT
		MIN	TYP	MAX	
REF5020 (V _{OUT} = 2.048V) ⁽¹⁾					
OUTPUT VOLTAGE	V _{OUT} 2.7V < V _{IN} < 18V		2.048		V
Output Voltage					
Initial Accuracy:					
High-Grade		−0.05		0.05	%
Standard-Grade		−0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		6		μV _{PP}
REF5025 (V _{OUT} = 2.5V)					
OUTPUT VOLTAGE	V _{OUT}		2.5		V
Output Voltage					
Initial Accuracy:					
High-Grade		−0.05		0.05	%
Standard-Grade		−0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		7.5		μV _{PP}
REF5030 (V _{OUT} = 3.0V)					
OUTPUT VOLTAGE	V _{OUT}		3.0		V
Output Voltage					
Initial Accuracy:					
High-Grade		−0.05		0.05	%
Standard-Grade		−0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		9		μV _{PP}
REF5040 (V _{OUT} = 4.096V)					
OUTPUT VOLTAGE	V _{OUT}		4.096		V
Output Voltage					
Initial Accuracy:					
High-Grade		−0.05		0.05	%
Standard-Grade		−0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		12		μV _{PP}
REF5045 (V _{OUT} = 4.5V)					
OUTPUT VOLTAGE	V _{OUT}		4.5		V
Output Voltage					
Initial Accuracy:					
High-Grade		−0.05		0.05	%
Standard-Grade		−0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		13.5		μV _{PP}
REF5050 (V _{OUT} = 5.0V)					
OUTPUT VOLTAGE	V _{OUT}		5.0		V
Output Voltage					
Initial Accuracy:					
High-Grade		−0.05		0.05	%
Standard-Grade		−0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		15		μV _{PP}
REF5010 (V _{OUT} = 10.0V)					
OUTPUT VOLTAGE	V _{OUT}		10.0		V
Output Voltage					
Initial Accuracy:					
High-Grade		−0.05		0.05	%
Standard-Grade		−0.1		0.1	%
NOISE					
Output Voltage Noise	f = 0.1Hz to 10Hz		30		μV _{PP}

(1) For $V_{\text{OUT}} \leq 2.5\text{V}$, the minimum supply voltage is 2.7V.

ELECTRICAL CHARACTERISTICS: ALL DEVICES

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

At $T_A = +25^{\circ}\text{C}$, $I_{\text{LOAD}} = 0$, $C_L = 1\mu\text{F}$, and $V_{\text{IN}} = (V_{\text{OUT}} + 0.2\text{V})$ to 18V, unless otherwise noted.

PARAMETER	CONDITIONS	REF50xx			UNIT
		MIN	TYP	MAX	
OUTPUT VOLTAGE TEMPERATURE DRIFT					
Output Voltage Temperature Drift	dV_{OUT}/dT				
High-Grade			2.5	3	ppm/°C
Standard-Grade			3	8	ppm/°C
LINE REGULATION					
Line Regulation	dV_{OUT}/dV_{IN}				
REF5020 ⁽¹⁾ Only	$V_{IN} = 2.7V$ to 18V		0.1	1	ppm/V
All Other Devices			0.1	1	ppm/V
Over Temperature			0.2	1	ppm/V
LOAD REGULATION					
Load Regulation	dV_{OUT}/dI_{LOAD}	$-10mA < I_{LOAD} < +10mA, V_{IN} = V_{OUT} + 0.75V$	20	30	ppm/mA
Over Temperature				50	ppm/mA
SHORT-CIRCUIT CURRENT					
Short-Circuit Current	I_{SC}	$V_{OUT} = 0$	25		mA
TEMP PIN					
Voltage Output		At $T_A = +25^{\circ}C$	575		mV
Temperature Sensitivity			2.64		mV/°C
TURN-ON SETTLING TIME					
Turn-On Settling Time		To 0.1% with $C_L = 1\mu F$	200		μs
POWER SUPPLY					
Supply Voltage	V_S	See Note ⁽¹⁾	$V_{OUT} + 0.2^{(1)}$	18	V
Quiescent Current			0.8	1	mA
Over Temperature				1.2	mA
TEMPERATURE RANGE					
Specified Range			-40	+125	°C
Operating Range			-55	+125	°C
Thermal Resistance	θ_{JA}				
MSOP-8			150		°C/W
SO-8			150		°C/W

(1) For $V_{\text{OUT}} \leq 2.5\text{V}$, the minimal supply voltage is 2.7V.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, and $V_S = V_{\text{OUT}} + 0.2\text{V}$, unless otherwise noted. For $V_{\text{OUT}} \leq 2.5\text{V}$, the minimum supply voltage is 2.7V.

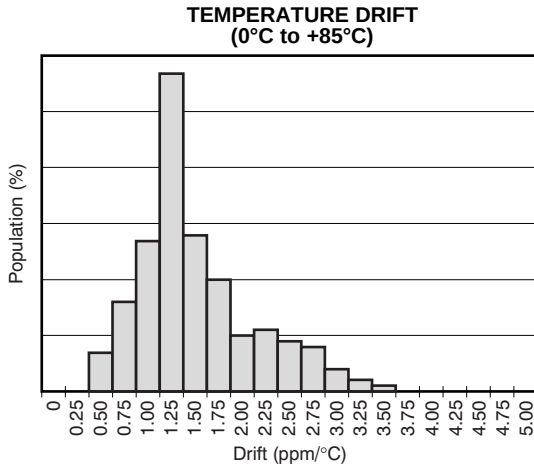


Figure 1.

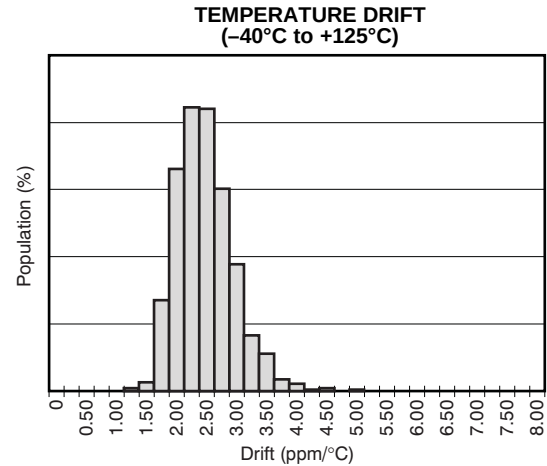


Figure 2.

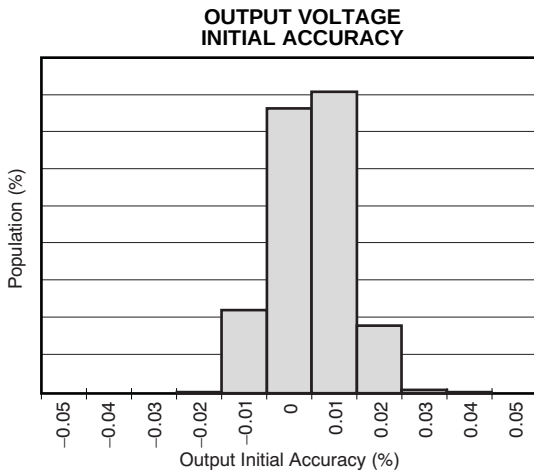


Figure 3.

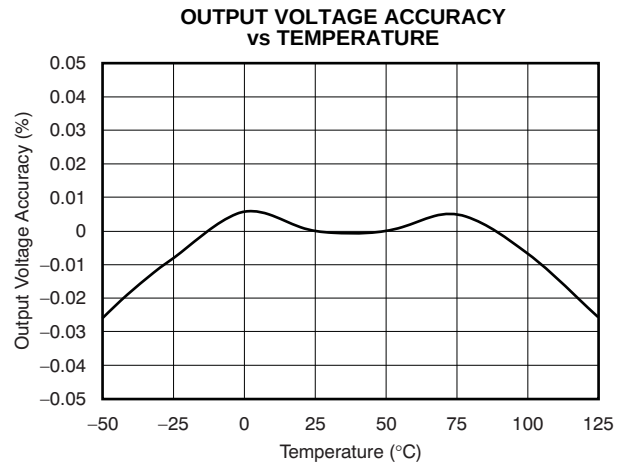


Figure 4.

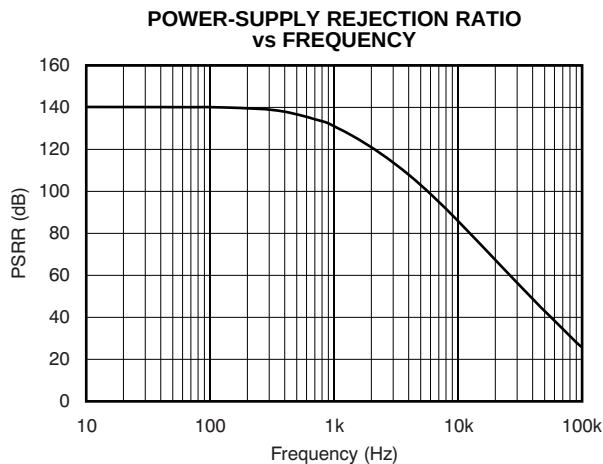


Figure 5.

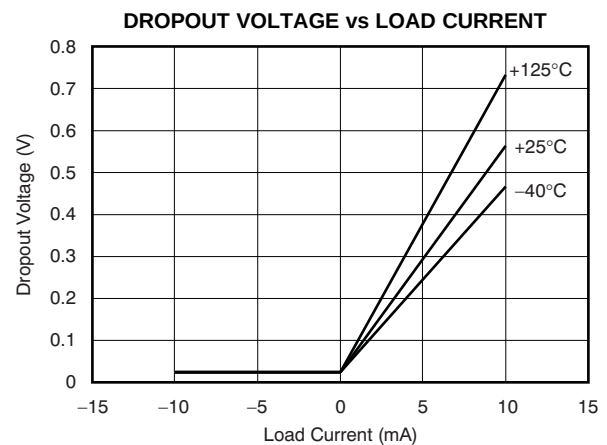


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, and $V_S = V_{\text{OUT}} + 0.2\text{V}$, unless otherwise noted. For $V_{\text{OUT}} \leq 2.5\text{V}$, the minimum supply voltage is 2.7V.

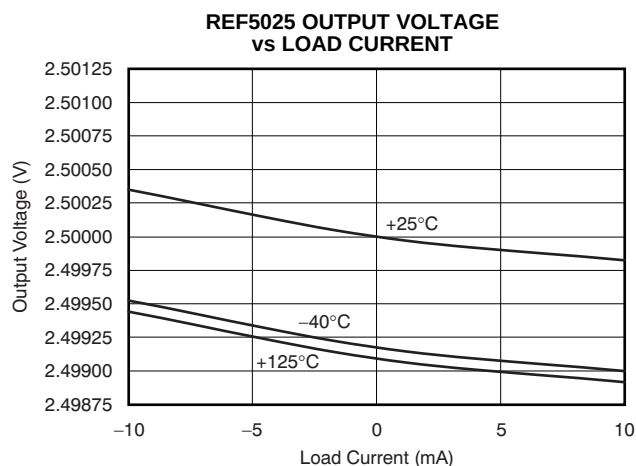


Figure 7.

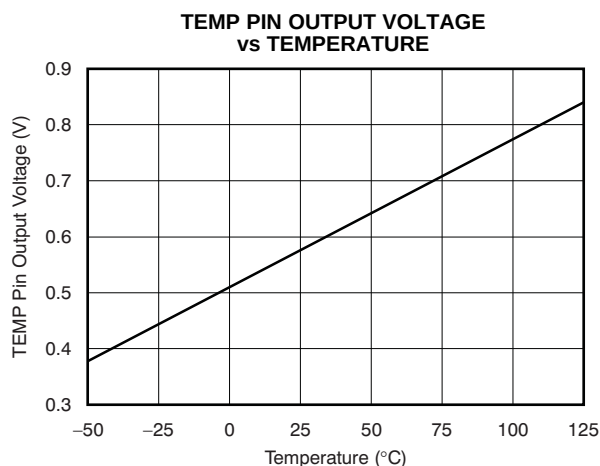


Figure 8.

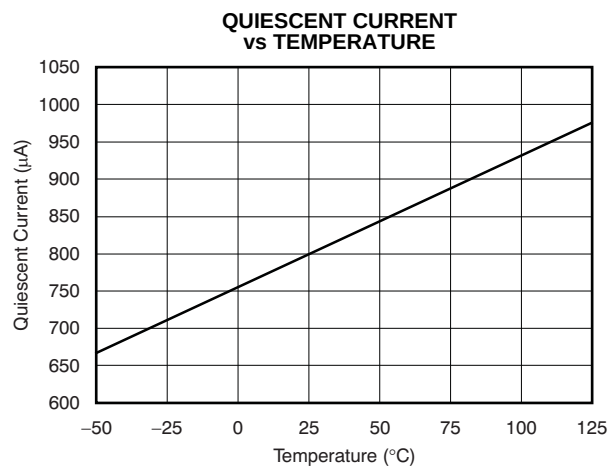


Figure 9.

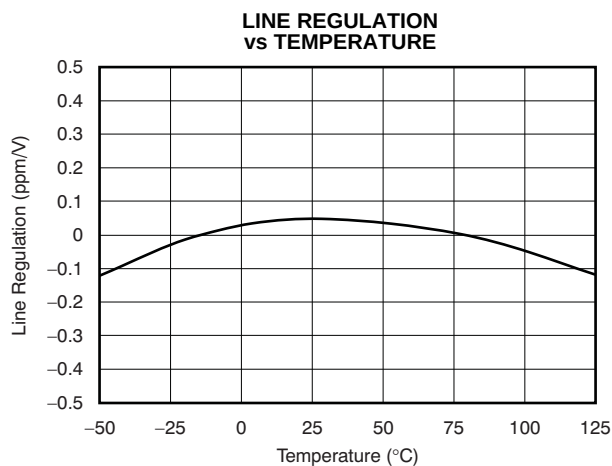


Figure 10.

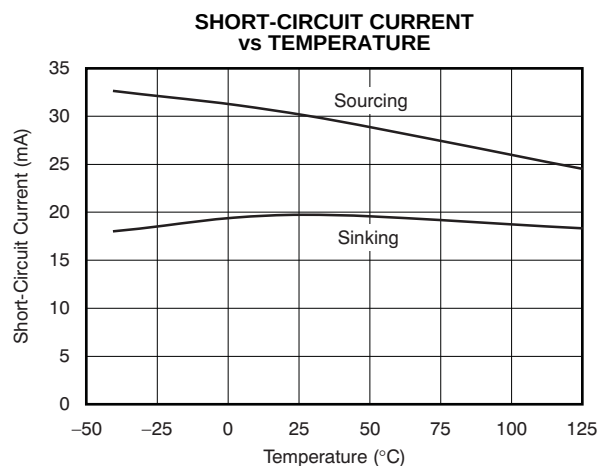


Figure 11.

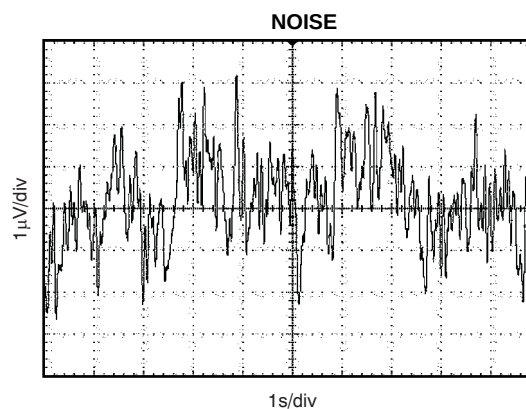


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, and $V_S = V_{\text{OUT}} + 0.2\text{V}$, unless otherwise noted. For $V_{\text{OUT}} \leq 2.5\text{V}$, the minimum supply voltage is 2.7V.

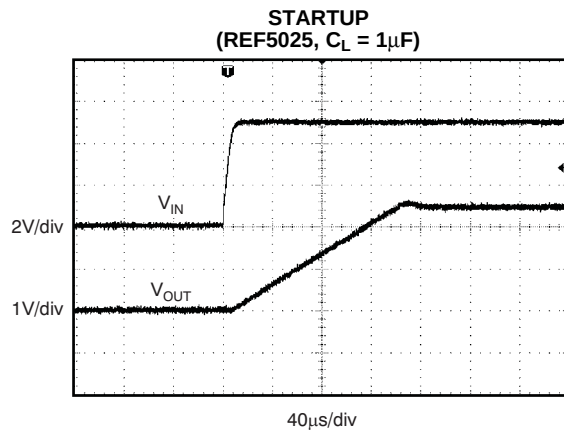


Figure 13.

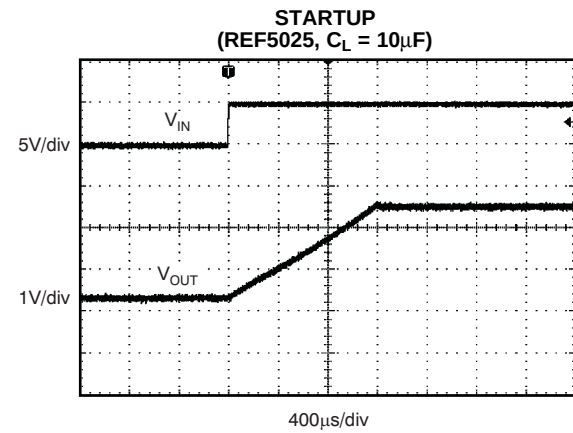


Figure 14.

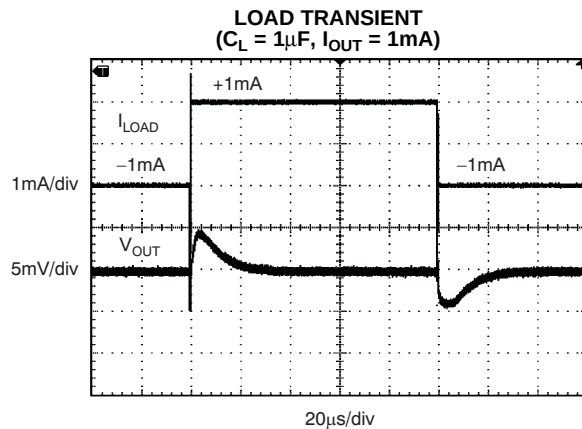


Figure 15.

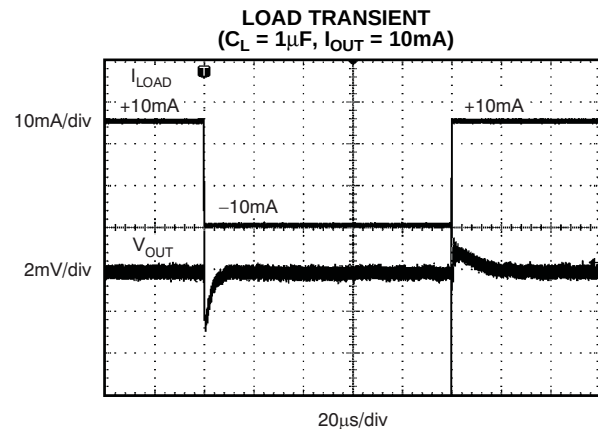


Figure 16.

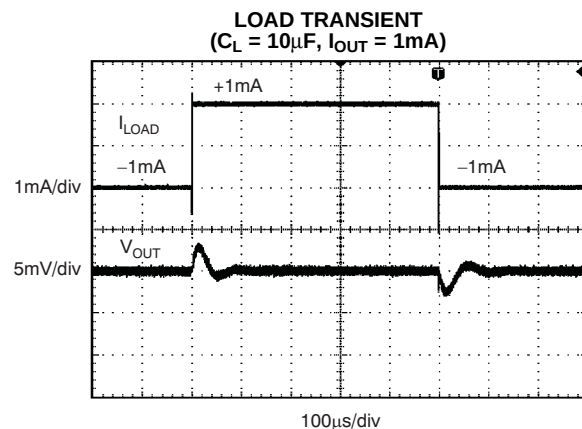


Figure 17.

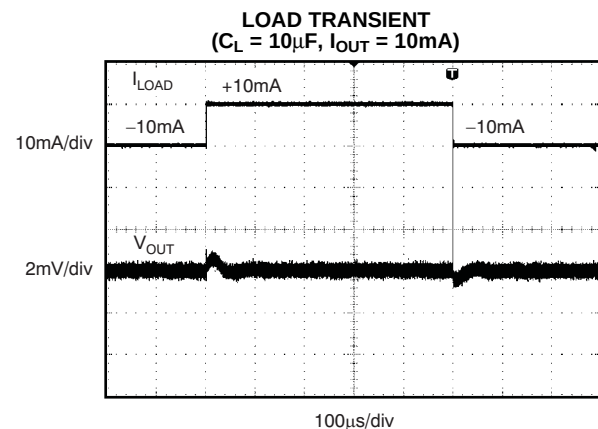


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $I_{\text{LOAD}} = 0$, and $V_S = V_{\text{OUT}} + 0.2\text{V}$, unless otherwise noted. For $V_{\text{OUT}} \leq 2.5\text{V}$, the minimum supply voltage is 2.7V.

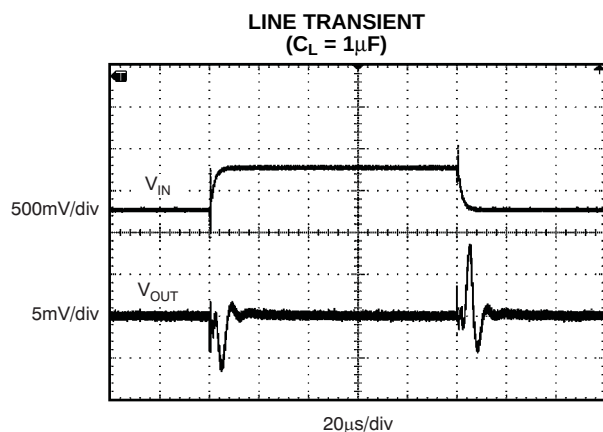


Figure 19.

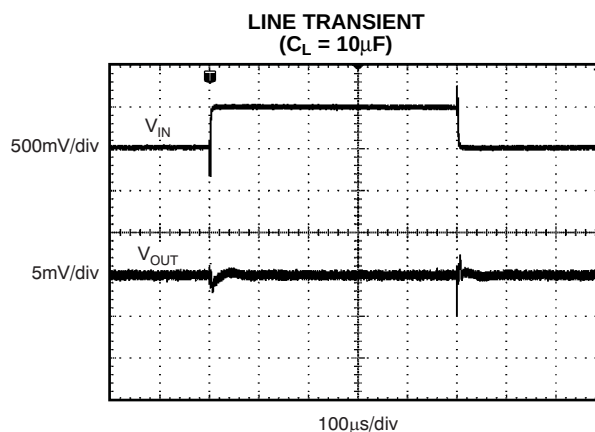


Figure 20.

APPLICATION INFORMATION

The REF50xx is family of low-noise, precision bandgap voltage references that are specifically designed for excellent initial voltage accuracy and drift. [Figure 21](#) shows a simplified block diagram of the REF50xx.

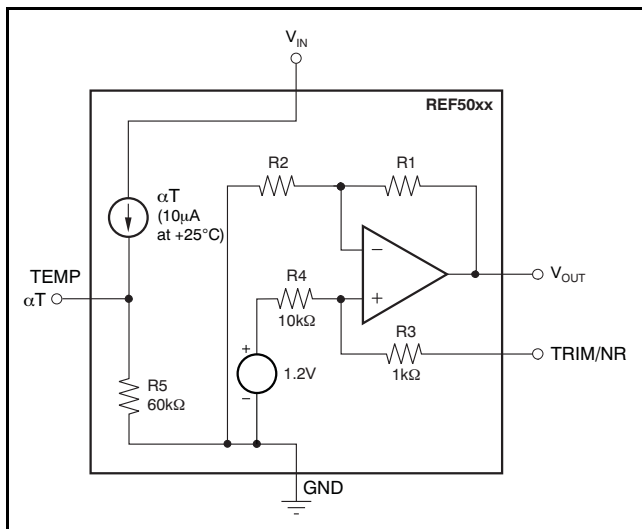


Figure 21. REF50xx Simplified Block Diagram

BASIC CONNECTIONS

[Figure 22](#) shows the typical connections for the REF50xx. A supply bypass capacitor ranging between 1μF to 10μF is recommended. A 1μF to 50μF output capacitor (C_L) must be connected from V_{OUT} to GND. The ESR value of C_L must be less than or equal to 1.5Ω to ensure output stability. To minimize noise, the recommended ESR of C_L is between 1Ω and 1.5Ω.

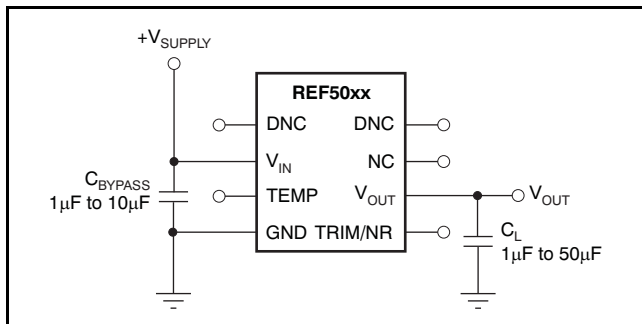


Figure 22. Basic Connections

SUPPLY VOLTAGE

The REF50xx family of voltage references features extremely low dropout voltage. With the exception of the REF5020, which has a minimum supply requirement of 2.7V, these references can be operated with a supply of 200mV above the output voltage in an unloaded condition. For loaded conditions, a typical dropout voltage versus load plot is shown in [Figure 6](#) of the Typical Characteristics.

OUTPUT ADJUSTMENT USING THE TRIM/NR PIN

The REF50xx provides a very accurate, factory-trimmed voltage output. However, V_{OUT} can be adjusted using the trim and noise reduction pin (TRIM/NR, pin 5). [Figure 23](#) shows a typical circuit that allows an output adjustment of ±15mV.

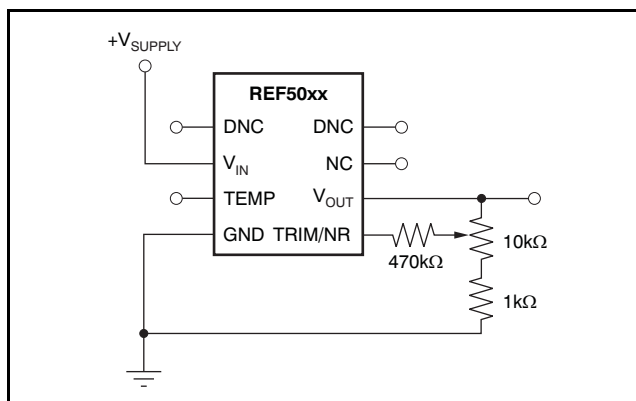


Figure 23. V_{OUT} Adjustment Using the TRIM/NR Pin

The REF50xx allows access to the bandgap through the TRIM/NR pin. Placing a capacitor from the TRIM/NR pin to GND (see [Figure 24](#)) in combination with the internal R_3 and R_4 resistors creates a low-pass filter. A capacitance of 1μF creates a low-pass filter with the corner frequency between 10Hz and 20Hz. Such a filter decreases the overall noise measured on the V_{OUT} pin by half. Higher capacitance results in a lower filter cutoff frequency, further reducing output noise. Note that use of this capacitor increases startup time.

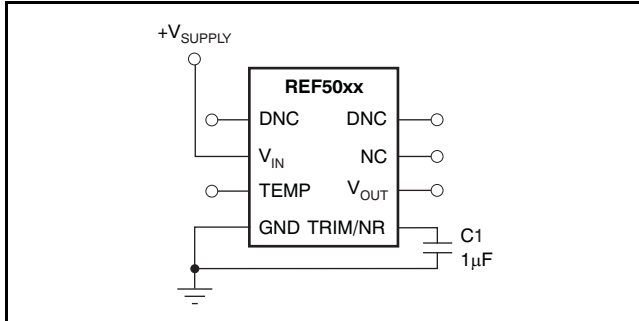


Figure 24. Noise Reduction Using the TRIM/NR Pin

TEMPERATURE DRIFT

The REF50xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by the following equation:

$$\text{Drift} = \left(\frac{V_{\text{OUTMAX}} - V_{\text{OUTMIN}}}{V_{\text{OUT}} \times \text{Temp Range}} \right) \times 10^6 (\text{ppm}) \quad (1)$$

The REF50xx features a maximum drift coefficient of 3ppm/°C for the high-grade version, and 8ppm/°C for the standard-grade.

TEMPERATURE MONITORING

The temperature output terminal (TEMP, pin 3) provides a temperature-dependent voltage output with approximately 60kΩ source impedance. As seen in [Figure 8](#), the output voltage follows the nominal relationship:

$$V_{\text{TEMP PIN}} = 509\text{mV} + 2.64 \times T(^{\circ}\text{C})$$

This pin indicates general chip temperature, accurate to approximately ±15°C. Although it is not generally suitable for accurate temperature measurements, it can be used to indicate temperature changes or for temperature compensation of analog circuitry. A temperature change of 30°C corresponds to an approximate 79mV change in voltage at the TEMP pin.

The TEMP pin has high output impedance (see [Figure 21](#)). Loading this pin with a low-impedance circuit induces a measurement error; however, it does not have any effect on V_{OUT} accuracy. To avoid errors caused by low-impedance loading, buffer the TEMP pin output with a suitable low-temperature drift op amp, such as the [OPA333](#), [OPA335](#), or [OPA376](#), as shown in [Figure 25](#).

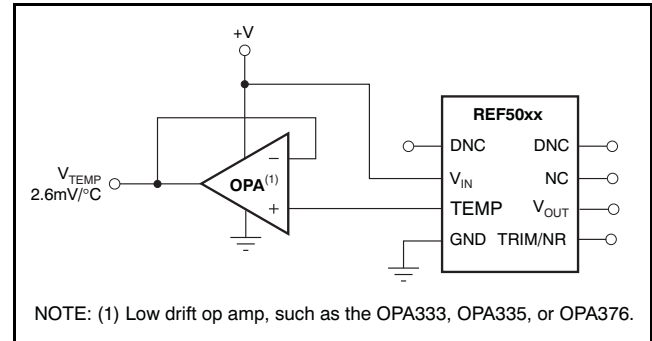


Figure 25. Buffering the TEMP Pin Output

POWER DISSIPATION

The REF50xx family is specified to deliver current loads of ±10mA over the specified input voltage range. The temperature of the device increases according to the equation:

$$T_J = T_A + P_D \times \theta_{JA}$$

Where:

T_J = Junction temperature (°C)

T_A = Ambient temperature (°C)

P_D = Power dissipated (W)

θ_{JA} = Junction-to-ambient thermal resistance (°C/W)

The REF50xx junction temperature must not exceed the absolute maximum rating of +150°C.

NOISE PERFORMANCE

Typical 0.1Hz to 10Hz voltage noise for each member of the REF50xx family is specified in the [Electrical Characteristics: Per Device](#) table. The noise voltage increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade performance.

APPLICATION CIRCUITS

NEGATIVE REFERENCE VOLTAGE

For applications requiring a negative and positive reference voltage, the REF50xx and OPA735 can be used to provide a dual-supply reference from a 5V supply. Figure 26 shows the REF5025 used to provide a 2.5V supply reference voltage. The low drift performance of the REF50xx complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Care must be taken to match the temperature coefficients of R_1 and R_2 .

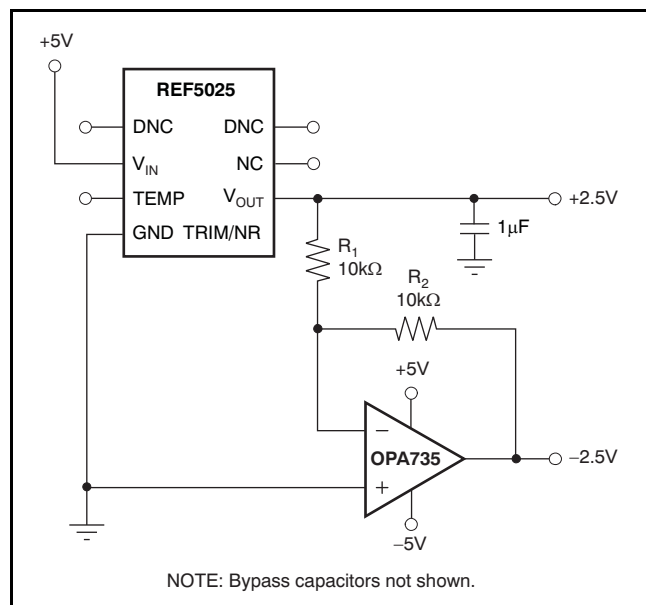


Figure 26. The REF5025 and OPA735 Create Positive and Negative Reference Voltages

DATA ACQUISITION

Data acquisition systems often require stable voltage references to maintain accuracy. The REF50xx family features low noise, very low drift, and high initial accuracy for high-performance data converters. Figure 27 shows the REF5040 in a basic data acquisition system.

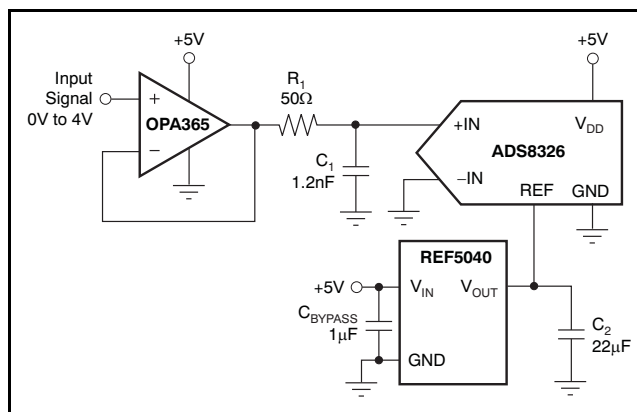


Figure 27. Basic Data Acquisition System

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
REF5010AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5010AIDGKR	PREVIEW	MSOP	DGK	8	2500	TBD	Call TI	Call TI
REF5010AIDGKT	PREVIEW	MSOP	DGK	8	250	TBD	Call TI	Call TI
REF5010AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5010ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5010IDGKR	PREVIEW	MSOP	DGK	8	2500	TBD	Call TI	Call TI
REF5010IDGKT	PREVIEW	MSOP	DGK	8	250	TBD	Call TI	Call TI
REF5010IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5020AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5020AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5020AIDGKR	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5020AIDGKT	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5020AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5020AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5020ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5020IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5020IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5020IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5025AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5025AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5025AIDGKR	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5025AIDGKT	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5025AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5025AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5025ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5025IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5025IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5025IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
REF5030AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5030AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5030AIDGKR	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5030AIDGKT	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5030AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5030AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5030ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5030IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5030IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5030IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5040AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5040AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5040AIDGKR	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5040AIDGKT	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5040AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5040AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5040ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5040IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5040IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5040IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5045AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5045AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5045AIDGKR	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5045AIDGKT	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5045AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5045AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5045ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5045IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
REF5045IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5045IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5050AID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5050AIDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5050AIDGKR	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5050AIDGKT	PREVIEW	MSOP	DGK	8		TBD	Call TI	Call TI
REF5050AIDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5050AIDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5050ID	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5050IDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5050IDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
REF5050IDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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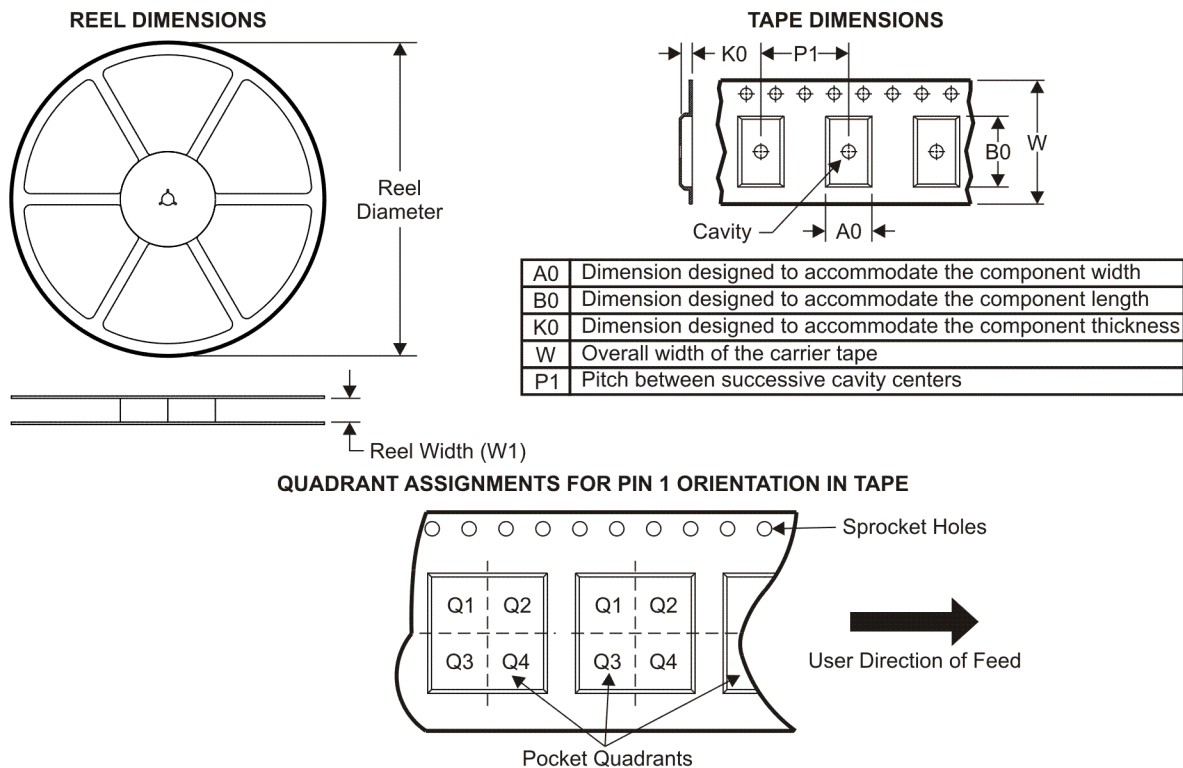
OTHER QUALIFIED VERSIONS OF REF5020 :

- Automotive: [REF5020-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

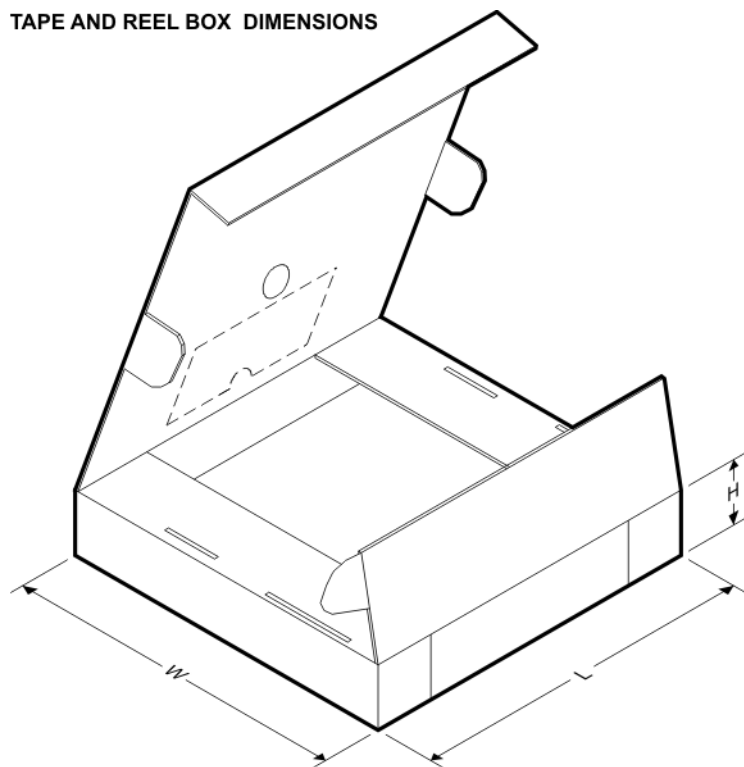
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF5010IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5020AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5020IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5025IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5030IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5040IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5045IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
REF5050IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

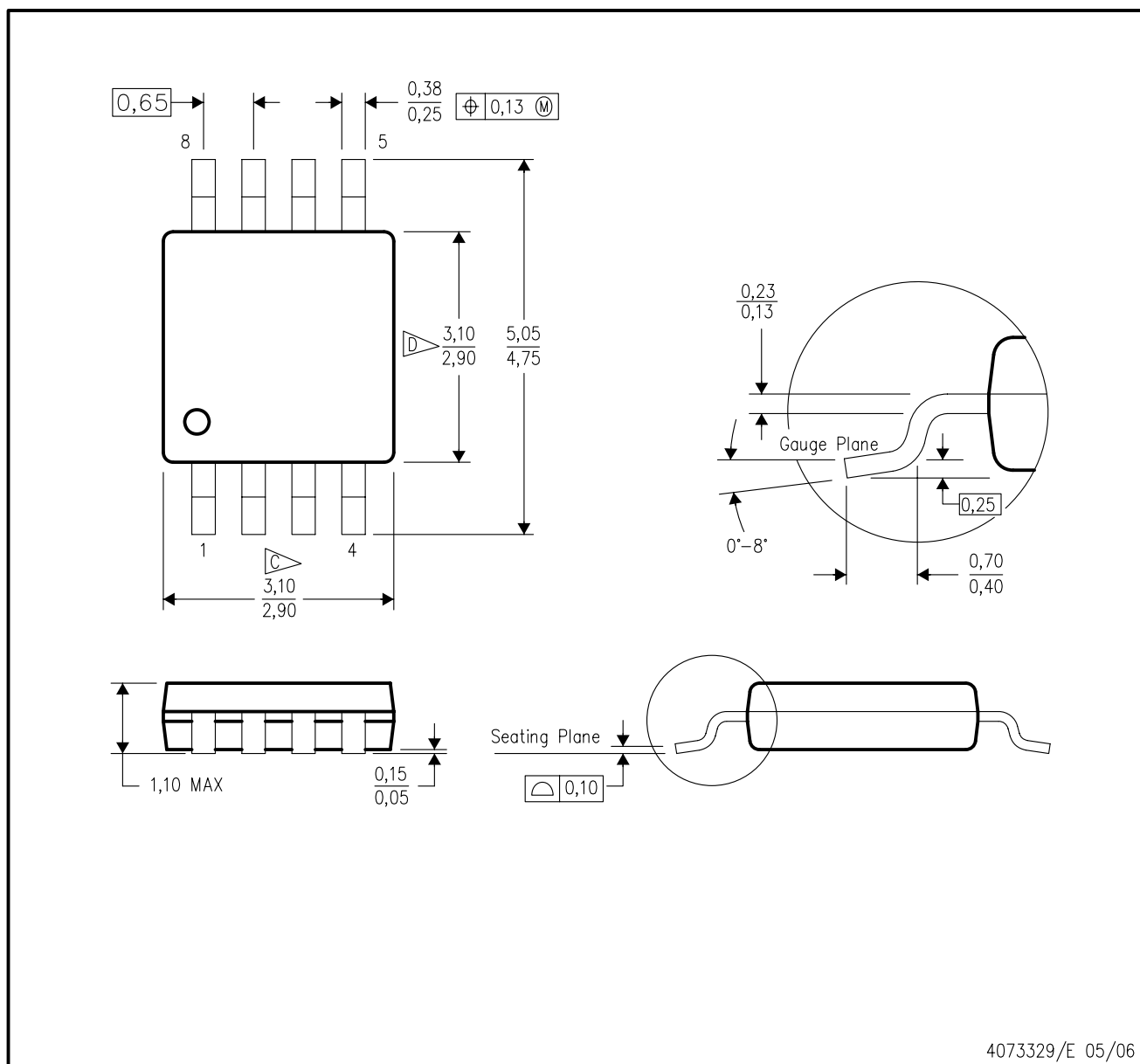


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF5010IDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5020AIDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5020IDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5025AIDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5025IDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5030AIDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5030IDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5040AIDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5040IDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5045AIDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5045IDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5050AIDR	SOIC	D	8	2500	346.0	346.0	29.0
REF5050IDR	SOIC	D	8	2500	346.0	346.0	29.0

DGK (S-PDSO-G8)

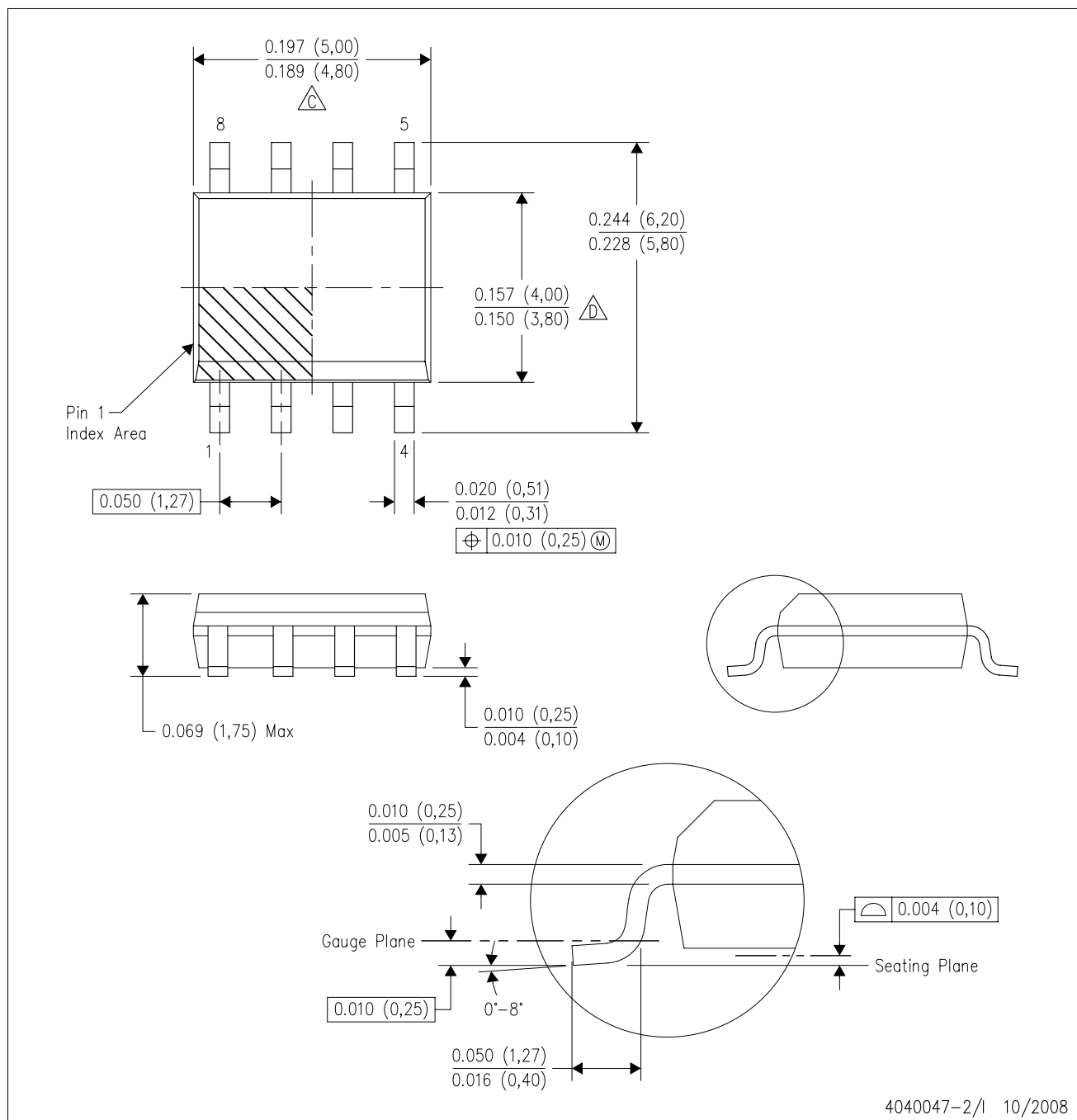
PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
- $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
- E. Reference JEDEC MS-012 variation AA.

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