

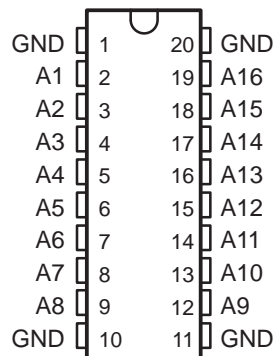
SN74F1016

16-BIT SCHOTTKY BARRIER DIODE R-C BUS-TERMINATION ARRAY

SDFS093 – NOVEMBER 1992 – REVISED DECEMBER 1993

- Designed to Reduce Reflection Noise
- Repetitive Peak Forward Current . . . 300 mA
- 16-Bit Array Structure Suited for Bus-Oriented Systems

DW PACKAGE
(TOP VIEW)

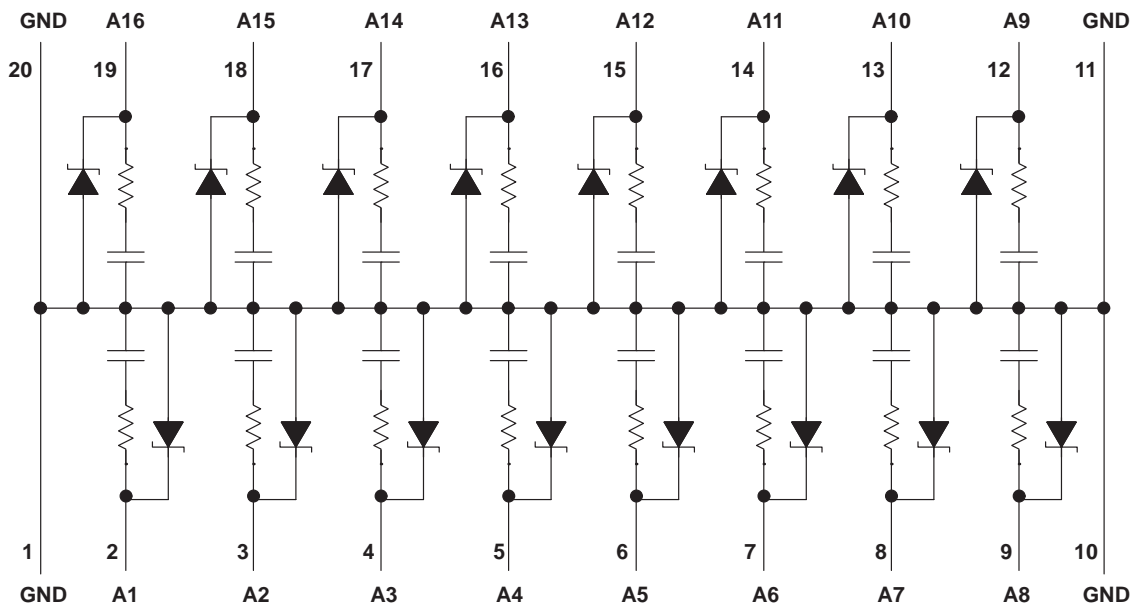


description

This bus-termination array is designed to reduce reflection noise and minimize ringing on high-performance bus lines. The SN74F1016 features a 16-bit R-C network and Schottky barrier diode array. These Schottky diodes provide clamp-to-ground functionality and serve to minimize overshoot and undershoot of high-speed switching buses.

The SN74F1016 is characterized for operation from 0°C to 70°C.

schematic diagram



- Resistor = 50 Ω ± 10%
 Capacitor = 47 pF ± 10%, V_R = 2.5 V, f = 1 MHz
 Diode = Schottky

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



Copyright © 1993, Texas Instruments Incorporated

SN74F1016
16-BIT SCHOTTKY BARRIER DIODE
R-C BUS-TERMINATION ARRAY

SDFS093 – NOVEMBER 1992 – REVISED DECEMBER 1993

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Steady-state reverse voltage, V_R	7 V
Continuous forward current, I_F : Any D terminal from GND	50 mA
Total through all GND terminals	170 mA
Repetitive peak forward current, I_{FRM}^\ddagger : Any D terminal from GND	300 mA
Total through all GND terminals	1.2 A
Continuous total power dissipation at (or below) 25°C free-air temperature	500 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ These values apply for $t_W \leq 100 \mu s$, duty cycle $\leq 20\%$.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

single-diode operation (see Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_R Static reverse current	$V_R = 7 V$			2	μA
V_{FM} Peak forward voltage	$I_F = 200 mA$		1.25		V
C_t Total capacitance	$V_R = 0$			80	pF
	$V_R = 2 V$			60	
	$V_R = 3 V$			55	

† All typical values are at $T_A = 25^\circ C$.

NOTE 1: Test conditions and limits apply separately to each of the diodes. The diodes not under test are open-circuited during the measurement of these characteristics.

multiple-diode operation

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_x Internal crosstalk current	Total GND current = 1.2 A, See Note 2		10	50	μA

NOTE 2: I_x is measured under the following conditions with one diode static, all others switching:
 Switching diodes: $t_W = 100 \mu s$, duty cycle = 20%;
 Static diode: $V_R = 5 V$; the static diode input current is the internal crosstalk current I_x .

switching characteristics, $T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{rr} Reverse recovery time	$I_F = 10 mA$, $I_{RM(REC)} = 10 mA$, $I_{R(REC)} = 1 mA$, $R_L = 100 \Omega$		8	10	ns

undershoot characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{US} Undershoot voltage	$t_f = 2 ns$, $t_W = 50 ns$, $V_{IH} = 5 V$, $V_{IL} = 0$, $Z_S = 25 \Omega$, $Z_O = 50 \Omega$, L = 36-inch coaxial cable		0.7	0.8	V



APPLICATION INFORMATION

Large negative transients occurring at the inputs of memory devices (DRAMs, SRAMs, EPROMs, etc.) or on the CLOCK lines of many clocked devices can result in improper operation of the devices. The SN74F1016 diode termination array helps suppress negative transients caused by transmission line reflections, crosstalk, and switching noise.

Diode terminations have several advantages when compared to resistor termination schemes. Split resistor or Thevenin equivalent termination can cause a substantial increase in power consumption. The use of a single resistor to ground to terminate a line usually results in degradation of the output high level, resulting in reduced noise immunity. Series damping resistors placed on the outputs of the driver will reduce negative transients, but they can also increase propagation delays down the line, as a series resistor reduces the output drive capability of the driving device. Diode terminations have none of these drawbacks.

The operation of the diode arrays in reducing negative transients is explained in Figure 1. The diode conducts current whenever the voltage reaches a negative value large enough for the diode to turn on. Suppression of negative transients is tracked by the current-voltage characteristic curve for that diode. A typical current voltage for the SN74F1016 is shown in Figure 1.

The maximum effectiveness of the diode arrays in suppressing negative transients occurs when they are placed at the end of a line and/or the end of a long stub branching off a main transmission line. The diodes can also be used to reduce the negative transients that occur due to discontinuities in the middle of a line. An example of this is a slot in a backplane that is provided for an add-on card.

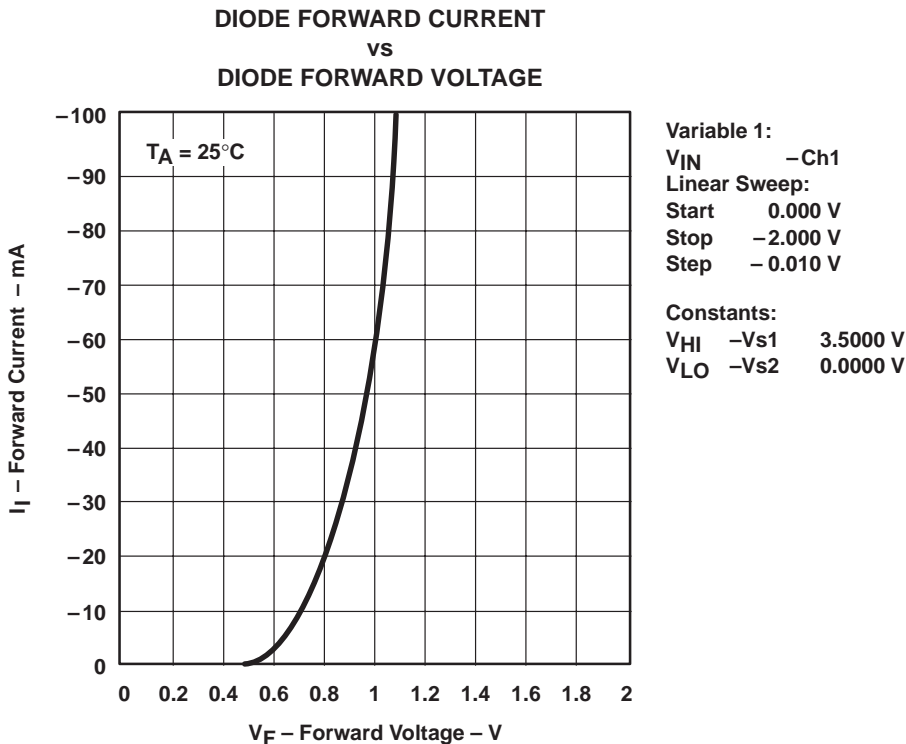
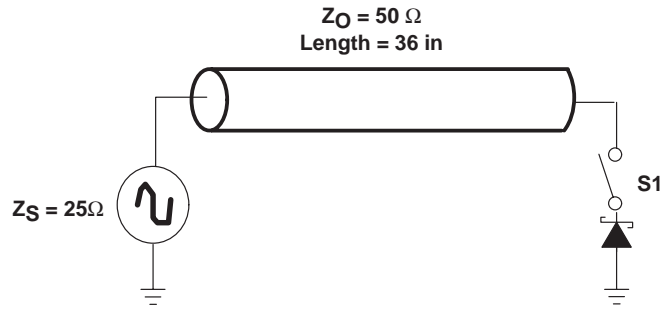


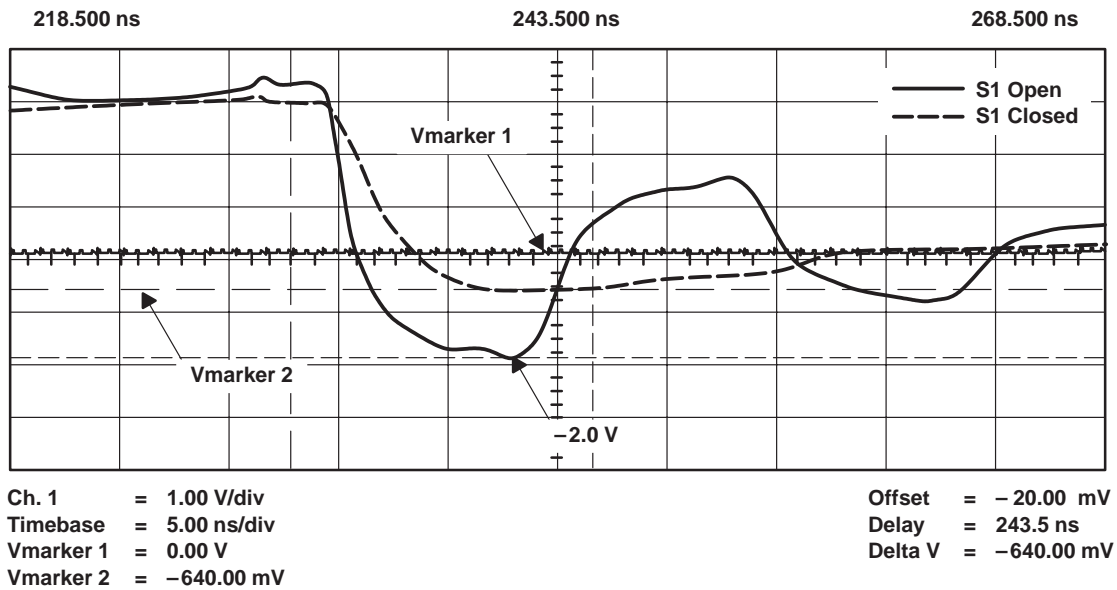
Figure 1

SN74F1016
16-BIT SCHOTTKY BARRIER DIODE
R-C BUS-TERMINATION ARRAY

SDFS093 – NOVEMBER 1992 – REVISED DECEMBER 1993



(a) UNDERSHOOT TEST SETUP



(b) SCOPE DISPLAY

Figure 2. Undershoot Test Setup and Scope Display

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.