ISO 7816 Compatible

2K X76F200 256 x 8 bit

Secure SerialFlash

FEATURES

- **64-bit Password Security**
- **One Array (240 Bytes) Two Passwords (16 Bytes)**
  - **—Read Password**
  - **—Write Password**
- **Programmable Passwords**
- **Retry Counter Register**
  - **—Allows 8 tries before clearing of the array**
- **32-bit Response to Reset (RST Input)**
- **8 byte Sector Write mode**
- **1MHz Clock Rate**
- **2 wire Serial Interface**
- **Low Power CMOS**
  - **—2.0 to 5.5V operation**
  - **—Standby current Less than 1µA**
  - **—Active current less than 3 mA**
- **High Reliability Endurance:**
  - **—100,000 Write Cycles**
- **Data Retention: 100 years**
- **Available in:**
  - **—8 lead PDIP, SOIC, TSSOP, Smart Card and Smart Card Module**

DESCRIPTION

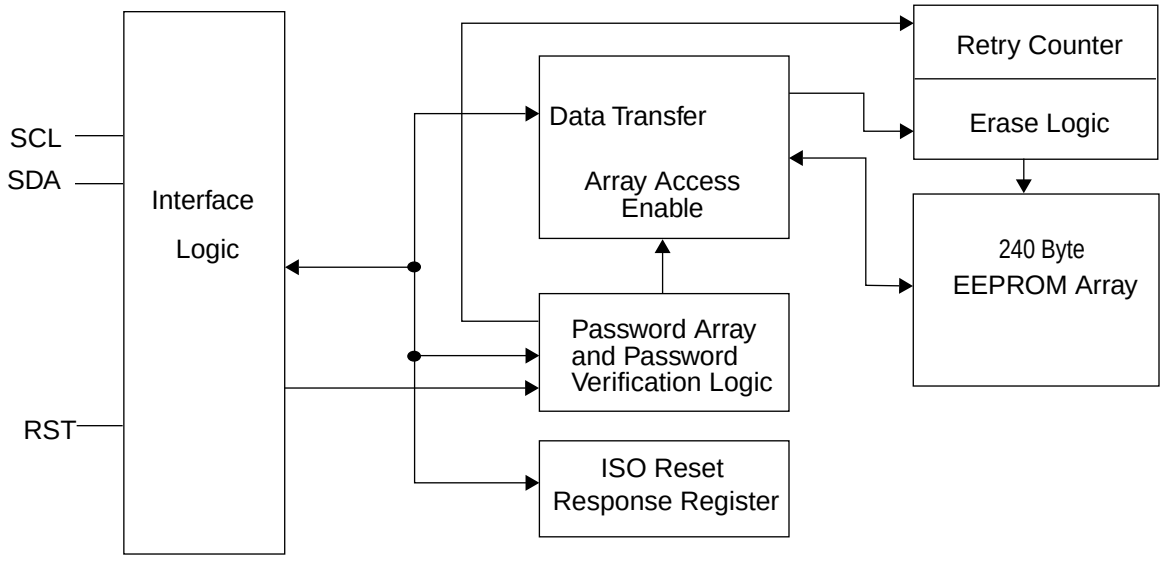
The X76F200 is a Password Access Security Supervisor, containing one 1920-bit Secure SerialFlash array. Access to the memory array can be controlled by two 64-bit passwords. These passwords protect read and write operations of the memory array.

The X76F200 features a serial interface and software protocol allowing operation on a popular two wire bus. The bus signals are a clock Input (SCL) and a bidirectional data input and output (SDA).

The X76F200 also features a synchronous response to reset providing an automatic output of a hard-wired 32-bit data stream conforming to the industry standard for memory cards.

The X76F200 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles and a minimum data retention of 100 years.

Functional Diagram



©Xicor, Inc. 1999 Patents Pending

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is an open drain serial data input/output pin. During a read cycle, data is shifted out on this pin. During a write cycle, data is shifted in on this pin. In all other cases, this pin is in a high impedance state.

Reset (RST)

RST is a device reset pin. When RST is pulsed high the X76F200 will output 32 bits of fixed data which conforms to the standard for “synchronous response to reset”. The part must not be in a write cycle for the response to reset to occur. See Figure 7. If there is power interrupted during the Response to Reset, the response to reset will be aborted and the part will return to the standby state. The response to reset is "mask programmable" only!

DEVICE OPERATION

The X76F200 memory array consists of thirty 8-byte sectors. Read or write access to the array always begins at the first address of the sector. Read operations then can continue indefinitely. Write operations must total 8 bytes.

There are two primary modes of operation for the X76F200; Protected READ and protected WRITE. Protected operations must be performed with one of two 8-byte passwords.

The basic method of communication for the device is generating a start condition, then transmitting a command, followed by the correct password. All parts will be shipped from the factory with all passwords equal to ‘0’. The user must perform ACK Polling to determine the validity of the password, before starting a data transfer (see Acknowledge Polling.) Only after the correct password is accepted and a ACK polling has been performed, can the data transfer occur.

To ensure the correct communication, RST must remain LOW under all conditions except when running a “Response to Reset sequence”.

Data is transferred in 8-bit segments, with each transfer being followed by an ACK, generated by the receiving device.

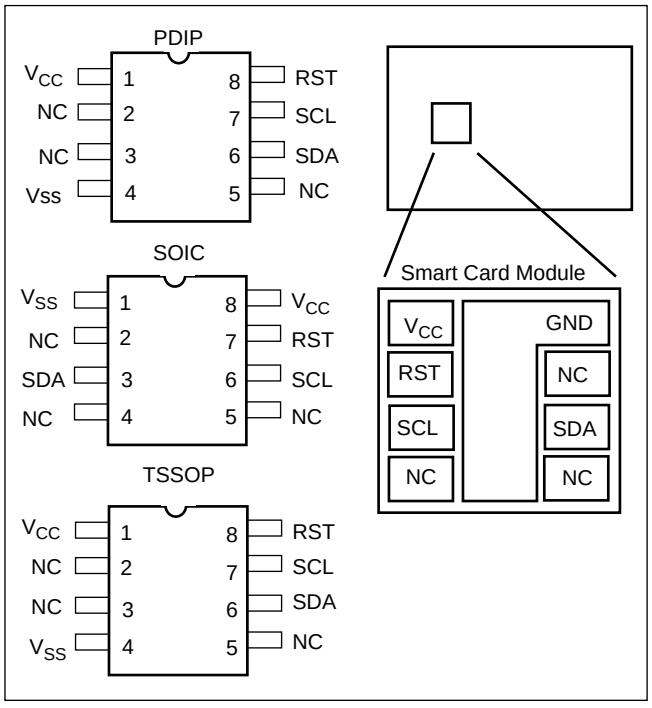
If the X76F200 is in a nonvolatile write cycle a “no ACK” (SDA=High) response will be issued in response to loading of the command byte. If a stop is issued prior to the nonvolatile write cycle the write operation will be terminated and the part will reset and enter into a standby mode.

The basic sequence is illustrated in Figure 1.

PIN NAMES

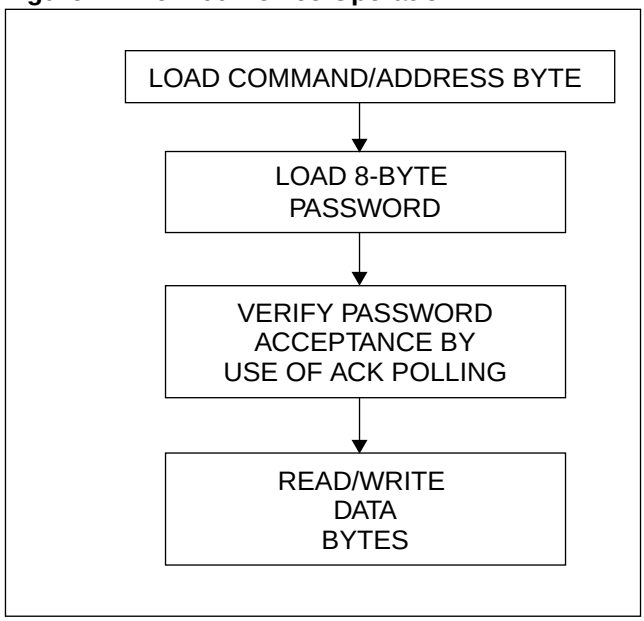
Symbol	Description
SDA	Serial Data Input/Output
SCL	Serial Clock Input
RST	Reset Input
Vcc	Supply Voltage
Vss	Ground
NC	No Connect

PIN CONFIGURATION



After each transaction is completed, the X76F200 will reset and enter into a standby mode. This will also be the response if an unsuccessful attempt is made to access a protected array.

Figure 1. X76F200 Device Operation



Retry Counter

The X76F200 contains a retry counter. The retry counter allows 8 accesses with an invalid password before any action is taken. The counter will increment with any combination of incorrect passwords. If the retry counter overflows, the memory area and both of the passwords are cleared to "0". If a correct password is received prior to retry counter overflow, the retry counter is reset and access is granted.

Device Protocol

The X76F200 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as a receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X76F200 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figure 2 and Figure 3.

Start Condition

All commands are preceeded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X76F200 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition is met.

A start may be issued to terminate the input of a control byte or the input data to be written. This will reset the device and leave it ready to begin a new read or write command. Because of the push/pull output, a start cannot be generated while the part is outputting data. Starts are inhibited while a write is in progress.

Stop Condition

All communications must be terminated by a stop condition. The stop condition is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to reset the device during a command or data input sequence and will leave the device in the standby power mode. As with starts, stops are inhibited when outputting data and while a write is in progress.

Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data.

The X76F200 will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write condition have been selected, the X76F200 will respond with an acknowledge after the receipt of each subsequent eight-bit word.

Figure 2. Data Validity

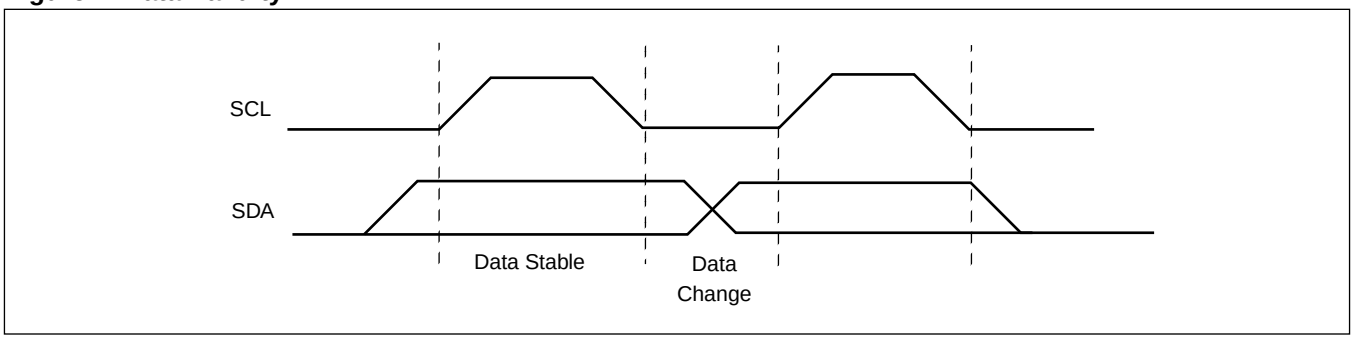


Figure 3. Definition of Start and Stop Conditions

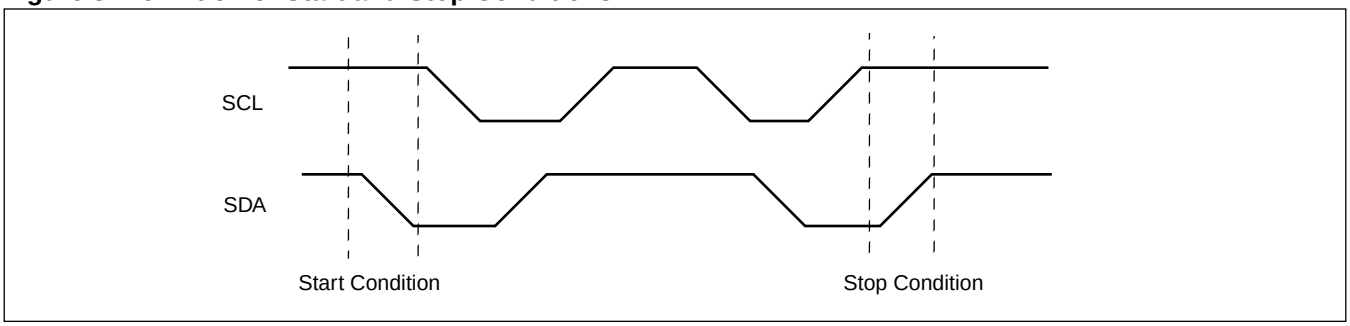


Table 1. X76F200 Instruction Set

Command after Start	Command Description	Password used
1 0 S_4 S_3 S_2 S_1 S_0 0	Sector Write	Write
1 0 S_4 S_3 S_2 S_1 S_0 1	Sector Read	Read
1 1 1 1 1 1 0 0	Change Write Password	Write
1 1 1 1 1 1 1 0	Change Read Password	Write
0 1 0 1 0 1 0 1	Password ACK Command	None

Illegal command codes will be disregarded. The part will respond with a “no-ACK” to the illegal byte and then return to the standby mode. All write/read operations require a password.

PROGRAM OPERATIONS

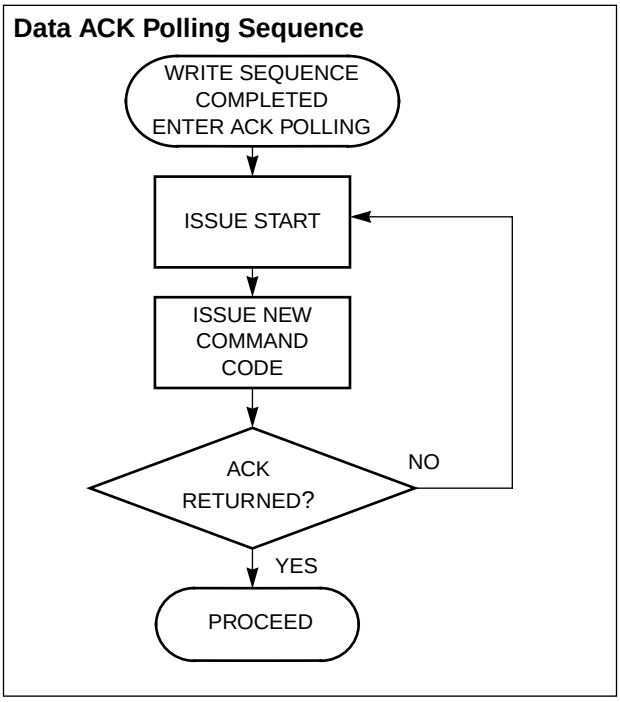
Sector Write

The sector write mode requires issuing the 8-bit write command followed by the password and then the data bytes transferred as illustrated in figure 4. The write command byte contains the address of the sector to be written. Data is written starting at the first address of a sector and eight bytes must be transferred. After the last byte to be transferred is acknowledged a stop condition is issued which starts the nonvolatile write cycle. If more or less than 8 bytes are transferred, the data in the sector remains unchanged.

ACK Polling

Once a stop condition is issued to indicate the end of the host’s write sequence, the X76F200 initiates the internal nonvolatile write cycle. In order to take advantage of the typical 5ms write cycle, ACK polling can begin immediately. This involves issuing the start condition

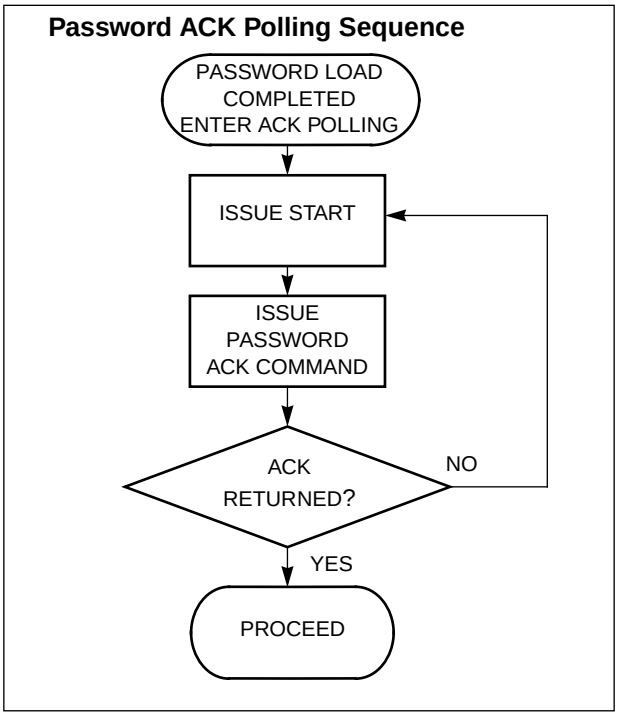
followed by the new command code of 8 bits (1st byte of the protocol.) If the X76F200 is still busy with the nonvolatile write operation, it will issue a “no-ACK” in response. If the nonvolatile write operation has completed, an “ACK” will be returned and the host can then proceed with the rest of the protocol.



After the password sequence, there is always a nonvolatile write cycle. This is done to discourage random guesses of the password if the device is being tampered with. In order to continue the transaction, the X76F200 requires the master to perform a password ACK polling sequence with the specific command code of 55h. As with regular Acknowledge polling the user can either time out for 10ms, and then issue the ACK polling once, or continuously loop as described in the flow.

If the password that was inserted was correct, then an “ACK” will be returned once the nonvolatile cycle in response to the passwrod ACK polling sequence is over.

If the password that was inserted was incorrect, then a “no ACK” will be returned even if the nonvolatile cycle is over. Therefore, the user cannot be certain that the password is incorrect until the 10ms write cycle time has elapsed.



READ OPERATIONS

Read operations are initiated in the same manner as write operations but with a different command code.

Sector Read

With sector read, a sector address is supplied with the read command. Once the password has been acknowledged data may be read from the sector. An acknowledge must follow each 8-bit data transfer. A read operation always begins at the first byte in the sector, but may stop at any time. Random accesses to the array are not possible. Continuous reading from the array will return data from successive sectors. After reading the last sector in the array, the address is automatically set to the first sector in the array and data can continue to be read out. After the last bit has been read, a stop condition is generated without sending a preceding acknowledge.

Figure 4. Sector Write Sequence (Password Required)

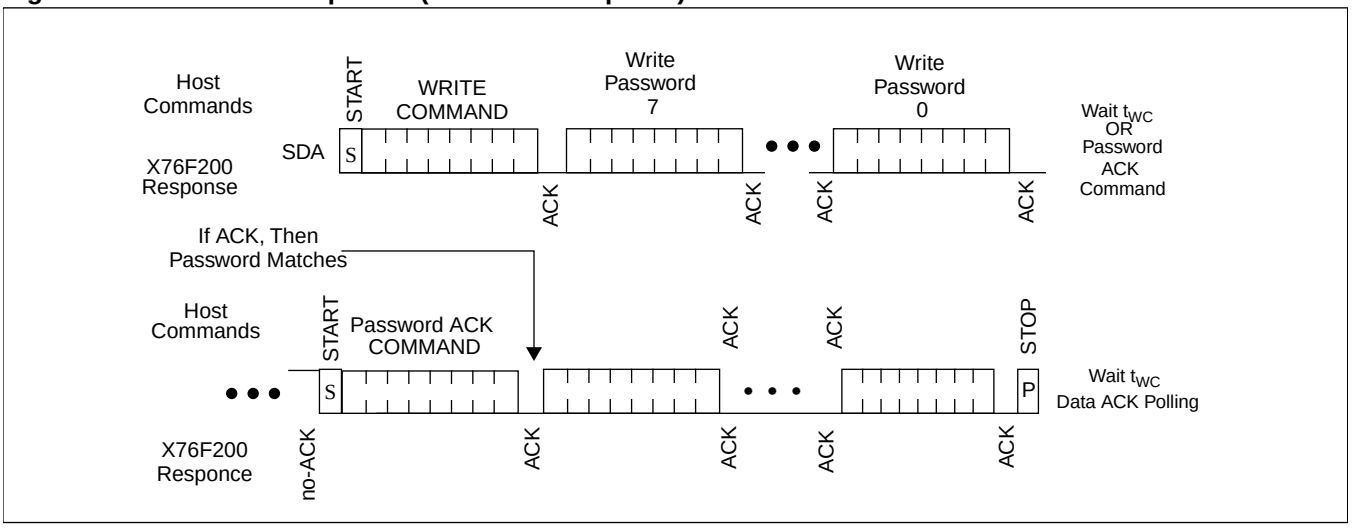


Figure 5. Acknowledge Polling

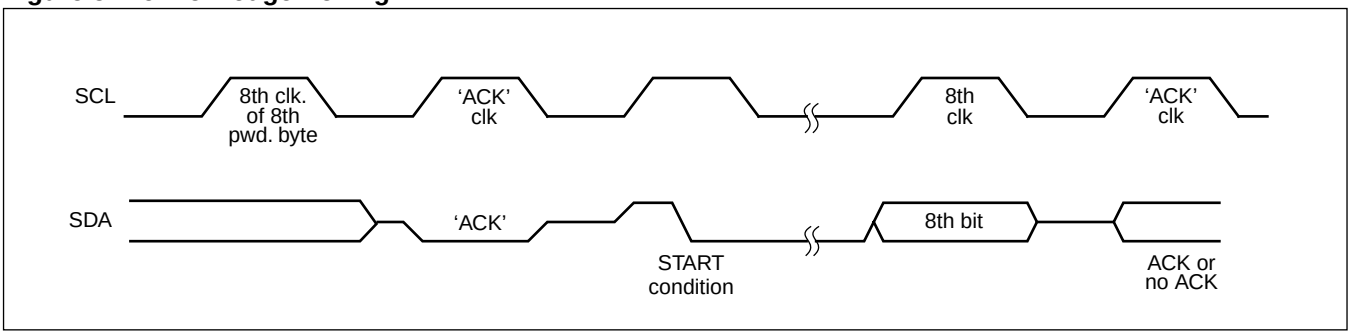
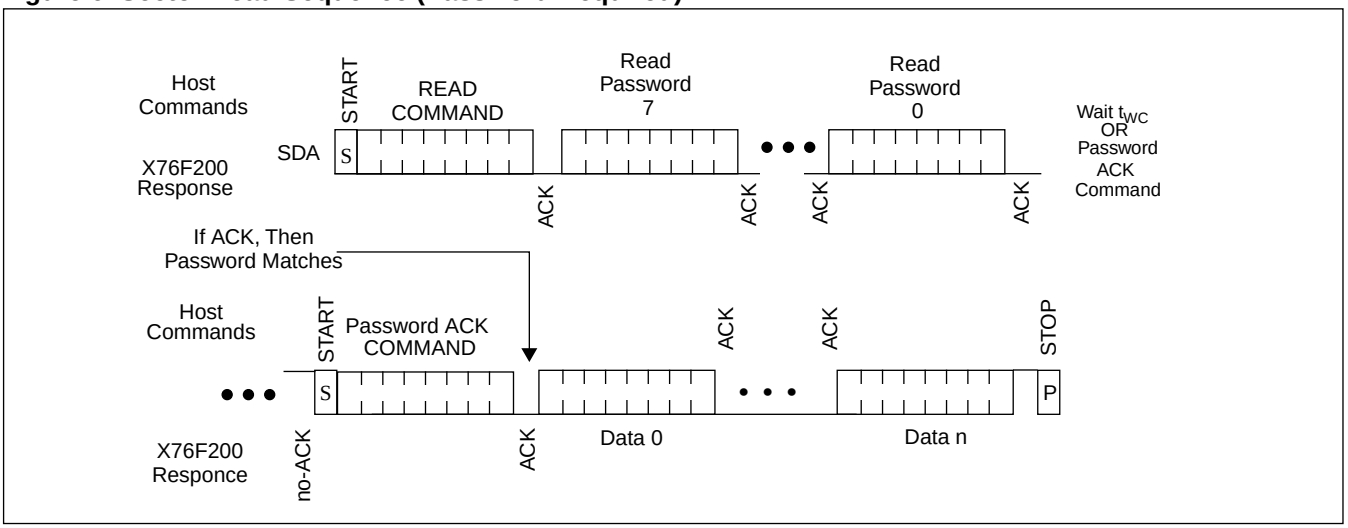


Figure 6. Sector Read Sequence (Password Required)



PASSWORDS

Passwords are changed by sending the "change read password" or "change write password" commands in a normal sector write operation. A full eight bytes containing the new password must be sent, following successful transmission of the current write password and a valid password ACK response. The user can use a repeated ACK Polling command to check that a new password has been written correctly. An ACK indicates that the new password is valid.

There is no way to read any of the passwords.

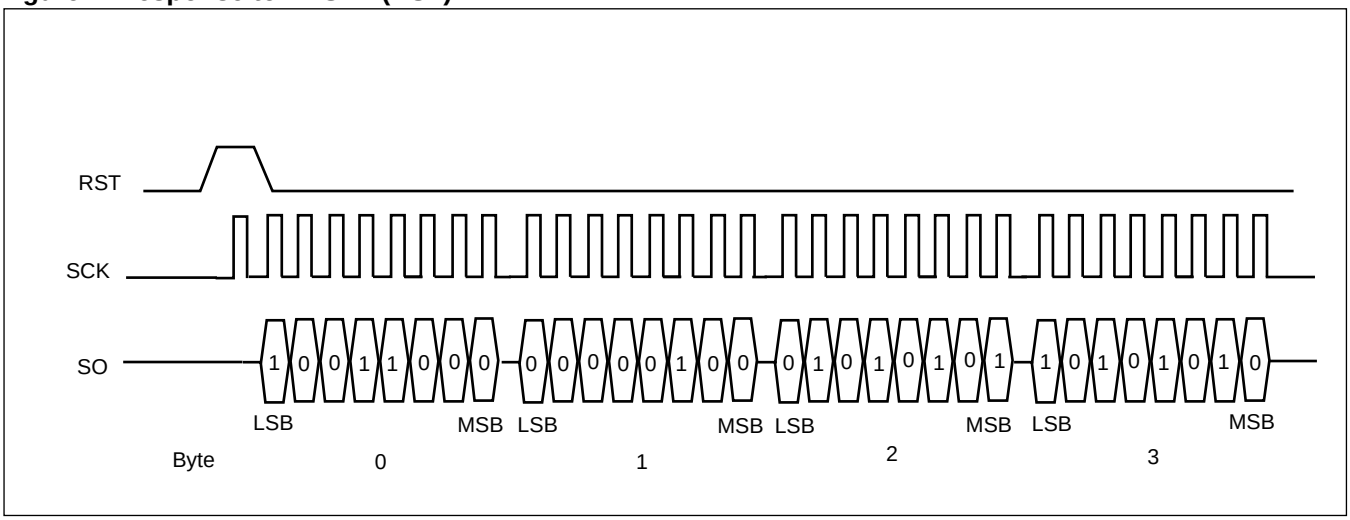
RESPONSE TO RESET (DEFAULT = 19 20 AA 55)

The ISO Response to reset is controlled by the RST and CLK pins. When RST is pulsed high during a clock pulse, the device will output 32 bits of data, one bit per clock, and it resets to the standy state. This conforms to the ISO standard for “synchronous response to reset”. The part must not be in a write cycle for the response to reset to occur.

After initiating a nonvolatile write cycle the RST pin must not be pulsed until the nonvolatile write cycle is complete. If not, the ISO response will not be activated. If the RST is pulsed HIGH and the CLK is within the RST pulse (meet the t_{NOL} spec.) in the middle of an ISO transaction, it will output the 32 bit sequence again (starting at bit 0). Otherwise, this aborts the ISO operation and the part returns to standby state. If the RST is pulsed HIGH and the CLK is outside the RST pulse (in the middle of an ISO transaction), this aborts the ISO operation and the part returns to standby state.

If there is power interrupted during the Response to Reset, the response to reset will be aborted and the part will return to the standby state. A Response to Reset is not available during a nonvolatile write cycle.

Figure 7. Response to RESET (RST)



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature .....–65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} .....–1V to +7V
D.C. Output Current.....5mA
Lead Temperature
(Soldering, 10 seconds)..... 300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temp	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

Supply Voltage	Limits
X76F200	4.5V to 5.5V
X76F200 – 2	2.0V to 5.5V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Read)		1	mA	$f_{SCL} = V_{CC} \times 0.1/V_{CC} \times 0.9$ Levels @ 400 KHz, SDA = Open, RST = V_{SS}
I_{CC2}(3)	V_{CC} Supply Current (Write)		3	mA	$f_{SCL} = V_{CC} \times 0.1/V_{CC} \times 0.9$ Levels @ 400 KHz, SDA = Open, RST = V_{SS}
I_{SB1}(1)	V_{CC} Supply Current (Standby)		1	µA	$V_{IL} = V_{CC} \times 0.1$, $V_{IH} = V_{CC} \times 0.9$ f_{SCL} = 400 KHz, f_{SDA} = 400 KHz
I_{SB2}(1)	V_{CC} Supply Current (Standby)		1	µA	$V_{SDA} = V_{SCC} = V_{CC}$ Other = GND or V_{CC}–0.3V
I_{LI}	Input Leakage Current		10	µA	$V_{IN} = V_{SS}$ to V_{CC}
I_{LO}	Output Leakage Current		10	µA	$V_{OUT} = V_{SS}$ to V_{CC}
V_{IL}(2)	Input LOW Voltage	–0.5	$V_{CC} \times 0.1$	V	
V_{IH}(2)	Input HIGH Voltage	$V_{CC} \times 0.9$	$V_{CC} + 0.5$	V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3mA

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

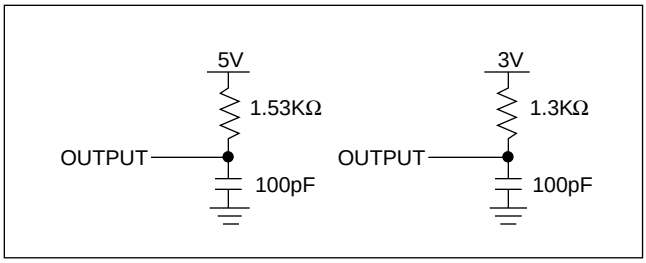
Symbol	Test	Max.	Units	Conditions
C_{OUT}(3)	Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance (RST, SCL)	6	pF	V_{IN} = 0V

NOTES: (1) Must perform a stop command after a read command prior to measurement

(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

(3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10ns
Input and Output Timing Level	$V_{CC} \times 0.5$
Output Load	100pF

AC CHARACTERISTICS

(T_A = -40˚C to +85˚C, V_{CC} = +2.0V to +5.5V, unless otherwise specified.)

Symbol	Parameter	Min	Max	Units
f_{SCL}	SCL Clock Frequency	0	1	MHz
t_{AA}[2]	SCL LOW to SDA Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	1.2		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
t_{LOW}	Clock LOW Period	1.2		µs
t_{HIGH}	Clock HIGH Period	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	0.6		µs
$t_{HD:DAT}$	Data In Hold Time	10		ns
$t_{SU:DAT}$	Data In Setup Time	100		ns
t_R	SDA and SCL Rise Time	$20+0.1XC_b$[1]	300	ns
t_F	SDA and SCL Fall Time	$20+0.1XC_b$[1]	300	ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{DH}	Data Out Hold Time	0		µs
t_{NOL}	RST to SCL Non-Overlap	500		ns
t_{RDV}	RST LOW to SDA Valid During Response to Reset	0	450	ns
t_{CDV}	CLK LOW to SDA Valid During Response to Reset	0	450	ns
t_{RST}	RST High Time	1.5		µs
$t_{SU:RST}$	RST Setup Time	500		ns

Notes: 1. C_b = total capacitance of one bus line in pF
2. t_{AA} = 1.1µs Max below V_{CC} = 2.0V.

RESET AC SPECIFICATIONS

Power Up Timing

Symbol	Parameter	Min.	Typ[2]	Max.	Units
t_{PUR}[1]	Time from Power Up to Read			1	mS
t_{PUW}[1]	Time from Power Up to Write			5	mS

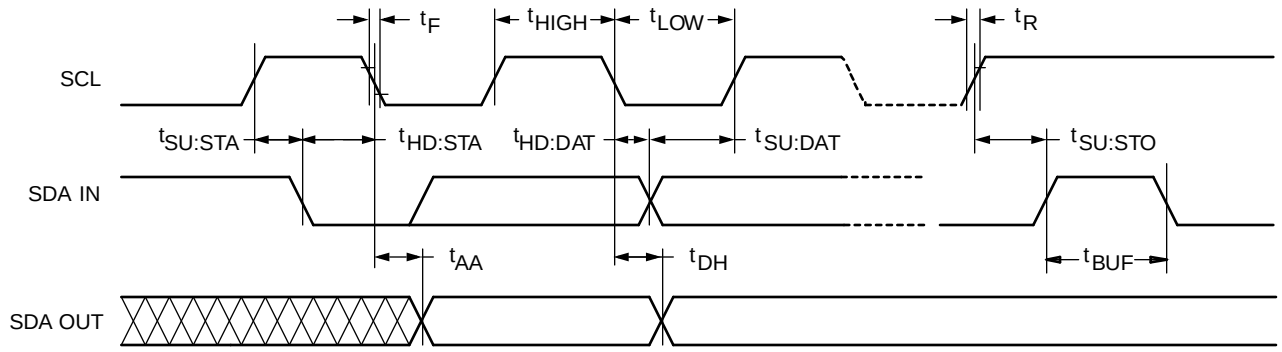
Notes: 1. Delays are measured from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.
2. Typical values are for T_A = 25˚C and V_{CC} = 5.0V

Nonvolatile Write Cycle Timing

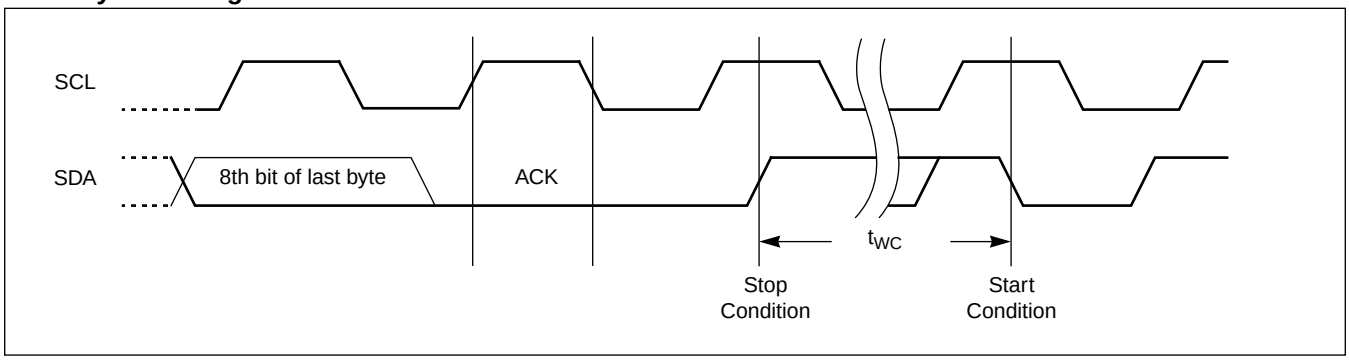
Symbol	Parameter	Min.	Typ.(1)	Max.	Units
t_{WC}[1]	Write Cycle Time		5	10	mS

Notes: 1. t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

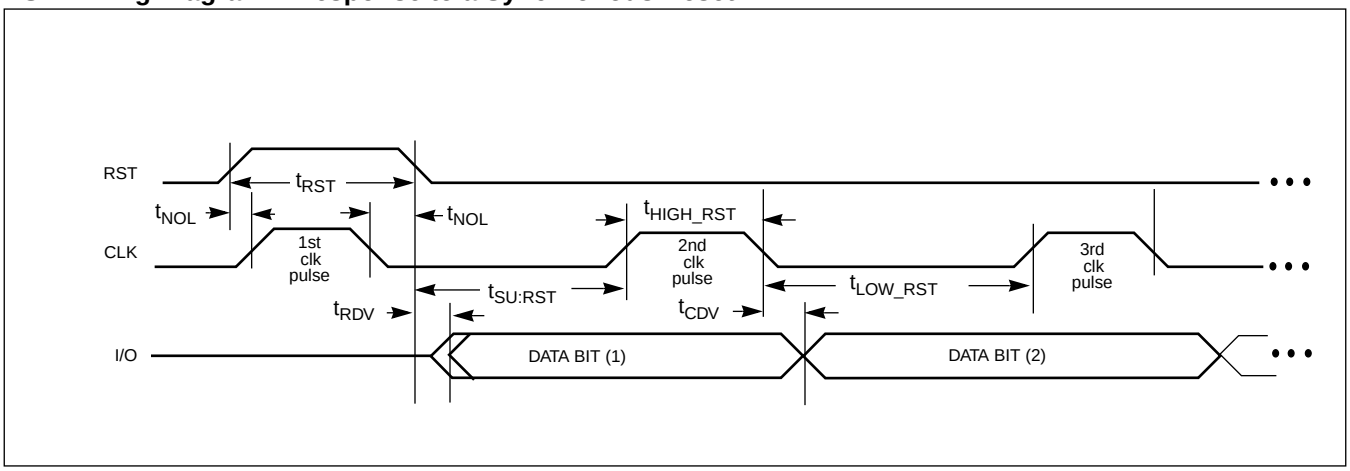
BUS TIMING



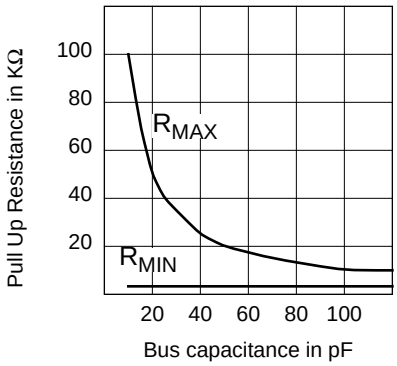
Write Cycle Timing



RST Timing Diagram – Response to a Synchronous Reset



GUIDELINES FOR CALCULATING TYPICAL VALUES OF BUS PULL UP RESISTORS

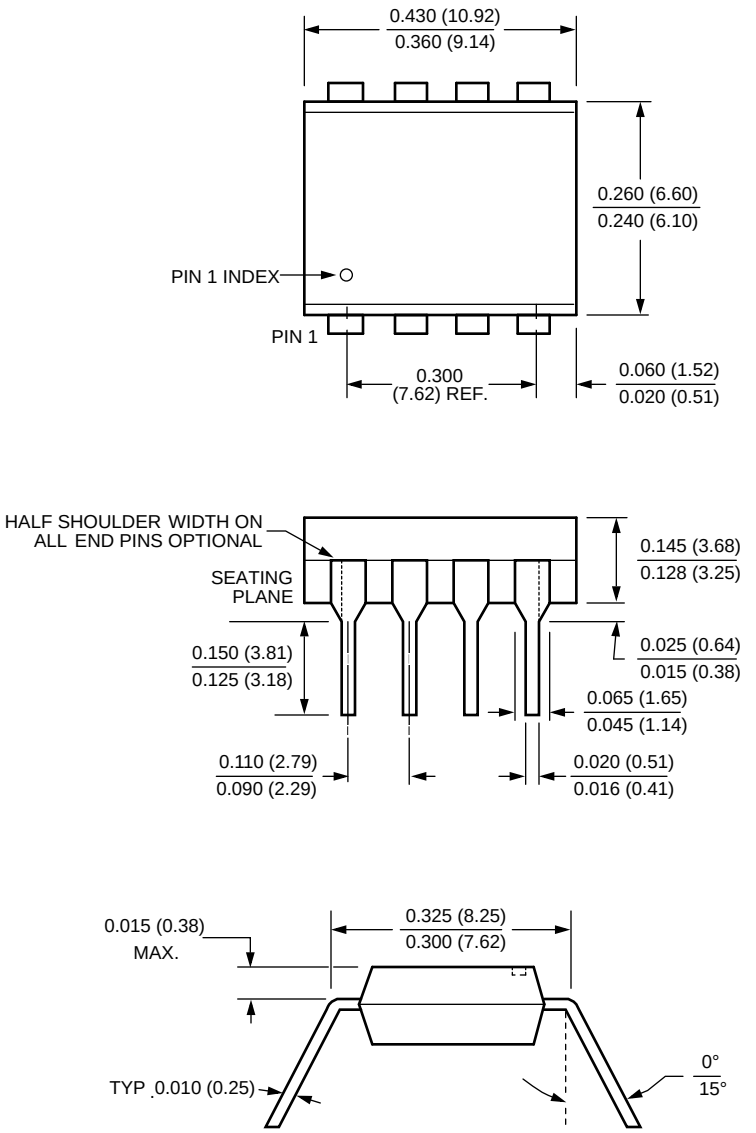


$$R_{MIN} = \frac{V_{CCMAX}}{I_{OLMIN}} = 1.8K\Omega$$

$$R_{MAX} = \frac{t_R}{C_{BUS}}$$

t_R = maximum allowable SDA rise time

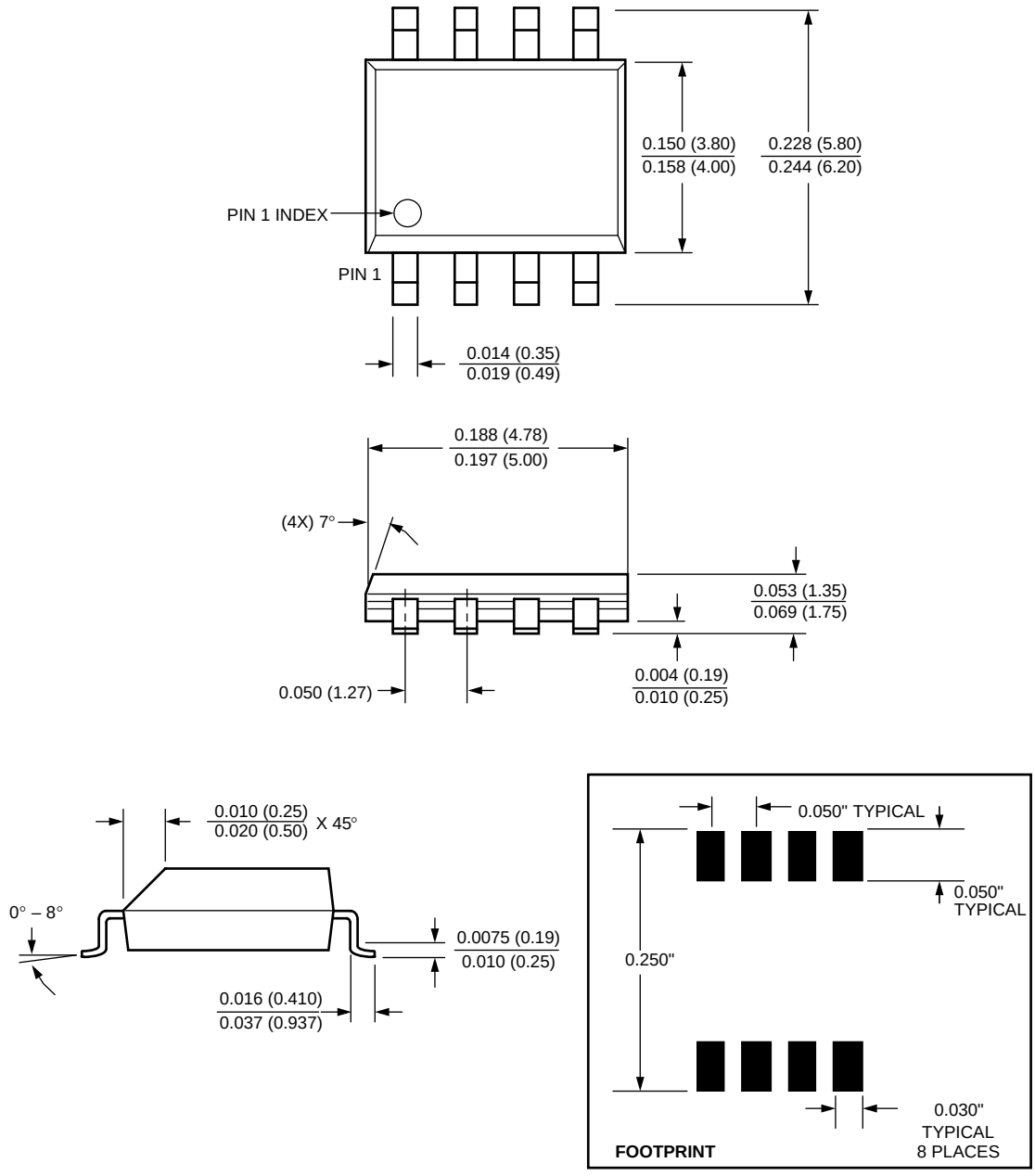
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:

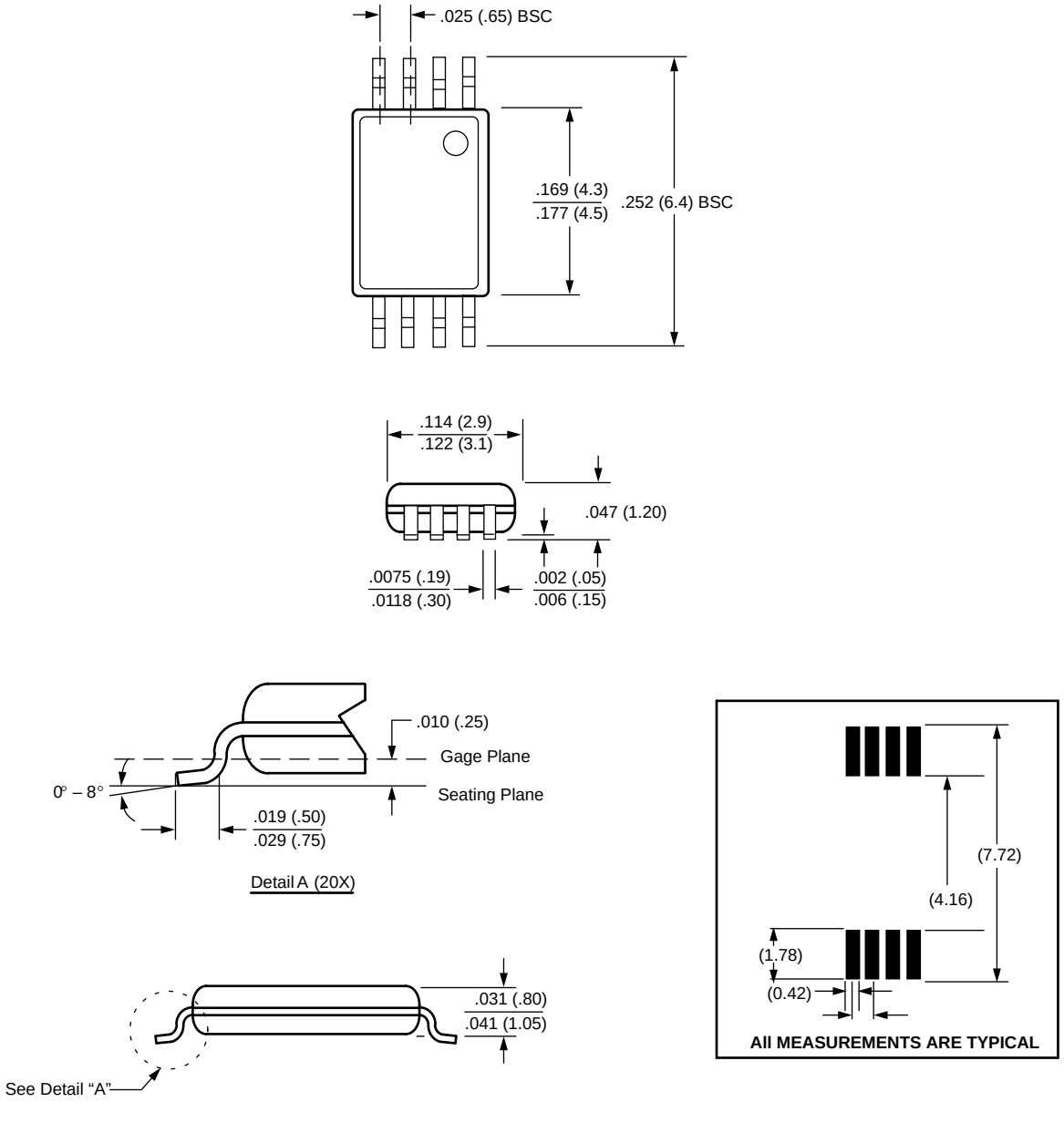
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



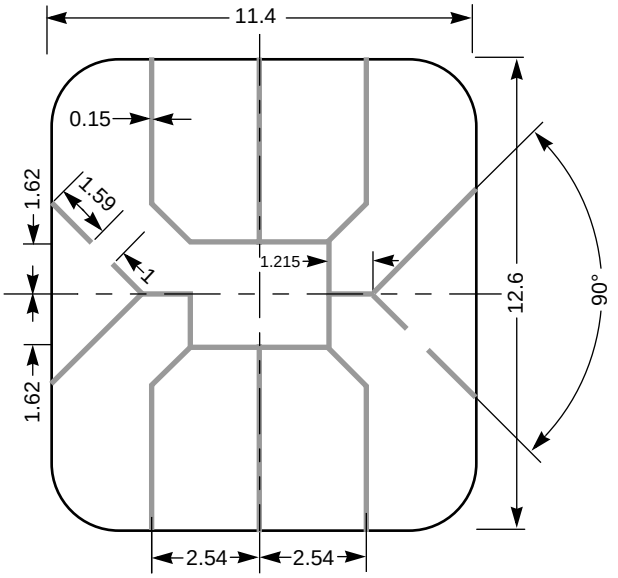
NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

8-LEAD PLASTIC, TSSOP, PACKAGE TYPE V

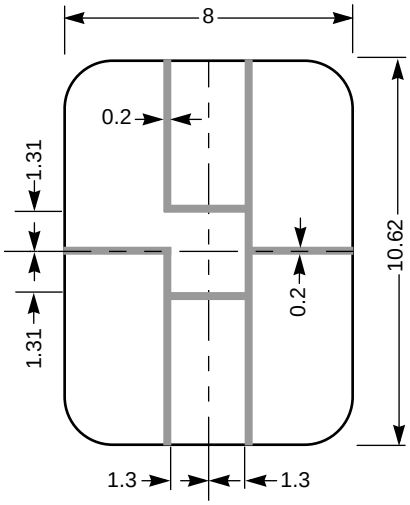


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

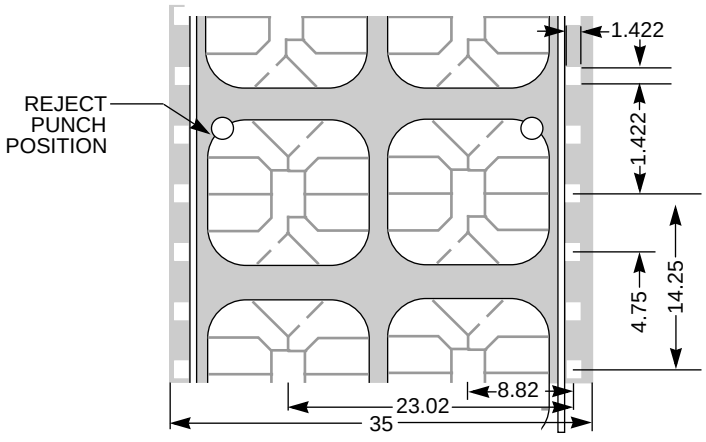
8 CONTACT MODULE



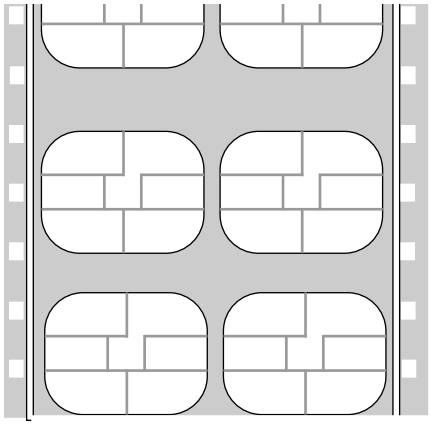
6 CONTACT MODULE



35mm TAPE

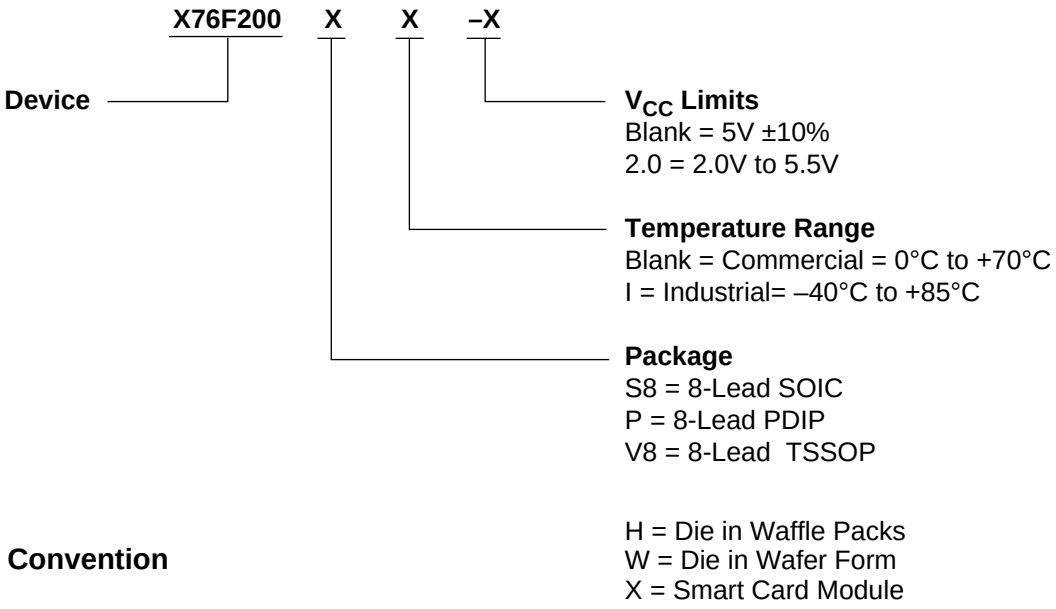


35mm TAPE



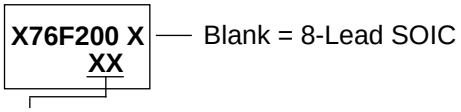
NOTE: ALL MEASUREMENTS IN MILLIMETERS

ORDERING INFORMATION



Part Mark Convention

8-Lead SOIC/PDIP



D = 2.0 to 5.5V, 0 to +70°C
E = 2.0 to 5.5V, -40 to +85°C
Blank = 4.5 to 5.5V, 0 to +70°C
I = 4.5 to 5.5V, -40 to +85°C

8-Lead TSSOP



LIMITED WARRANTY

Devices sold by Xicor, Inc. are covered by the warranty and patent indemnification provisions appearing in its Terms of Sale only. Xicor, Inc. makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Xicor, Inc. makes no warranty of merchantability or fitness for any purpose. Xicor, Inc. reserves the right to discontinue production and change specifications and prices at any time and without notice.

Xicor, Inc. assumes no responsibility for the use of any circuitry other than circuitry embodied in a Xicor, Inc. product. No other circuits, patents, licenses are implied.

U.S. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829, 482; 4,874, 967; 4,883, 976. Foreign patents and additional patents pending.

LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.