WM1824

24-bit 192kHz Stereo DAC with 2Vrms Ground Referenced Line Output

DESCRIPTION

The WM1824 is a stereo DAC with integral charge pump. This provides 2Vrms line driver outputs using a single 3.3V power supply rail.

The device features ground-referenced outputs and the use of a DC servo to eliminate the need for line driving coupling capacitors and effectively eliminate power on pops and clicks.

The device is controlled and configured via a hardware control interface.

The device supports all common audio sampling rates between 8kHz and 192kHz using all common MCLK fs rates. The audio interface operates in slave mode.

The WM1824 has a 3.3V tolerant digital interface, allowing logic up to 3.3V to be connected.

The device is available in a 24-pin QFN.

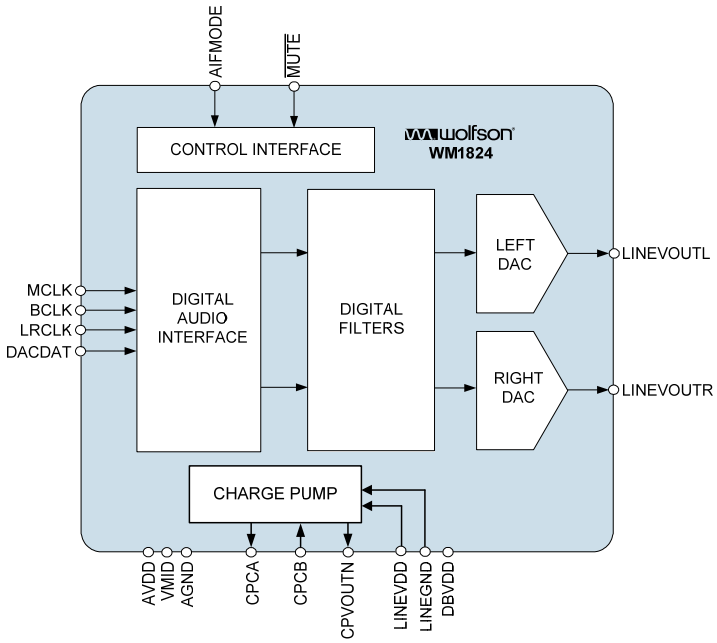
FEATURES

- High performance stereo DAC with ground referenced line driver
- Audio Performance
  - 106dB SNR ('A-weighted')
  - -89dB THD @ -1dBFS
- 120dB mute attenuation
- All common sample rates from 8kHz to 192kHz supported
- Hardware control mode
- Data formats: LJ, I^2S
- Maximum 1mV DC offset on Line Outputs
- Pop/Click suppressed Power Up/Down Sequencer
- AVDD, LINEVDD and DBVDD can operate at +3.3V ±10% allowing single supply
- 24-lead QFN package
- Operating temperature range: -40°C to 85°C

APPLICATIONS

- Consumer digital audio applications requiring 2Vrms output
  - Games Consoles
  - Set Top Box
  - A/V Receivers
  - DVD Players
  - Digital TV

BLOCK DIAGRAM



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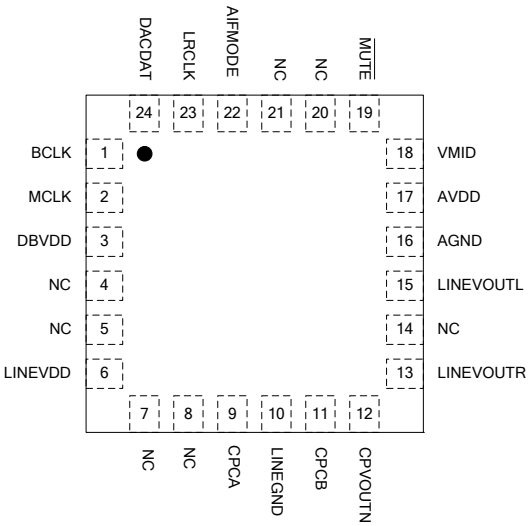
PIN CONFIGURATION



24-LEAD QFN (TOP VIEW)

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM1824CGEFL/V	−40°C to +85°C	24-lead QFN (pb-free)	MSL3	260°C
WM1824CGEFL/RV	−40°C to +85°C	24-lead QFN (pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 3,500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	BCLK	Digital In	Digital audio interface bit clock
2	MCLK	Digital In	Master clock
3	DBVDD	Supply	Digital Buffer Supply
4	NC		
5	NC		
6	LINEVDD	Supply	Charge Pump supply
7	NC		
8	NC		
9	CPCA	Analogue Out	Charge Pump fly back capacitor pin
10	LINEGND	Supply	Charge Pump ground
11	CPCB	Analogue Out	Charge Pump fly back capacitor pin
12	CPVOUTN	Analogue Out	Charge Pump negative rail decoupling pin
13	LINEVOUTR	Analogue Out	Right line output
14	NC		
15	LINEVOUTL	Analogue Out	Left line output
16	AGND	Supply	Analogue ground
17	AVDD	Supply	Analogue supply
18	VMID	Analogue Out	Analogue midrail decoupling pin
19	$\overline{\text{MUTE}}$	Digital In	0 = Mute enabled 1 = Mute disabled
20	NC		
21	NC		
22	AIFMODE	Digital In	1 = 24-bit Left Justified 0 = 24-bit I^2S
23	LRCLK	Digital In	Digital audio interface left/right clock
24	DACDAT	Digital In	Digital audio interface data input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
AVDD, LINEVDD, DBVDD	-0.3V	+4.5V
Voltage range digital inputs	LINEGND -0.3V	LINEVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Temperature range, T_A	-40°C	+125°C
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue grounds must always be within 0.3V of each other.
2. LINEVDD and AVDD must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue supply range	AVDD, LINEVDD		2.97	3.3	3.63	V
Ground	AGND, LINEGND			0		V
Digital Buffer supply range	DBVDD		1.62		3.63	V

ELECTRICAL CHARACTERISTICS

Test Conditions

LINEVDD=AVDD=DBVDD=3.3V, LINEGND=AGND=0V, T_A=+25°C, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Output Level		0dBFS	2.04	$\frac{2.1\times AVDD}{3.3}$	2.14	Vrms
Load Impedance			1[A]			kΩ
Load Capacitance		No external RC filter			300	pF
		With filter shown in Figure 15			1	µF
DAC Performance						
Signal to Noise Ratio	SNR	R_L = 10kΩ A-weighted		106		dB
		R_L = 10kΩ Un-weighted		104		dB
Dynamic Range	DNR	R_L = 10kΩ A-weighted		104		dB
Total Harmonic Distortion	THD	-1dBFS		-89		dB
		0dBFS		-86		dB
AVDD + LINEVDD Power Supply Rejection Ratio	PSRR	100Hz		54		dB
		1kHz		54		dB
		20kHz		50		dB
Channel Separation		1kHz		100		dB
		20Hz to 20kHz		95		dB
System Absolute Phase				0		degrees
Channel Level Matching				0.1		dB
Mute Attenuation				-120		dB
DC Offset at LINEVOUTL and LINEVOUTR			-1	0	1	mV
Digital Logic Levels						
Input HIGH Level	V_{IH}		0.7× LINEVDD			V
Input LOW Level	V_{IL}				0.3× LINEVDD	V
Input Capacitance				10		pF
Input Leakage			-0.9		0.9	µA

Note:

1. To prevent over-current protection shutdown of the device, ensure that the load impedance is never less than 100Ω. If a load impedance of less than 100Ω is presented to either LINEVOUTL or LINEVOUTR, the device may go into a protective shutdown state where the charge pump will stop running and the device will shut down. It will take a hardware reset to come out of this state (recycle the power supplies or hold /MUTE low for 1024 LRCLK cycles after the low impedance load condition has been removed).

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
4. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

POWER CONSUMPTION MEASUREMENTS

Test Conditions
LINEVDD=AVDD=DBVDD=3.3V, LINEGND=AGND=0V, T_A=+25°C, quiescent (no signal)

	TEST CONDITIONS	IAVDD (mA)	ILINEVDD (mA)	DBVDD (mA)	TOTAL (mA)
Off	No clocks applied	0.8	1.0	0.0	1.8
fs=48kHz, MCLK=256fs					
Standby	$\overline{\text{MUTE}}$ = 0	0.2	2.1	0.02	2.32
Playback	$\overline{\text{MUTE}}$ = 1	4.7	6.0	0.02	10.72
fs=96kHz, MCLK=256fs					
Standby	$\overline{\text{MUTE}}$ = 0	0.2	2.7	0.03	2.93
Playback	$\overline{\text{MUTE}}$ = 1	5.2	8.5	0.03	13.73
fs=192kHz, MCLK=128fs					
Standby	$\overline{\text{MUTE}}$ = 0	0.2	2.7	0.04	2.94
Playback	$\overline{\text{MUTE}}$ = 1	5.2	8.4	0.04	13.64

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

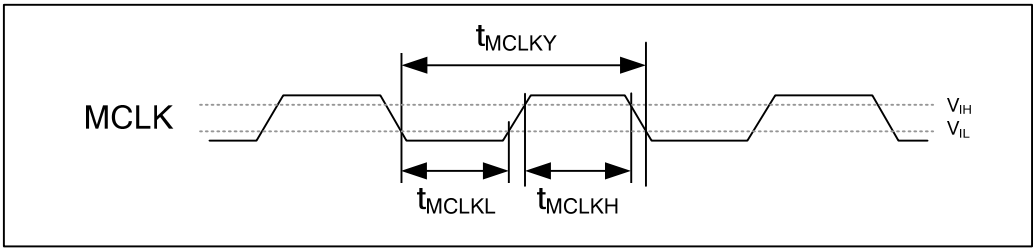


Figure 1 System Clock Timing Requirements

Test Conditions

LINEVDD=AVDD=DBVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Master Clock Timing Information					
MCLK cycle time	t_{MCLKY}	27		500	ns
MCLK high time	t_{MCLKH}	11			ns
MCLK low time	t_{MCLKL}	11			ns
MCLK duty cycle (t_{MCLKH}/t_{MCLKL})		40:60		60:40	%

AUDIO INTERFACE TIMING – SLAVE MODE

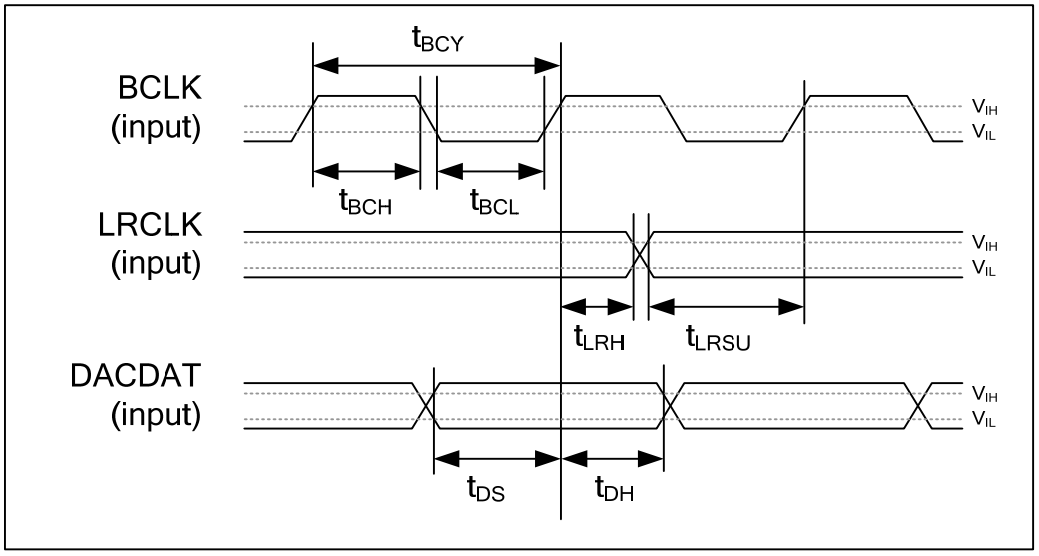


Figure 2 Digital Audio Data Timing – Slave Mode

Test Conditions

LINEVDD=AVDD=DBVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	27			ns
BCLK pulse width high	t_{BCH}	11			ns
BCLK pulse width low	t_{BCL}	11			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	7			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	5			ns
DACDAT hold time from LRCLK rising edge	t_{DH}	5			ns
DACDAT set-up time to BCLK rising edge	t_{DS}	7			ns

Table 1 Slave Mode Audio Interface Timing

Note:

BCLK period should always be greater than or equal to MCLK period.

POWER ON RESET CIRCUIT

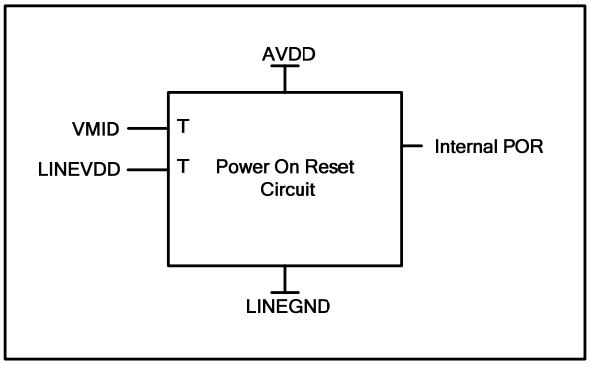


Figure 3 Internal Power on Reset Circuit Schematic

The WM1824 includes an internal Power-On-Reset circuit, as shown in Figure 3, which is used to reset the DAC digital logic into a default state after power up. The POR circuit is powered by AVDD and has as its inputs VMID and LINEVDD. It asserts POR low if VMID or LINEVDD are below a minimum threshold.

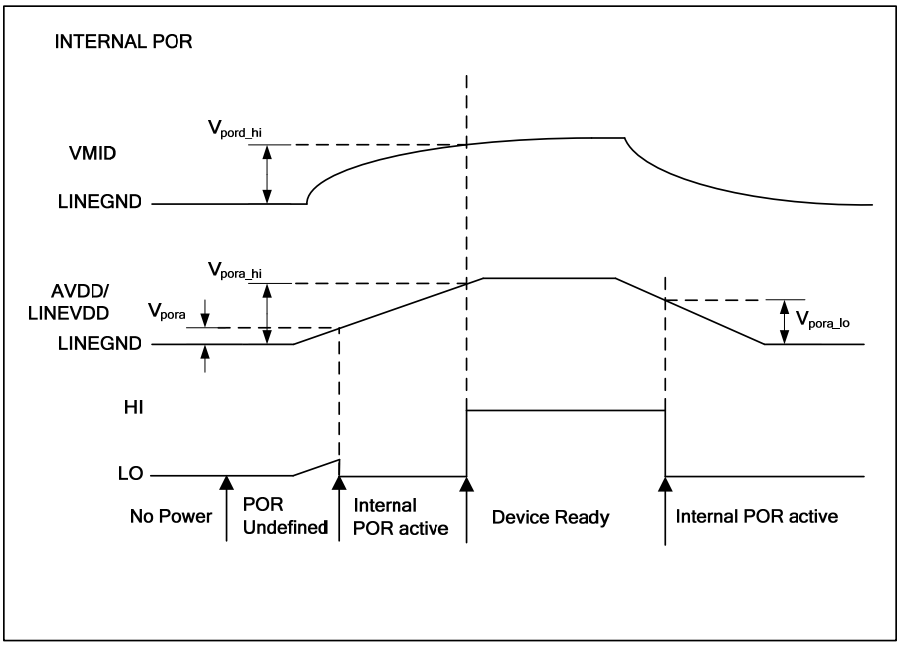


Figure 4 Typical Power Timing Requirements

Figure 4 shows a typical power-up sequence where LINEVDD comes up with AVDD. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee POR is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. After VMID rises to V_{pord_hi} and AVDD rises to $V_{pora_hi,}$ POR is released high and access to the control interface and audio interface may take place. This assumes that DBVDD is at a level within the recommended operating conditions.

On power down, PORB is asserted low whenever LINEVDD or AVDD drop below the minimum threshold V_{pora_low}.

Test Conditions

LINEVDD = AVDD = DBVDD = 3.3V AGND = LINEGND = 0V, T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
VDD level to POR defined (LINEVDD/AVDD rising)	V_{pora}	Measured from LINEGND		158		mV
VDD level to POR rising edge (VMID rising)	V_{pord_hi}	Measured from LINEGND	0.63	0.8	1	V
VDD level to POR rising edge (LINEVDD/AVDD rising)	V_{pora_hi}	Measured from LINEGND	1.44	1.8	2.18	V
VDD level to POR falling edge (LINEVDD/AVDD falling)	V_{pora_lo}	Measured from LINEGND	0.96	1.46	1.97	V

Table 2 Power on Reset

Note: All values are simulated results

DEVICE DESCRIPTION

INTRODUCTION

The WM1824 provides high fidelity, $2V_{rms}$ ground referenced stereo line output from a single supply line with minimal external components. The integrated DC servo eliminates the requirement for external mute circuitry by minimising DC transients at the output during power up/down. The device is well-suited to both stereo and multi-channel systems.

The device supports all common audio sampling rates between 8kHz and 192kHz using common MCLK fs rates, with a slave mode audio interface.

The WM1824 supports a simple hardware control mode, allowing access to 24-bit LJ and I^2S audio interface formats, as well as a mute control. An internal audio interface clock monitor automatically mutes the DAC output if the BCLK is interrupted.

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting audio data to the WM1824. The digital audio interface uses three pins:

- DACDAT: DAC data input
- LRCLK: Left/Right data alignment clock
- BCLK: Bit clock, for synchronisation

The WM1824 digital audio interface operates as a slave as shown in Figure 5.

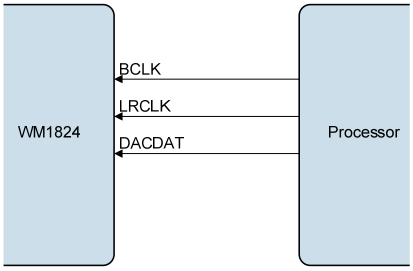


Figure 5 Slave Mode

INTERFACE FORMATS

The WM1824 supports two different audio data formats:

- Left justified
- I^2S

Both of these modes are MSB first. They are described in Audio Data Formats on page 13. Refer to the “Electrical Characteristics” section for timing information.

AUDIO DATA FORMATS

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

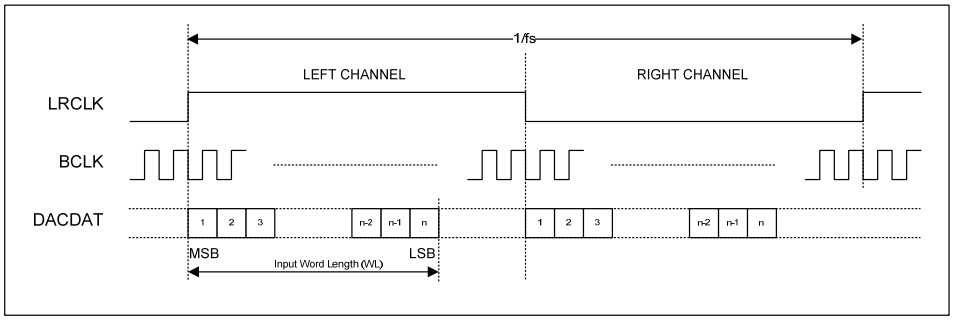


Figure 6 Left Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

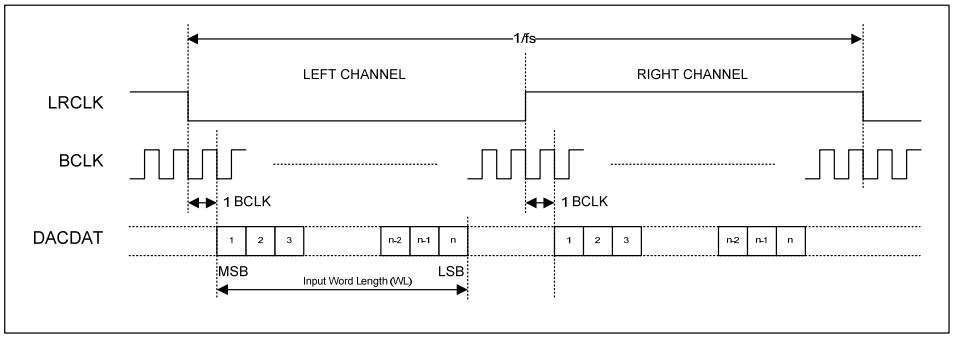


Figure 7 I^2S Justified Audio Interface (assuming n-bit word length)

DIGITAL AUDIO DATA SAMPLING RATES

The external master clock is applied directly to the MCLK input pin. In a system where there are a number of possible sources for the reference clock, it is recommended that the clock source with the lowest jitter be used for the master clock to optimise the performance of the WM1824.

The WM1824 has a detection circuit that automatically determines the relationship between the master clock frequency (MCLK) and the sampling rate (LRCLK), to within ±32 system clock periods. The MCLK must be synchronised with the LRCLK, although the device is tolerant of phase variations or jitter on the MCLK.

If during sample rate change the ratio between MCLK and LRCLK varies more than once within 1026 LRCLK periods, then it is recommended that the device be taken into the standby state or the off state before the sample rate change and held in standby until the sample rate change is complete. This will ensure correct operation of the detection circuit on the return to the enabled state. For details on the standby state, please refer to the Power up and down control section of the datasheet on page 15.

The DAC supports MCLK to LRCLK ratios of 128fs to 1152fs and sampling rates of 8kHz to 192kHz.

Table 3 shows typical master clock frequencies and sampling rates supported by the WM1824 DAC.

Sampling Rate LRCLK	MASTER CLOCK FREQUENCY (MHz)						
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs
8kHz	Unavailable	Unavailable	2.048	3.072	4.096	6.144	9.216
32kHz	Unavailable	Unavailable	8.192	12.288	16.384	24.576	36.864
44.1kHz	Unavailable	Unavailable	11.2896	16.9344	22.5792	33.8688	Unavailable
48kHz	Unavailable	Unavailable	12.288	18.432	24.576	36.864	Unavailable
88.2kHz	11.2896	16.9344	22.5792	33.8688	Unavailable	Unavailable	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable	Unavailable
176.4kHz	22.5792	33.8688	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable

Table 3 MCLK Frequencies and Audio Sample RatesHardware Control Interface

The device is configured according to logic levels applied to the hardware control pins as described in Table 4.

PIN NAME	PIN NUMBER	DESCRIPTION
$\overline{\text{MUTE}}$	19	**Mute Control** 0 = Mute 1 = Normal operation
AIFMODE	22	**Audio Interface Mode** 1 = 24-bit LJ 0 = 24-bit I^2S

Table 4 Hardware Control Pin Configuration

MUTE

The $\overline{\text{MUTE}}$ pin controls the DAC mute to both left and right channels. When the mute is asserted a softmute is applied to ramp the signal down in 800 samples. When the mute is de-asserted the signal returns to full scale in one step.

POWER UP AND DOWN CONTROL

The MCLK, BCLK and $\overline{\text{MUTE}}$ pins are monitored to control how the device powers up or down, and this is summarised in Figure 8 below.

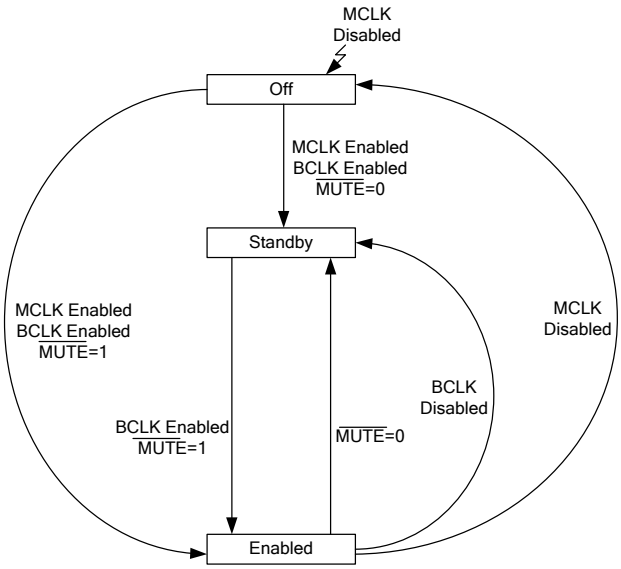


Figure 8 Hardware Power Sequence Diagram

Off to Enable

To power up the device to enabled, start MCLK and BCLK and set $\overline{\text{MUTE}}$ = 1.

Off to Standby

To power up the device to standby, start MCLK and BCLK and set $\overline{\text{MUTE}}$ = 0. Once the device is in standby mode, BCLK can be disabled and the device will remain in standby mode.

Standby to Enable

To transition from the standby state to the enabled state, set the $\overline{\text{MUTE}}$ pin to logic 1 and start BCLK.

Enable to Standby

To power down to a standby state leaving the charge pump running, either set the $\overline{\text{MUTE}}$ pin to logic 0 or stop BCLK. MCLK must continue to run in these situations. The device will automatically mute and power down quietly in either case.

Note: It is recommended that the device is placed in standby mode before sample rate change if the sample rate changes more than once in 1026 LRCLK periods, as detailed in Digital Audio Data Sampling Rates on page 13.

Enable to Off

To power down the device completely, stop MCLK at any time. It is recommended that the device is placed into standby mode as described above before stopping MCLK to allow a quiet shutdown.

For the timing of the off state to enabled state transition (power on to audio out timing), and the enabled state to standby state transition (the shutdown timing), please refer to WTN0302.

POWER DOMAINS

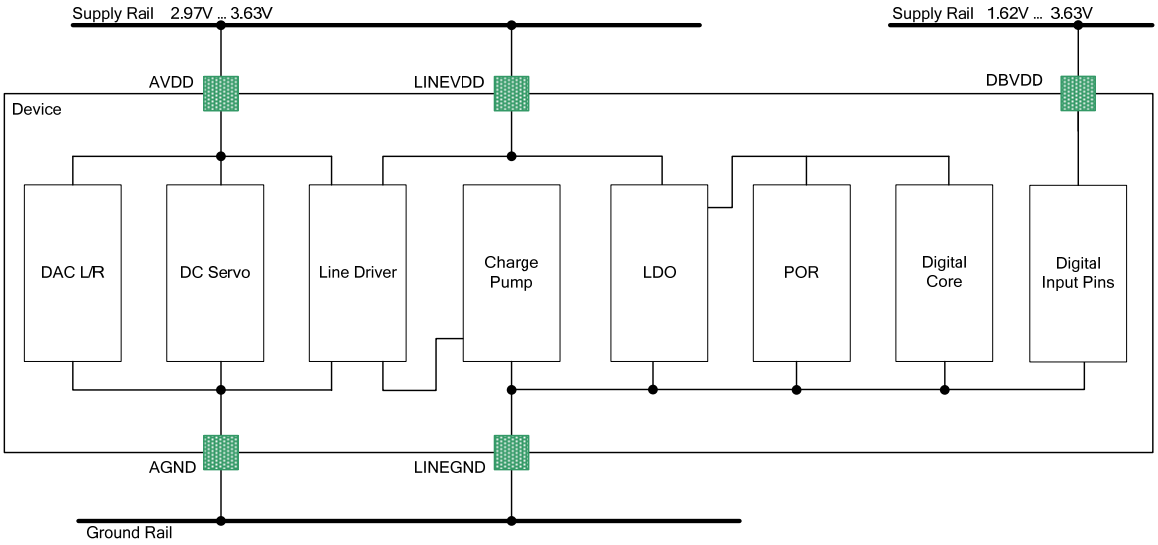


Figure 9 Power Domain Diagram

Power Domain	Name	Blocks Using This Domain	Domain Description
DAC Power Supplies			
3.3V ± 10%	AVDD	Line Driver DAC DC Servo	Analogue Supply
3.3V ± 10%	LINEVDD	Charge Pump Digital LDO Digital Pad buffers	Analogue Supply
1.8V – 3.3V ± 10%	DBVDD	Digital Input Pins	Digital Buffer Supply
Internally Generated Power Supplies and References			
1.65V ± 10%	VMID	DAC, LDO	Ext decoupled resistor string
-3.3V ± 10%	CPVOUTN	Line Driver	Charge pump generated voltage

Table 5 Power Domains

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Filter – 256fs to 1152fs					
Passband	± 0.1dB			0.454fs	
Passband Ripple				0.1	dB
Stopband		0.546fs			
Stopband attenuation	f > 0.546fs	-50			dB
Group Delay			10		Fs
DAC Filter – 128fs and 192fs					
Passband	± 0.1dB			0.247fs	
Passband Ripple				0.1	dB
Stopband		0.753fs			
Stopband attenuation	f > 0.753fs	-50			dB
Group Delay			10		Fs

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

DAC FILTER RESPONSES

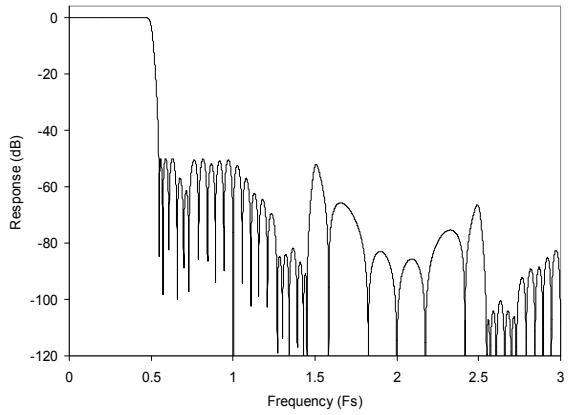


Figure 10 DAC Digital Filter Frequency Response – 256fs to 1152fs Clock Modes

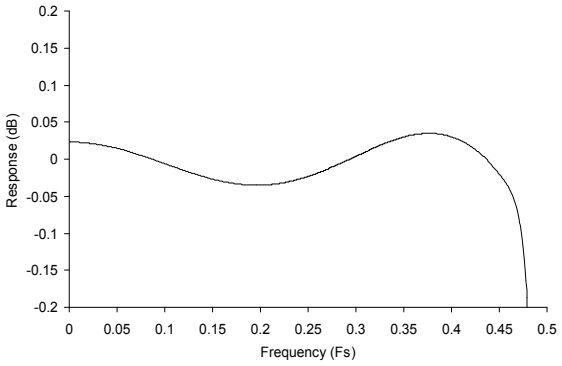


Figure 11 DAC Digital Filter Ripple – 256fs to 1152fs Clock Modes

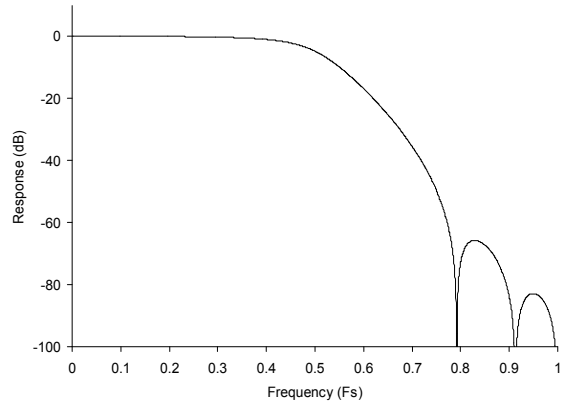


Figure 12 DAC Digital Filter Frequency Response – 128fs and 192fs Clock Modes

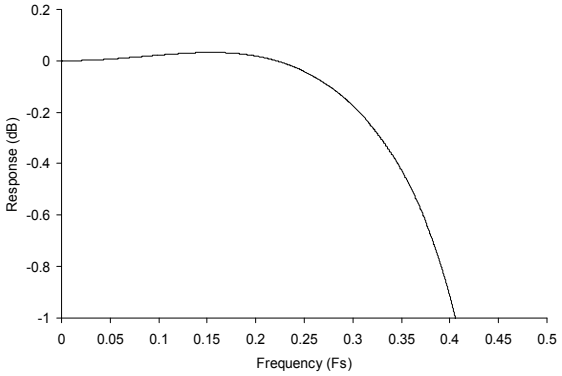


Figure 13 DAC Digital Filter Ripple – 128fs to 192fs Clock Modes

APPLICATIONS INFORMATION

RECOMMENDED EXTERNAL COMPONENTS

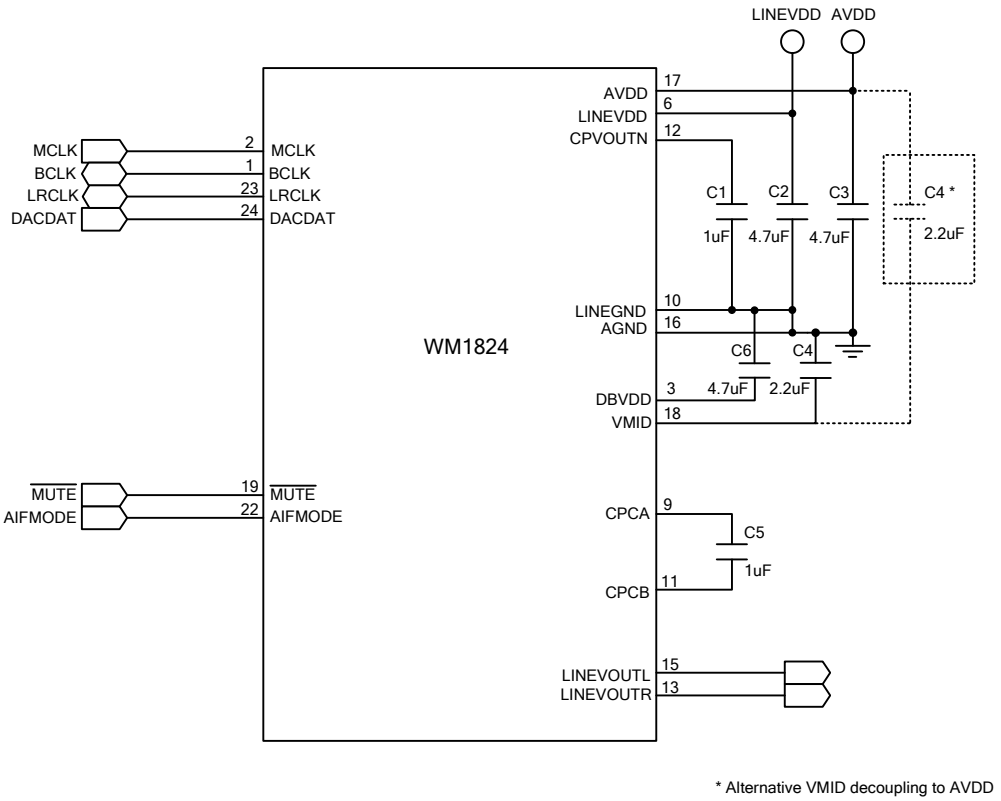


Figure 14 Recommended External Components

Notes:

1. Wolfson recommend using a single, common ground plane. Where this is not possible, care should be taken to optimise split ground configuration for audio performance.
2. Charge Pump fly-back capacitor C5 should be placed as close to WM1824 as possible, followed by Charge Pump decoupling capacitor C1, then LINEVDD and VMID decoupling capacitors.
3. Capacitor types should be chosen carefully. Capacitors with very low ESR are recommended for optimum performance.

RECOMMENDED ANALOGUE LOW PASS FILTER

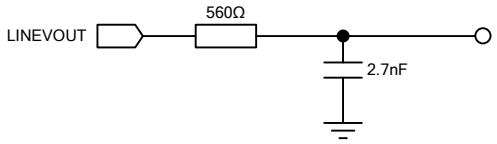


Figure 15 Recommended Analogue Low Pass Filter (one channel shown)

An external single-pole RC filter is recommended if the device is driving a wideband amplifier. Other filter architectures may provide equally good results.

The filter shown in Figure 15 has a -3dB cut-off at 105.26kHz and a droop of 0.15dB at 20kHz. The typical output from the WM1824 is 2.1Vrms – when a 10kΩ load is placed at the output of this recommended filter the amplitude across this load is 1.99Vrms.

RELEVANT APPLICATION NOTES

The following application notes may provide additional guidance for use of the WM1824.

DEVICE PERFORMANCE:

WAN0129 – Decoupling and Layout Methodology for Wolfson DACs, ADCs and CODECs

WAN0144 – Using Wolfson Audio DACs and CODECs with Noisy Supplies

GENERAL:

WAN0108 – Moisture Sensitivity Classification and Plastic IC Packaging

WAN0109 – ESD Damage in Integrated Circuits: Causes and Prevention

WAN0158 – Lead-Free Solder Profiles for Lead-Free Components

WAN0161 – Electronic End-Product Design for ESD

If you require more information or require technical support, please contact the nearest Wolfson Microelectronics regional office:

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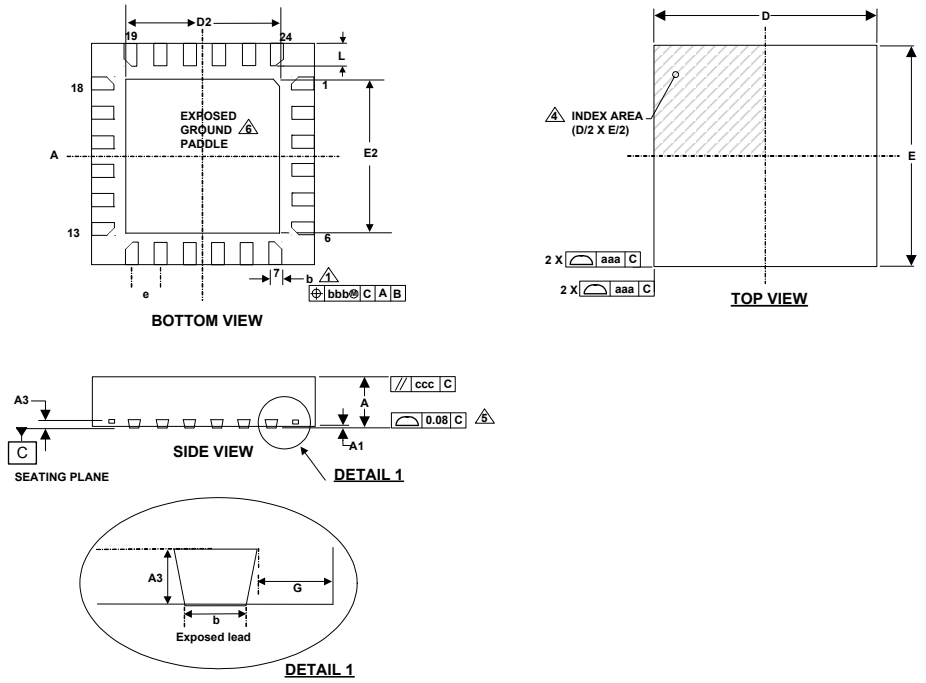
PACKAGE DIMENSIONS

FL: 24 PIN QFN PLASTIC PACKAGE 4 x 4 x 0.75 mm BODY, 0.50 mm LEAD PITCH **DM070.A**



Symbols				
	MIN	**NOM**	**MAX**	**NOTE**
A	0.70	0.75	0.80	
A1	0	0.35	0.05	
A3		0.203 REF		
b	0.20	0.25	0.30	1
D		4.00 BSC		
D2	2.4	2.50	2.6	2
E		4.00 BSC		
E2	2.4	2.50	2.6	2
e		0.50 BSC		
G		0.65		
L	0.35	0.40	0.45	
Tolerances of Form and Position				
aaa		0.1		
bbb		0.1		
ccc		0.1		
REF:		JEDEC, MO-220		

NOTES:
1. **DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.2 mm AND 0.30 mm FROM TERMINAL TIP.**
2. **FALLS WITHIN JEDEC, MO-220.**
3. **ALL DIMENSIONS ARE IN MILLIMETRES.**
4. **THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-002.**
5. **COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.**
6. **REFER TO APPLICATIONS NOTE WAN_0118 FOR FURTHER INFORMATION REGARDING PCB FOOTPRINTS AND QFN PACKAGE SOLDERING.**
7. **THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.**

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REVISION HISTORY

DATE	REV	ORIGINATOR	CHANGES	PAGE
24/03/10	3.1/ 4.0	BT	Removed MCLK Jitter Spec in System Clock Timing table, page 8	
		BT	Removed maximum line load from electrical characteristics	
		BT	Updated power state diagram to show all transitions, page 15	
		BT	Added note in Power up and down control section to recommend putting the device in standby mode if more than 1 sample rate change occurs in 1026 LRCLK cycles, page 15	
		BT	Added reference to WTN0302 in Power up and down control section, page 15	
		BT	Added paragraph in Digital Audio Data Sampling Rates section to recommend putting the device in standby or off mode if more than 1 sample rate change occurs in 1026 LRCLK cycles, page 13	
		BT	Changed RC value of recommended output filter	20
		BT	Added 100Ω minimum load impedance to prevent over-current shutdown note to electrical characteristics table	6
24/11/10	4.0	JMacD	Updated to Production Data status	
05/12/12	4.1	JMacD	Order codes changed from WM1824GEFL/R and WM1824GEFL/RV to WM1824**C**GEFL/R and WM1824**C**GEFL/RV to reflect change to copper wire bonding.	3
15/12/12	4.1	JMacD	Relevant Application Note section updated	20