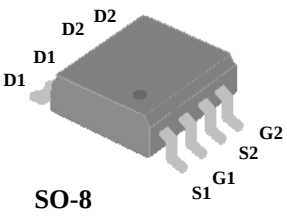
AP4500GM-HF

Halogen-Free Product

Advanced Power Electronics Corp.

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **Simple Drive Requirement**
- ▼ **Low Gate Charge**
- ▼ **Fast Switching Performance**
- ▼ **RoHS Compliant & Halogen-Free**



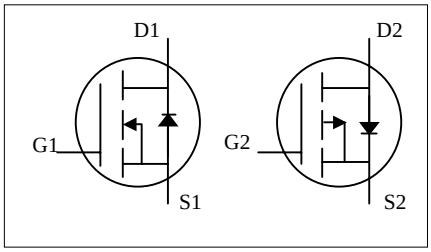
SO-8

N-CH	BV_{DSS}	20V
	$R_{DS(ON)}$	30mΩ
	I_D	6A
P-CH	BV_{DSS}	-20V
	$R_{DS(ON)}$	50mΩ
	I_D	-5A

Description

Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is widely preferred for commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-channel	P-channel	
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	±12	±12	V
I_D@T_A=25℃	Continuous Drain Current[3]	6	-5	A
I_D@T_A=70℃	Continuous Drain Current[3]	4.8	-4	A
I_{DM}	Pulsed Drain Current[1]	20	-20	A
P_D@T_A=25℃	Total Power Dissipation	2.0		W
	Linear Derating Factor	0.016		W/℃
T_{STG}	Storage Temperature Range	-55 to 150		℃
T_J	Operating Junction Temperature Range	-55 to 150		℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	62.5	℃/W

N-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	20	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=4.5V, I_D=6A	-	-	30	mΩ
		V_{GS}=2.5V, I_D=5.2A	-	-	45	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250uA	0.5	-	1.2	V
g_{fs}	Forward Transconductance	V_{DS}=10V, I_D=6A	-	6	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=20V, V_{GS}=0V	-	-	1	uA
	Drain-Source Leakage Current (T_j=70°C)	V_{DS}=20V ,V_{GS}=0V	-	-	25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=6A	-	10	15	nC
Q_{gs}	Gate-Source Charge	V_{DS}=16V	-	1.1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=4.5V	-	4.1	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=10V	-	7	-	ns
t_r	Rise Time	I_D=1A	-	10	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=5V	-	21	-	ns
t_f	Fall Time	R_D=10Ω	-	5	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	570	910	pF
C_{oss}	Output Capacitance	V_{DS}=20V	-	90	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	85	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=1.7A, V_{GS}=0V	-	-	1.2	V
t_{rr}	Reverse Recovery Time[2]	I_S=6A, V_{GS}=0V,	-	21	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	14	-	nC

P-CH Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-20	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-4.5V, I_D=-2.2A	-	-	50	mΩ
		V_{GS}=-2.5V, I_D=-1.8A	-	-	90	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.5	-	-1	V
g_{fs}	Forward Transconductance	V_{DS}=-10V, I_D=-2.2A	-	2.2	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-20V, V_{GS}=0V	-	-	-1	uA
	Drain-Source Leakage Current (T_j=70°C)	V_{DS}=-16V, V_{GS}=0V	-	-	-25	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±12V, V_{DS}=0V	-	-	±100	nA
Q_g	Total Gate Charge[2]	I_D=-5A	-	13	20	nC
Q_{gs}	Gate-Source Charge	V_{DS}=-16V	-	1.5	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	V_{GS}=-4.5V	-	4.5	-	nC
$t_{d(on)}$	Turn-on Delay Time[2]	V_{DS}=-10V	-	8	-	ns
t_r	Rise Time	I_D=-1A	-	17	-	ns
$t_{d(off)}$	Turn-off Delay Time	R_G=3.3Ω,V_{GS}=-5V	-	24	-	ns
t_f	Fall Time	R_D=10Ω	-	36	-	ns
C_{iss}	Input Capacitance	V_{GS}=0V	-	920	1500	pF
C_{oss}	Output Capacitance	V_{DS}=-20V	-	90	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	85	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	30
V_{SD}	Forward On Voltage[2]	I_S=-1.8A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time[2]	I_S=-5A, V_{GS}=0V,	-	28	-	ns
Q_{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	16	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board ; 135 ℃/W when mounted on Min. copper pad.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.
USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.
APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.
APEC RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN.

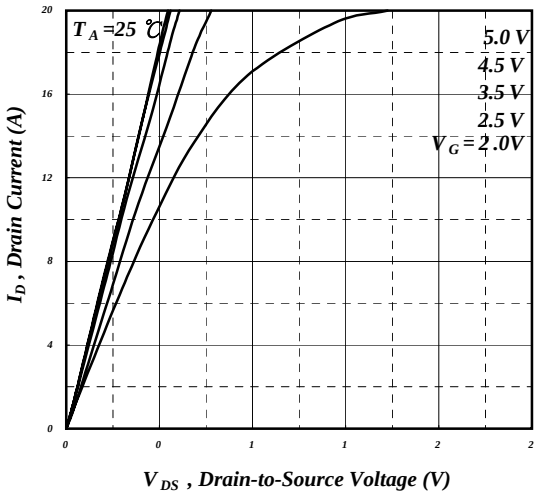


Fig 1. Typical Output Characteristics

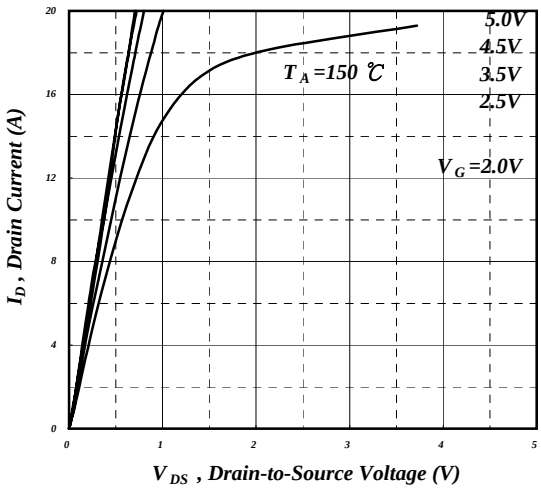


Fig 2. Typical Output Characteristics

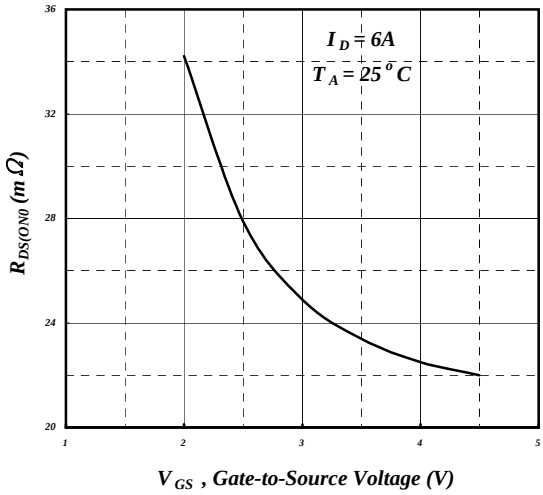


Fig 3. On-Resistance v.s. Gate Voltage

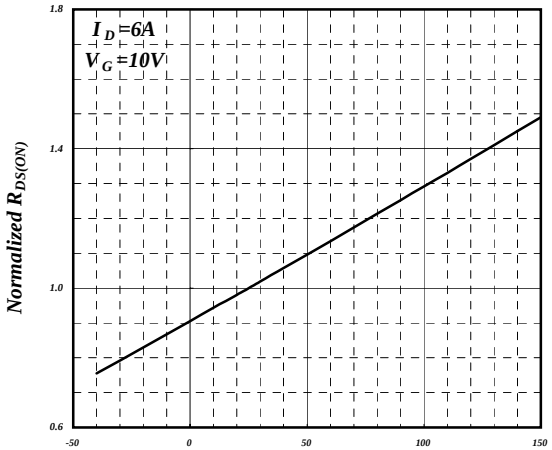


Fig 4. Normalized On-Resistance v.s. Junction Temperature

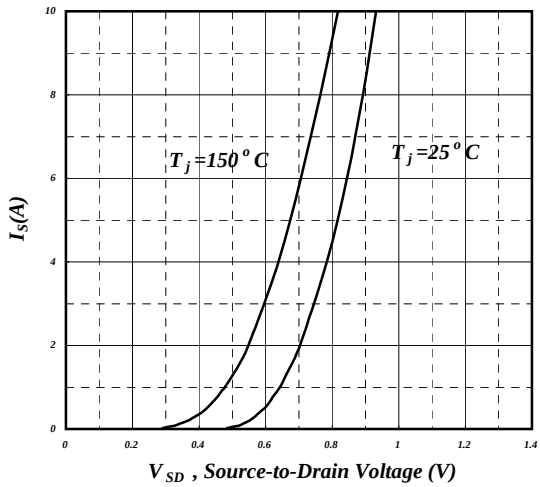


Fig 5. Forward Characteristic of Reverse Diode

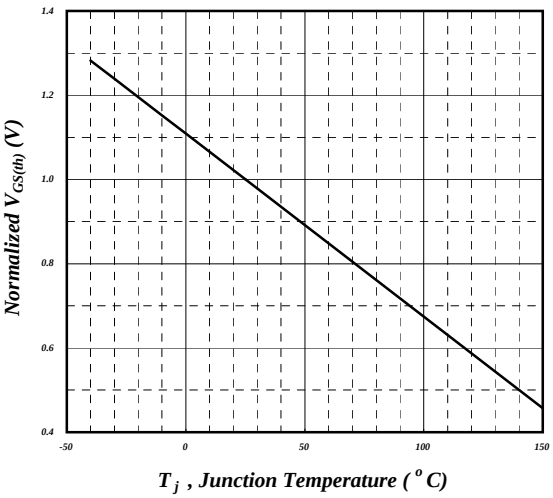


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

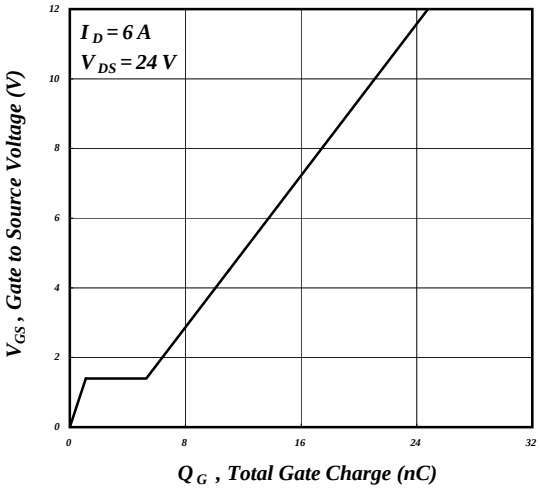


Fig 7. Gate Charge Characteristics

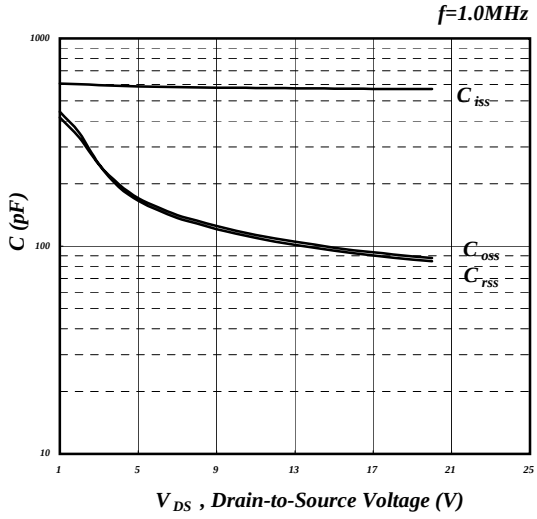


Fig 8. Typical Capacitance Characteristics

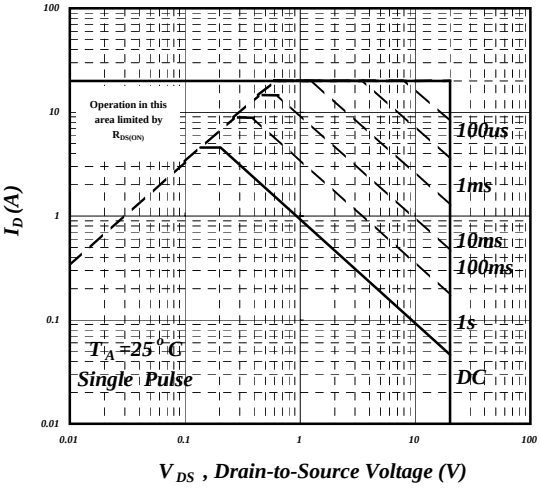


Fig 9. Maximum Safe Operating Area

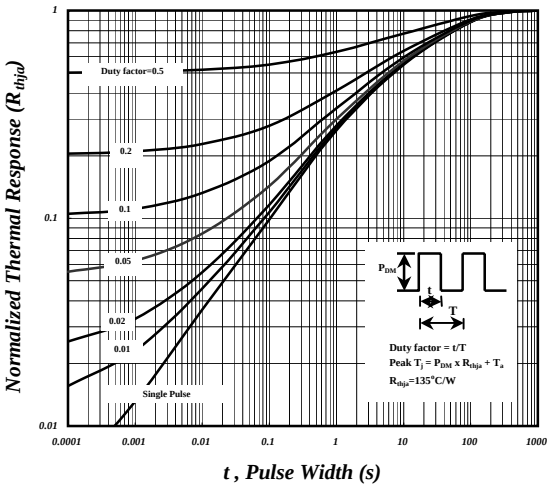


Fig 10. Effective Transient Thermal Impedance

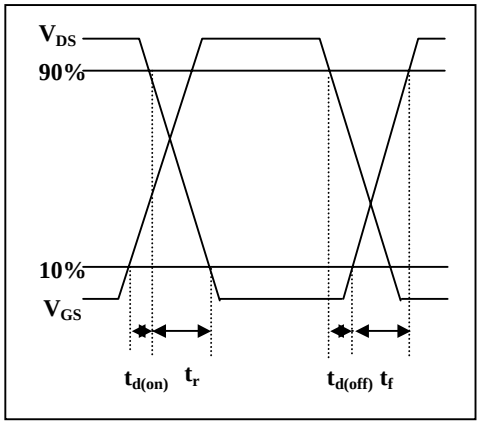


Fig 11. Switching Time Waveform

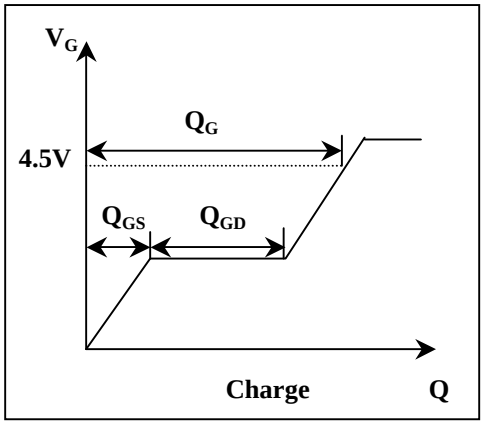


Fig 12. Gate Charge Waveform

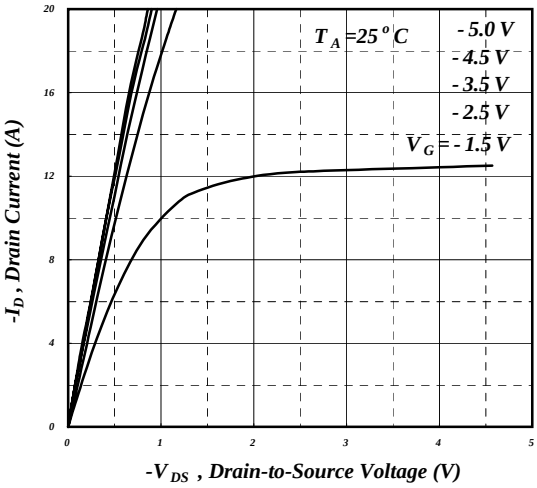


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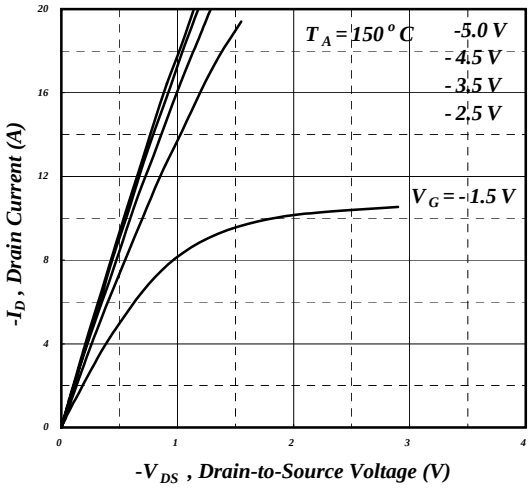


Fig 2. Typical Output Characteristics

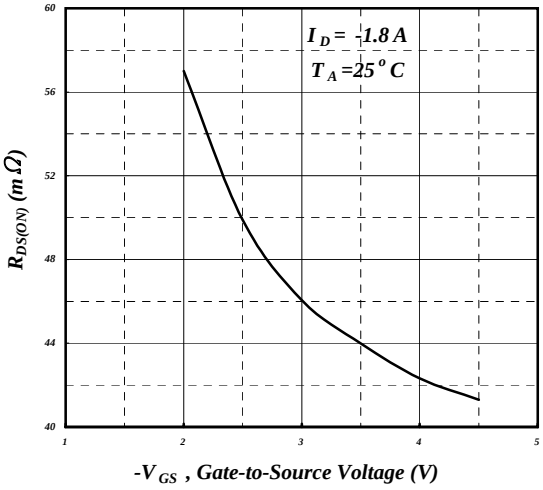


Fig 3. On-Resistance v.s. Gate Voltage

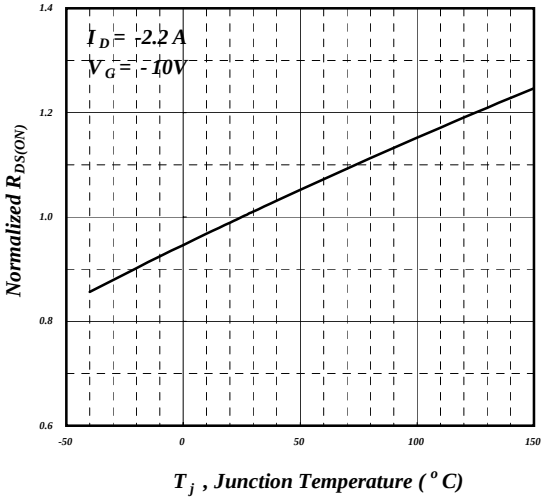


Fig 4. Normalized On-Resistance v.s. Junction Temperature

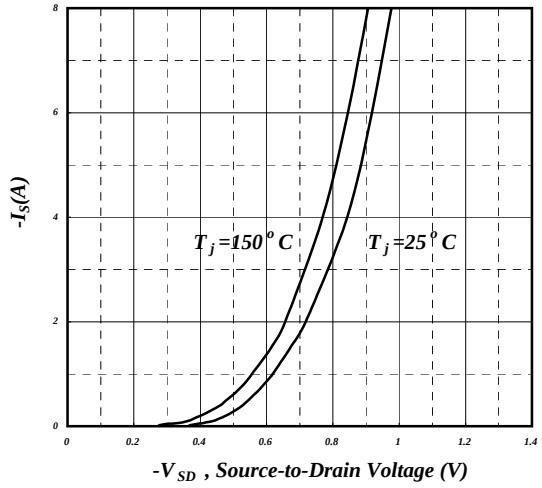


Fig 5. Forward Characteristic of Reverse Diode

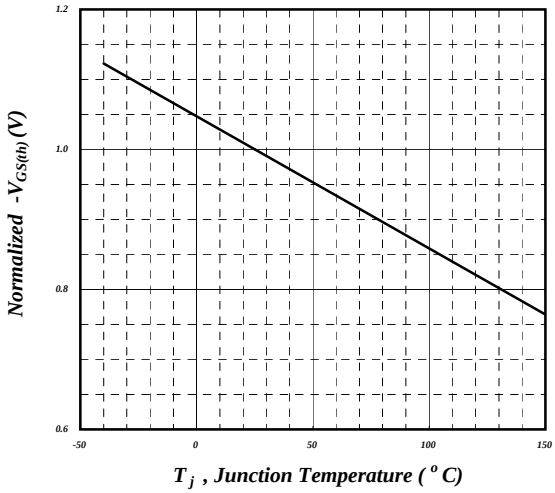


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

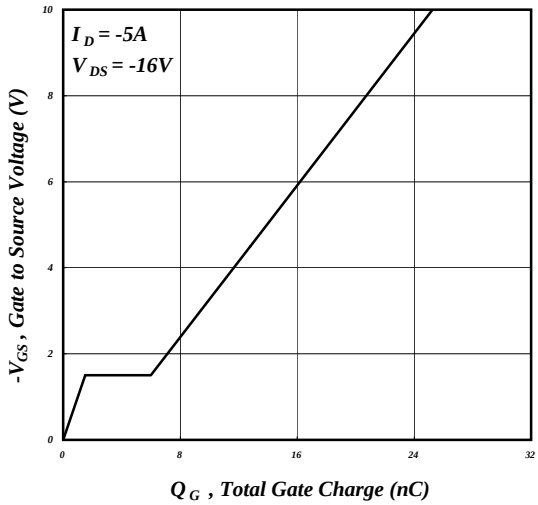


Fig 7. Gate Charge Characteristics

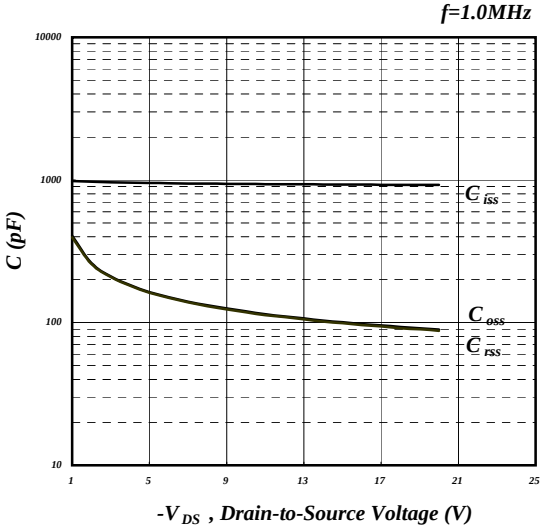


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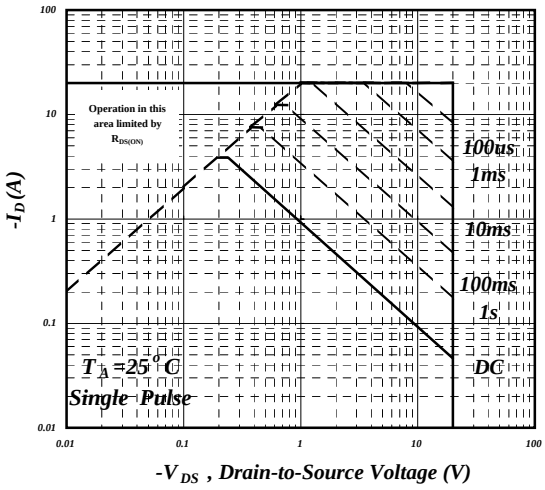


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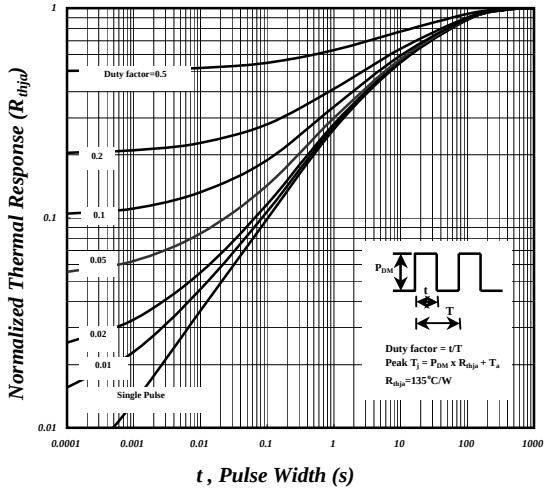


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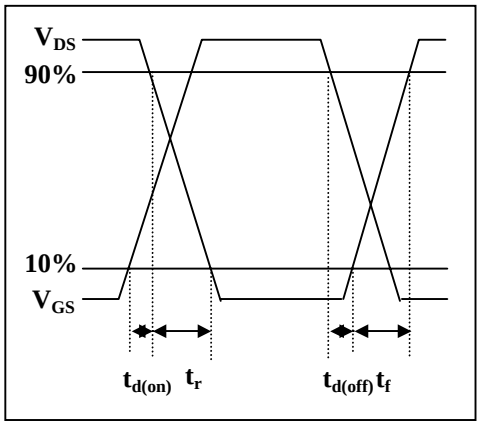


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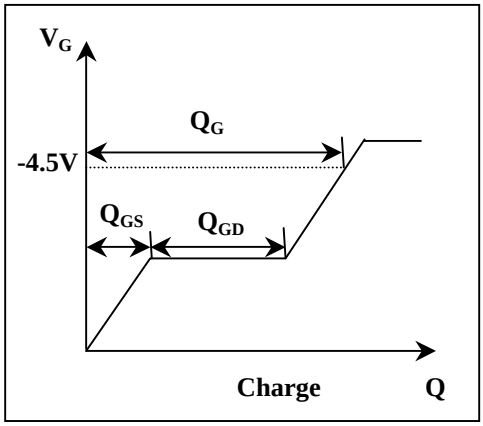


Fig 12. Gate Charge Waveform