SAMSUNG ELECTRONICS

VID - 97 - D001

JAN. 1998

SPECIFICATION

for KS5520

SYSTEM LSI BUSINESS

SAMSUNG ELECTRONICS CO.

SAMSUNG ELECTRONICS

SPECIFICATION
for KS5520

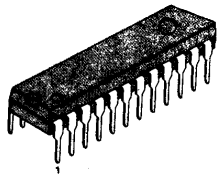
Important Notice

CONTENTS

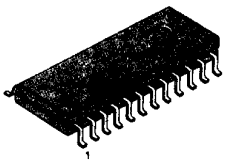
1. OUTLINE OF PRODUCT

The KS5520 is a single chip VLSI device which performs the on screen display function with sync seperation of video composite signal and AFC is proposed.
It can choose total 256 characters and display up to 360 characters in a screen.
It can also select various built-in functions such as character color select, inverse, etc. These functions are compatible with all video systems including NTSC, PAL, SECAM.

24 - SDIP - 300



24 - SOP - 375



2. FUNCTIONS

- On screen display
- Sync separator and sync detector
- AFC

3. FEATURES

- Screen structure : 360 (30 columns × 12 rows)
- Character structure : 12 × 18 dots
- Character types : 256 kinds of color characters
- Display position : 62 horizontal position
  64 vertical position
- Character size : 4 × 4 times of normal in both vertical and horizontal directions
- Blinking : controllable in character unit, blinking time also controllable
- Blanking : controllable in line units, blanking mode change possible
  Blank color fill possible in character units (8 colors)
- Background coloring : 8 colors
- Character coloring : coloring of characters possible in blank mode
- Inverse character display : controllable in character units
- Synchronous ways : automatic selection of internal or external synchronization via MICOM control
- Built-in clamp, horizontal/vertical sync separator & sync detector circuit
- Sync detection sensitivity can be adjusted via MICOM control.
- Built-in analog horizontal/vertical sync PLL circuit
- Scroll & Box Drawing ability
- Half-Tone function ability
- NTSC / PAL / SECAM mode via MICOM control

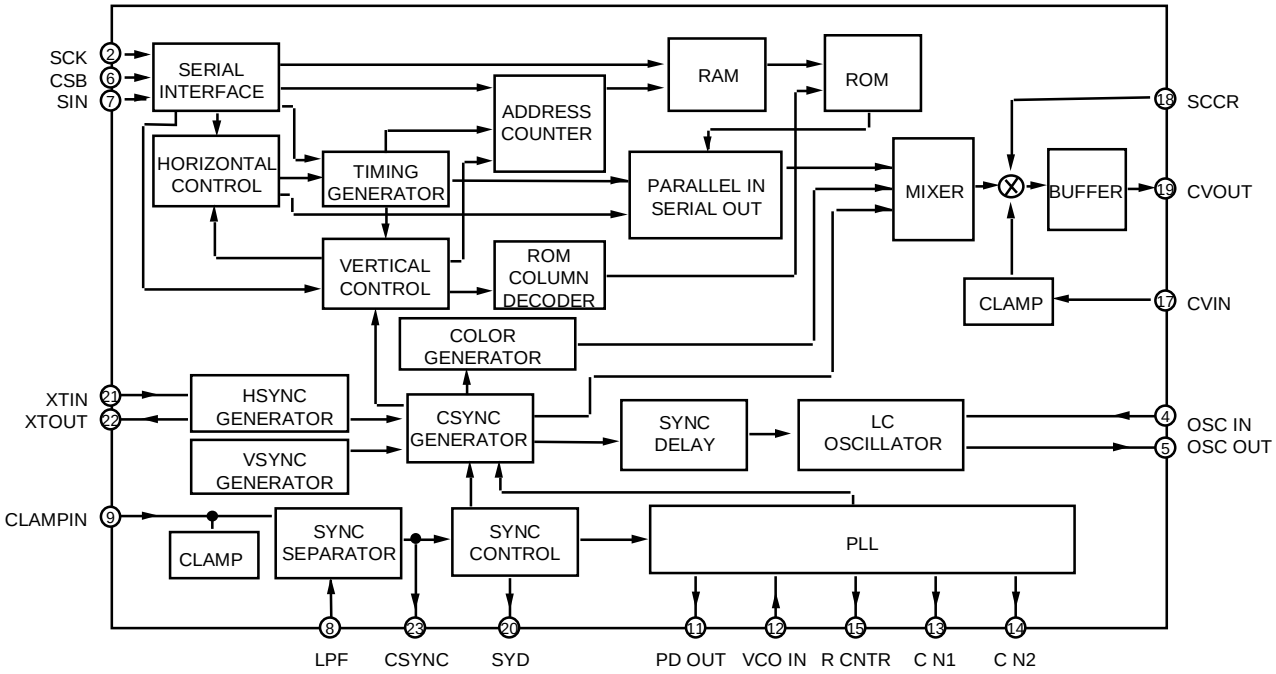
4.2 ORDERING INFORMATION

Device	Package	Operating Temprature
KS5520-XX	24-SDIP-300	- 20 ~ + 70℃
KS5520D-XX	24-SOP-375	- 20 ~ + 70℃

4.1 OPTION CODE

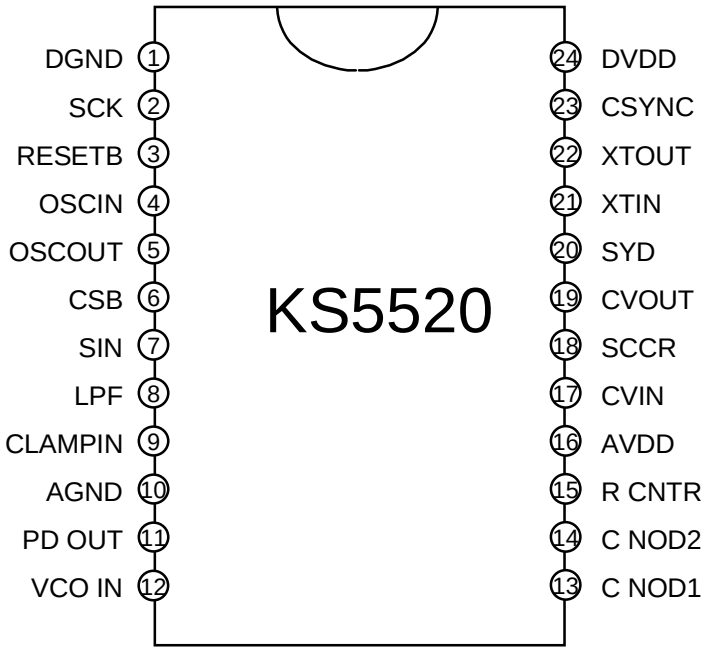
Code No.	Remark
KS5520-01	English, Russian, German, French, Spanish, Italian, Polish, Portuguese, Swedish Denish, Dutch, Esperanto, Vietnamese, Indonesian, Czechoslovak
KS5520D-04	English, Russian, German, French, Spanish, Italian, Polish, Portuguese, Swedish Denish, Dutch, Esperanto, Vietnamese, Indonesian, Czechoslovak, Greek

5. BLOCK DIAGRAM



6. PIN CONFIGURATION & DESCRIPTION

6.1 PIN CONFIGURATION



6.2 PIN DESCRIPTION

Pin No.	Symbol	I/O	Function
1	DGND	-	Digital Ground
2	SCK	I	Serial clock input. When CSB pin is low, then 16-bit serial data is inputted by controlling micom. Built-in pull-up resistor.
3	RESETB	I	Auto clear pin. If low, then all circuit is reset. Built-in pull-up resistor.
4	OSCIN	I	LC oscillation pin. Standard frequency is 9MHz & the horizontal start position and the horizontal size are controlled by the clock of oscillation block.
5	OSCOUT	O	
6	CSB	I	While pin 6 is low, serial data input is active. Built - in pull-up resistor
7	SIN	I	Serial data input pin. Built-in pull-up resistor
8	LPF	I	LPF gets rid of the color signal in a video input signal.
9	CLAMPIN	I	Clamp input pin of composite video signal of 2Vpp
10	AGND	-	Analog ground
11	PD OUT	O	Phase detect output of analog PLL. Loop filter is formed by PD OUT and VCO IN.
12	VCO IN	I	VCO input pin of PLL
13	C NOD1	O	Capacitor node 1 of PLL VCO
14	C NOD2	O	Capacitor node 2 of PLL VCO
15	R CNTR	O	Resistor node of PLL VCO
16	AVDD	-	5V Analog V_{DD}
17	CVIN	I	Composite video input pin
18	SCCR	I	When SECAM mode, color signal is mixed in the character level.
19	CVOUT	O	Composite video output pin

6.2 PIN DESCRIPTION (Continued)

Pin No.	Symbol	I/O	Function
20	SYD	O	H-sync detect output pin. If sync exists, then high if not, low
21	XTIN	I	X-tal input / output pin
22	XTOUT	O	NTSC : 14.31818 MHz, PAL : 17.734475MHz
23	CSYNC	O	When external, C-sync separator output is out, when internal, then internal C-sync is outputted.
24	DVDD	-	5V Digital V_{DD}

7. ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

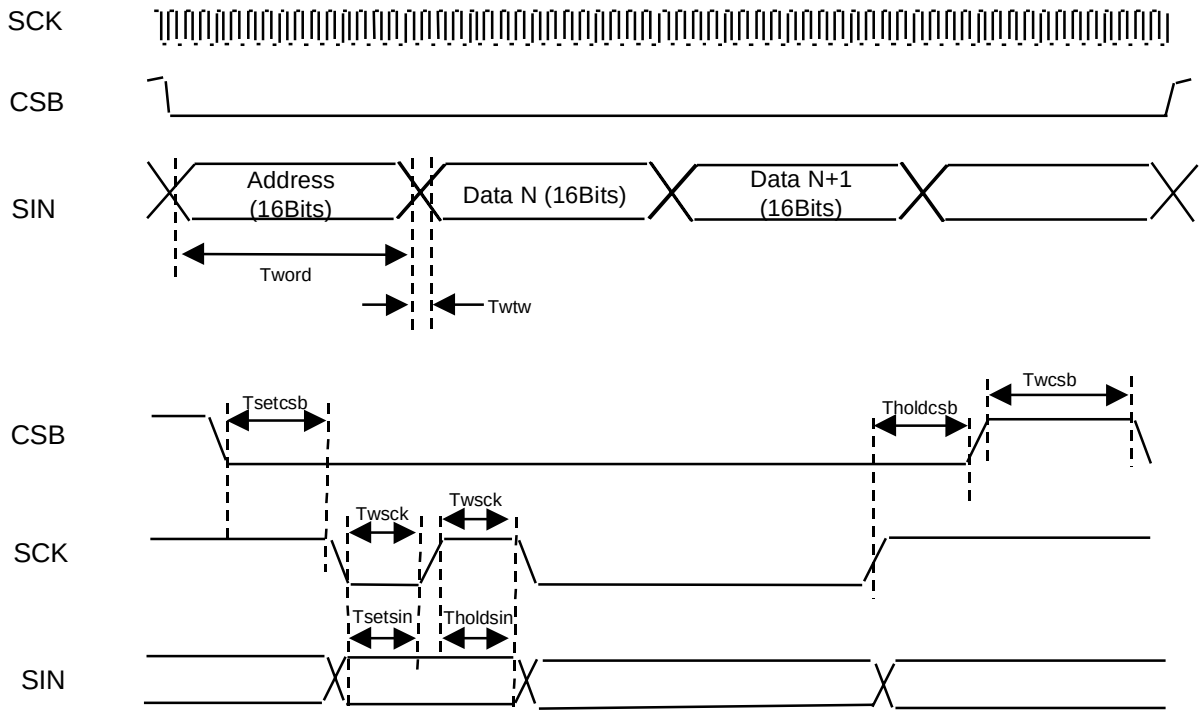
Characteristics	Symbol	Value	Unit
Supply Voltage	V_{DD}	3.0 ~ 7.0	V
Input Voltage	V_{IN}	V_{SS} - 0.3 ≤ V_{IN} ≤ V_{DD} + 0.3	V
Power Dissipation	P_D	200	mW
Operating Temperature	Topr	- 20 ~ + 70	℃
Storage Temperature	Tstg	- 40 ~ + 125	℃

8. ELECTRICAL CHARACTERISTICS (Ta = 25℃, AVDD = DVDD = 5V)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Voltage	VDD	4.75	5.00	5.25	V
Operating Current	Icc	20	40	60	mA
Input High Voltage	VIH	0.8VDD	-	-	V
Input Low Voltage	VIL	-	-	0.2VDD	V
Output High Voltage (2㎃ drive)	VOH	0.7VDD	-	-	V
Output Low Voltage (2㎃ drive)	VOL	-	-	0.3VDD	V
Pin8 LPF Voltage	Vp8	2.15	2.35	2.55	V
Pin9 Clamp Voltage	Vp9	1.25	1.45	1.65	V
Pin15 R_CNTR Voltage	Vp15	2.35	2.50	2.65	V
Pin17 Clamp Voltage	Vp17	0.60	0.80	1.00	V
Buffer Gain	Vp19G	1.80	2.00	2.20	V
LC Oscillation Frequency	Fosc	8.0	9.0	10.0	MHz
Hsync Duty	Fh_duty	250	550	850	nS
Hsync Frequency	H_fre	15.5	15.7	15.9	KHz
X-tal Oscillation Frequency	Fp22	14.1	14.3	14.5	MHz
Sync Separation Voltage	Vse	0.10	0.25	0.40	V
Blueback Sync Tip Level	Vbst	0.50	0.80	1.10	V
Blueback Pedestal Level	Vbpd	1.10	1.40	1.70	V
Blueback Color Burst Level High	Vcbh	1.40	1.70	2.00	V
Blueback Color Burst Level Low	Vcbl	0.80	1.10	1.40	V
Blueback Color Level High	Vbch	2.30	2.60	2.90	V
Blueback Color Level Low	Vbcl	1.30	1.60	1.90	V
Blueback Blank Level High	Vblkh	1.40	1.70	2.00	V
Blueback Blank Level Low	Vblk1	1.10	1.40	1.70	V
Blueback Character Level High	Vchh	2.40	2.70	3.00	V
Blank Color Off Level	Vbcof	1.10	1.40	1.70	V
Box White Level	Vbwl	2.20	2.50	2.80	V
Box Black Level	Vbbl	1.10	1.40	1.70	V
HalfTone Level	Vhalf	1.80	2.10	2.40	V
VCO Input Voltage	Vvco	2.30	2.50	2.70	V
AFC Freerun Frequency	Ffr	15.5	15.7	15.9	KHz
AFC Lock Range High	Falh	200	300	400	Hz
AFC Lock Range Low	Fall	-	-	-500	Hz

Note 1 : Specifications are subject to change without notice.

9. TIMING DIAGRAM



ITEM	SYMBOL	LIMITS			UNIT
		MIN	TYP	MAX	
SCK Width	Twsck	200	-	-	nsec
CSB Width	Twcsb	1	-	-	usec
CSB Setup Time	Tsetcsb	200	-	-	nsec
CSB Hold Time	Tholdcsb	2	-	-	usec
SIN Setup Time	Tsetsin	200	-	-	nsec
SIN Hold Time	Tholdsin	200	-	-	nsec
1 Word Write Time	Tword	10	-	-	usec
Word To Word Time	Twtw	1	-	-	usec

10. MEMORY STRUCTURE

It consists of 360*16 bits SRAM, 256 font ROM and 5 mode control register.

	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	Box_ Inv	Box 1	Box 0	R	G	B	Invert	Blink	C7	C6	C5	C4	C3	C2	C1	C0
1 2 3 . . . . . 357 358	* (Note)	* (Note)		* (Note)			* (Note)	* (Note)	Character Code (ROM Address)							
359	Box_ Inv	Box 1	Box 0	R	G	B	Invert	Blink	C7	C6	C5	C4	C3	C2	C1	C0
360	0	0	Half_ Tone	Blink 1	Blink 0	Blink_ Time	HZ 21	HZ 20	HZ 11	HZ 10	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
361	0	Ext_ fsc	Blank_ Level	Scroll_ Time	Scroll_ On	Inter -nal	VZ 21	VZ 20	VZ 11	VZ 10	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
362	0	RAM_ Erase	Disp_ On	P626/ P628	Inlace /Non-	Secam	NTSC/ PAL	Blk 1	Blk 0	Blk Col	C_ Level	R_ Lev1	R_ Lev0	R_ Cntr2	R_ Cntr1	R_ Cntr0
363	0	0	0	All_ Blank	DSP B	DSP A	DSP 9	DSP 8	DSP 7	DSP 6	DSP 5	DSP 4	DSP 3	DSP 2	DSP 1	DSP 0
364	0	Fll2	Fll1	Fll0	Flh3	Flh2	Flh1	Flh0	Fcl3	Fcl2	Fcl1	Fcl0	Fch3	Fch2	Fch1	Fch0

* (Note) : same as above.

< Raster Color Level Control > (Control Register 362 (16AH))

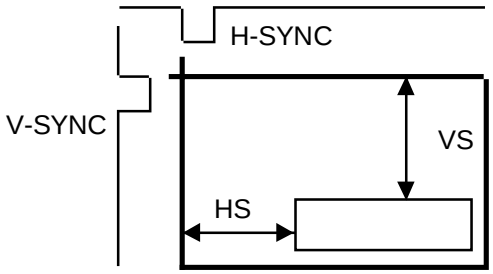
DA4(Lev 1)	DA3(Lev 0)	Raster Color Level `H`	Raster Color Level `L`	Remark
0	0	2.6V	1.6V	Level 0
0	1	2.2V	1.4V	Level 1
1	0	2.2V	1.4V	Level 1
1	1	2.0V	1.3V	Level 2

CONTROL REGISTER

1) Register 360 (168H)

<table>
<tr><th rowspan="2">DA0 ~ DAD</th><th rowspan="2">Register</th><th colspan="2">ContentSs</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Functions</th></tr>
<tr><td>0</td><td>HP0</td><td>0
1</td><td rowspan="6">$HS = Tc * \{ 4 * \sum_{n=0}^{5} (HPn * 2^{n}) + N \}$
Tc : osc. period (1/9 ㎒ = 111 nsec)
<table><tr><th>HSZ11
HSZ21</th><th>HSZ10
HSZ20</th><th>N</th></tr><tr><td>0</td><td>0</td><td>9</td></tr><tr><td>0</td><td>1</td><td>10</td></tr><tr><td>1</td><td>0</td><td>11</td></tr><tr><td>1</td><td>1</td><td>12</td></tr></table></td><td rowspan="6">Horizontal Start Position</td></tr>
<tr><td>1</td><td>HP1</td><td>0
1</td></tr>
<tr><td>2</td><td>HP2</td><td>0
1</td></tr>
<tr><td>3</td><td>HP3</td><td>0
1</td></tr>
<tr><td>4</td><td>HP4</td><td>0
1</td></tr>
<tr><td>5</td><td>HP5</td><td>0
1</td></tr>
<tr><td>6</td><td>HZ10</td><td>0
1</td><td rowspan="2"><table><tr><th>HZ11 \ HZ10</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">1st line horizontal character size control</td></tr>
<tr><td>7</td><td>HZ11</td><td>0
1</td></tr>
<tr><td>8</td><td>HZ20</td><td>0
1</td><td rowspan="2"><table><tr><th>HZ21 \ HZ20</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">2nd ~ 12th line horizontal character size control</td></tr>
<tr><td>9</td><td>HZ21</td><td>0
1</td></tr>
<tr><td>A</td><td>Blink Time</td><td>0
1</td><td>Blink Time = 1 sec
Blink Time = 0.5 sec</td><td>Blink Time Control</td></tr>
<tr><td>B</td><td>Blink 0</td><td>0
1</td><td rowspan="2"><table><tr><th>Blink1 \ Blink0</th><th>0</th><th>1</th></tr><tr><td>0</td><td>Off</td><td>Duty 25%</td></tr><tr><td>1</td><td>Duty 50%</td><td>Duty 75%</td></tr></table></td><td rowspan="2">Blinking Duty Control</td></tr>
<tr><td>C</td><td>Blink 1</td><td>0
1</td></tr>
<tr><td>D</td><td>Half-tone</td><td>0
1</td><td>Half-tone Off
Half-tone On</td><td>Half-tone On/Off</td></tr>
</table>

2) Register 361(169H)

<table>
<tr><th rowspan="2">DA0 ~ DAE</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Functions</th></tr>
<tr><td>0</td><td>VP0</td><td>0
1</td><td rowspan="6">$VS = H * \{ 4 * \sum_{n=0}^{5} (VPn * 2^{n}) + 3 \}$
H : horizontal synchronous pulse time
 
</td><td rowspan="6">Vertical Start Position</td></tr>
<tr><td>1</td><td>VP1</td><td>0
1</td></tr>
<tr><td>2</td><td>VP2</td><td>0
1</td></tr>
<tr><td>3</td><td>VP3</td><td>0
1</td></tr>
<tr><td>4</td><td>VP4</td><td>0
1</td></tr>
<tr><td>5</td><td>VP5</td><td>0
1</td></tr>
<tr><td>6</td><td>VZ10</td><td>0
1</td><td rowspan="2"><table><tr><th>VZ11 \ VZ10</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">1st line vertical character size control</td></tr>
<tr><td>7</td><td>VZ11</td><td>0
1</td></tr>
<tr><td>8</td><td>VZ20</td><td>0
1</td><td rowspan="2"><table><tr><th>VZ21 \ VZ20</th><th>0</th><th>1</th></tr><tr><td>0</td><td>1X</td><td>2X</td></tr><tr><td>1</td><td>3X</td><td>4X</td></tr></table></td><td rowspan="2">2nd ~ 12th line vertical character size control</td></tr>
<tr><td>9</td><td>VZ21</td><td>0
1</td></tr>
<tr><td>A</td><td>Internal</td><td>0
1</td><td>External SYNC
Internal SYNC</td><td>External / Internal Mode</td></tr>
<tr><td>B</td><td>Scroll On</td><td>0
1</td><td>Scroll Off
Scroll On</td><td>Scroll Display Control</td></tr>
<tr><td>C</td><td>Scroll Time</td><td>0
1</td><td>Scroll Time 0.5 sec
Scroll Time 1 sec</td><td>Scroll Time Control</td></tr>
<tr><td>D</td><td>Blank L Level</td><td>0
1</td><td>Blank Low Level 0 (1.4V)
Blank Low Level 1 (1.8V)</td><td>Blank Color Low Level Control</td></tr>
<tr><td>E</td><td>Ext fsc</td><td>0
1</td><td>External 4fsc X-TAL (Pin 21,22)
External fsc input to Pin 21(*Only for IC Test)</td><td>External fsc Clock Input</td></tr>
</table>

3) Register 362 (16AH)

<table>
<tr><th rowspan="2">DA0 ~ DAE</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Remark</th></tr>
<tr><th>State</th><th>Functions</th></tr>
<tr><td>0</td><td>R_cntr0</td><td>0
1</td><td rowspan="3"><table>
<tr><th>Cntr2</th><th>Cntr1</th><th>Cntr0</th><th>NTSC</th><th>PAL</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Red</td><td>Red</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Blue</td><td>G + Y</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>B + G</td><td>B + G</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Yellow</td><td>Blue</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Orange</td><td>Magenta</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Magenta</td><td>Yellow</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Cyan</td><td>Green</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Gray</td><td>Gray</td></tr>
</table></td><td rowspan="3">Raster Color Control</td></tr>
<tr><td>1</td><td>R_cntr1</td><td>0
1</td></tr>
<tr><td>2</td><td>R_cntr2</td><td>0
1</td></tr>
<tr><td>3</td><td>R_lev0</td><td>0
1</td><td rowspan="2"><table>
<tr><th>Lev 1 \ Lev 0</th><th>0</th><th>1</th></tr>
<tr><td>0</td><td>Level 0</td><td>Level 1</td></tr>
<tr><td>1</td><td>Level 1</td><td>Level 2</td></tr>
</table></td><td rowspan="2">Raster Color Level Control</td></tr>
<tr><td>4</td><td>R_lev1</td><td>0
1</td></tr>
<tr><td>5</td><td>C_level</td><td>0
1</td><td>Character Level 1 (2.7V)
Character Level 2 (2.5V)</td><td>Character Level Control</td></tr>
<tr><td>6</td><td>Blank Color</td><td>0
1</td><td>Blank Color Off
Blank Color On</td><td>When SECAM, Blank Color Off is not used.</td></tr>
<tr><td>7</td><td>BLK0</td><td>0
1</td><td rowspan="2">Blank Mode Select by Controlling the Data of Register 363 (16BH)</td><td rowspan="2"></td></tr>
<tr><td>8</td><td>BLK1</td><td>0
1</td></tr>
<tr><td>9</td><td>NTSC /PAL</td><td>0
1</td><td>NTSC
PAL</td><td rowspan="2">Color System Select</td></tr>
<tr><td>A</td><td>SECAM</td><td>0
1</td><td>NTSC or PAL
SECAM</td></tr>
<tr><td>B</td><td>Interlace /Non-I</td><td>0
1</td><td>Interlace
Non-Interlace</td><td>Scanning Type Control</td></tr>
<tr><td>C</td><td>P626/ P628</td><td>0
1</td><td>PAL 1 Field = 626H
PAL 1 Field = 628H</td><td>PAL Mode 1 Field Control</td></tr>
<tr><td>D</td><td>DSP ON</td><td>0
1</td><td>Display Off
Display On</td><td>Character Display Control</td></tr>
<tr><td>E</td><td>RAM ERS</td><td>0
1</td><td>RAM is not erased.
RAM is erased.</td><td></td></tr>
</table>

4) Register 363 (16BH)

DA0 ~ DAC	Register	Contents		Remark
		State	Functions	
0	DSP0	0	1st line BLANK mode select	
		1		
1	DSP1	0	2nd line BLANK mode select	
		1		
2	DSP2	0	3th line BLANK mode select	
		1		
3	DSP3	0	4th line BLANK mode select	
		1		
4	DSP4	0	5th line BLANK mode select	
		1		
5	DSP5	0	6th line BLANK mode select	
		1		
6	DSP6	0	7th line BLANK mode select	
		1		
7	DSP7	0	8th line BLANK mode select	
		1		
8	DSP8	0	9th line BLANK mode select	
		1		
9	DSP9	0	10th line BLANK mode select	
		1		
A	DSPA	0	11th line BLANK mode select	
		1		
B	DSPB	0	12th line BLANK mode select	
		1		
C	All BLK	0	Depend on BLK0, BLK1	
		1	All screen blank except character	

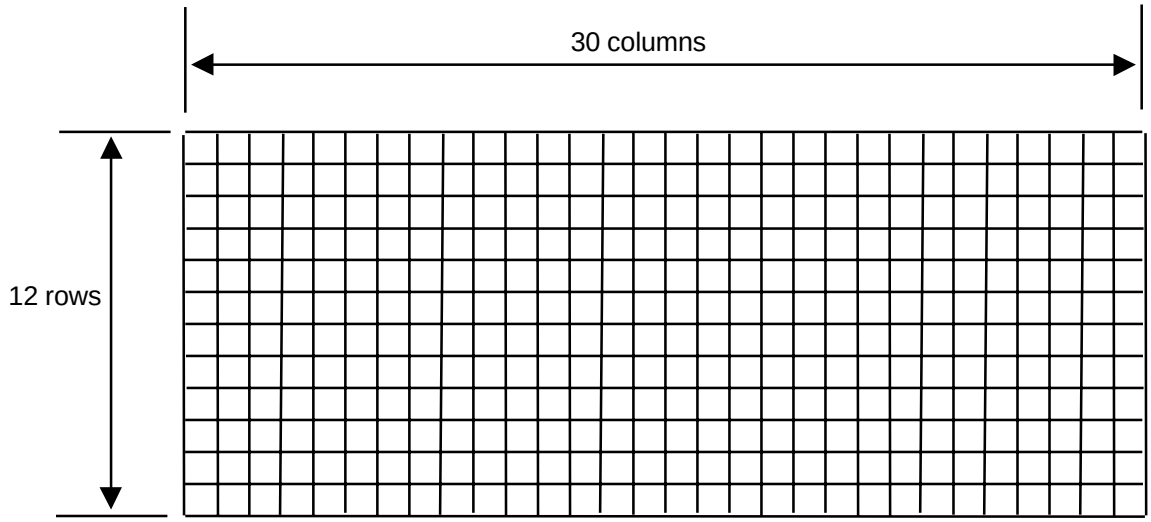
BLK1	BLK0	DSP	Blank Mode
0	0	0	Blank Off
		1	O*
	1	0	C*
		1	O*
1	0	0	O*
		1	R*
	1	0	R*
		1	C*
ALL BLK = 1			All Blank

C*	Character Blank
O*	Outline Blank
R*	Raster Blank

5) Register 364 (16CH)

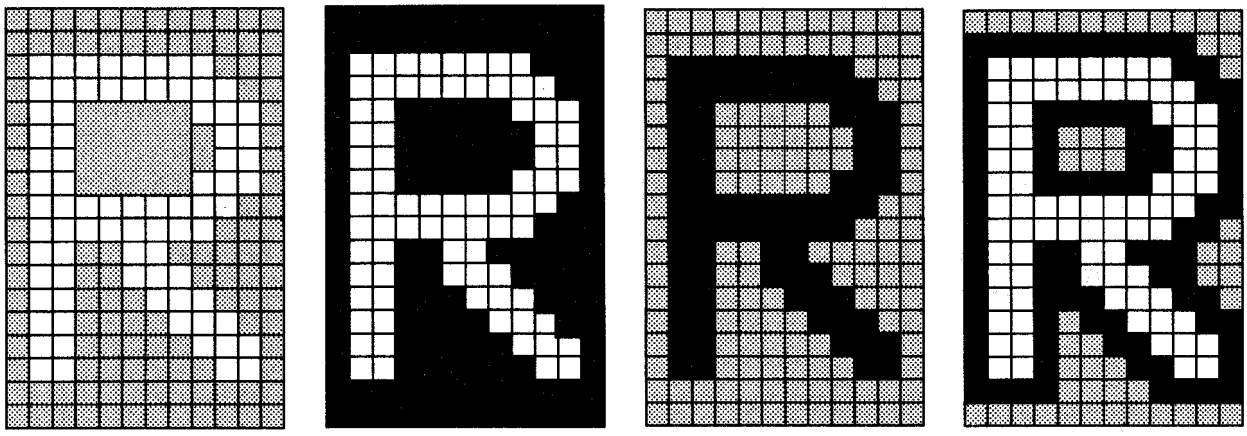
DA0 ~ DAE	Register	Contents		Remark
		State	Functions	
0	Fch0	0	$Fch = 30 * \{\sum_{n=0}^{3} Fchn * 512 * 2^{n}\}$ Hz Capture Range `H` = 15.36 kHz ~ 230.4 kHz	Sync Detect Capture Range High Sensitity Control
		1		
1	Fch1	0		
		1		
2	Fch2	0		
		1		
3	Fch3	0		
		1		
4	Fcl0	0	$Fcl = 30 * \{\sum_{n=0}^{3} Fchn * 64 * 2^{n}\}$ Hz Capture Range `L` = 1.92 kHz ~ 28.8 kHz	Sync Detect Capture Range Low Sensitity Control
		1		
5	Fcl1	0		
		1		
6	Fcl2	0		
		1		
7	Fcl3	0		
		1		
8	Flh0	0	$Flh = 30 * \{\sum_{n=0}^{3} Fchn * 512 * 2^{n}\}$ Hz Locking Range `H` = 15.36 kHz ~ 230.4 kHz	Sync Detect Locking Range High Sensitity Control
		1		
9	Flh1	0		
		1		
A	Flh2	0		
		1		
B	Flh3	0		
		1		
C	Fll0	0	$Fll = 30 * \{\sum_{n=0}^{2} Fchn * 64 * 2^{n}\}$ Hz Locking Range `L` = 1.92 kHz ~ 13.44 kHz	Sync Detect Locking Range Low Sensitity Control
		1		
D	Fll1	0		
		1		
E	Fll2	0		
		1		

11. SCREEN STRUCTURE



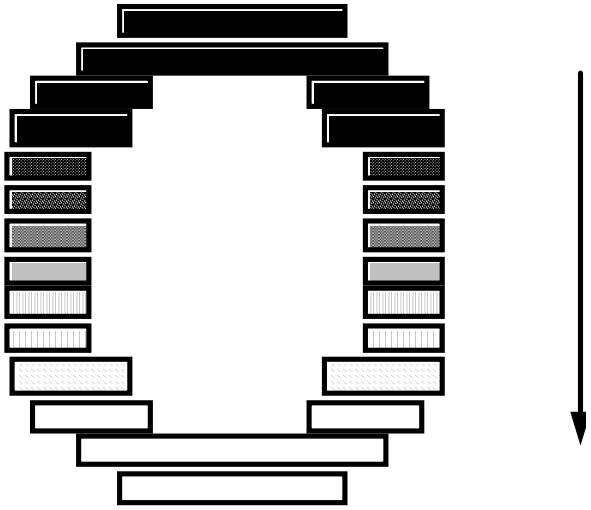
TV Screen

12. BLANK MODE



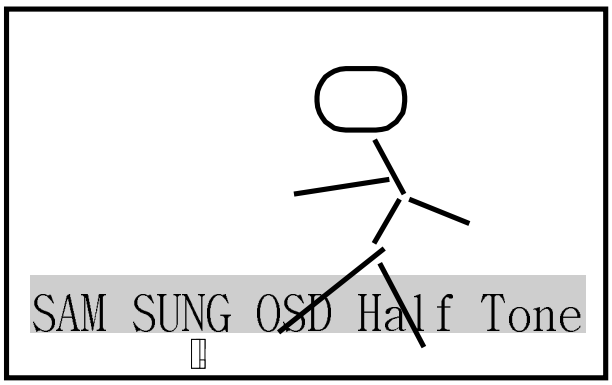
Blank Off Raster Blank Character Blank Outline Blank

13. SCROLL FUNCTION



When control register 361, scroll bit (DAB bit) is high, character display on/off from top to down slowly about 0.5 sec or 1 sec. (also controlled by register setting)

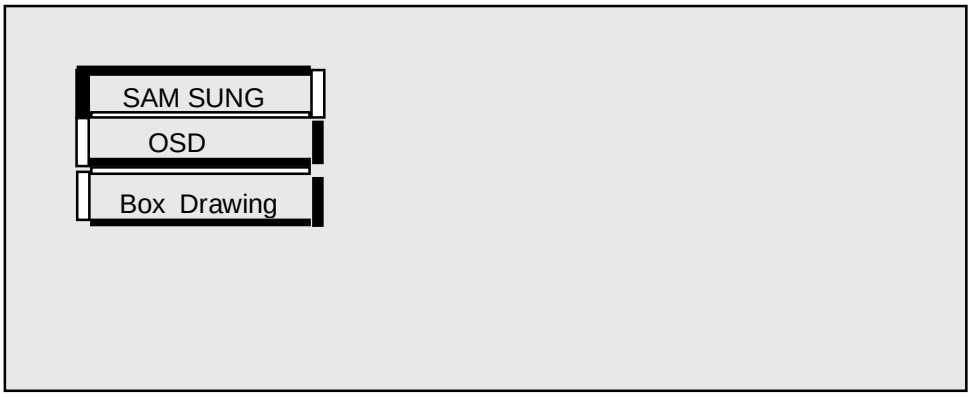
14. HALF-TONE FUNCTION



TV Screen

When control register 360, half tone bit (DAD bit) is high, character display with half luminance level and also display background screen.

15. BOX DRAWING FUNCTION



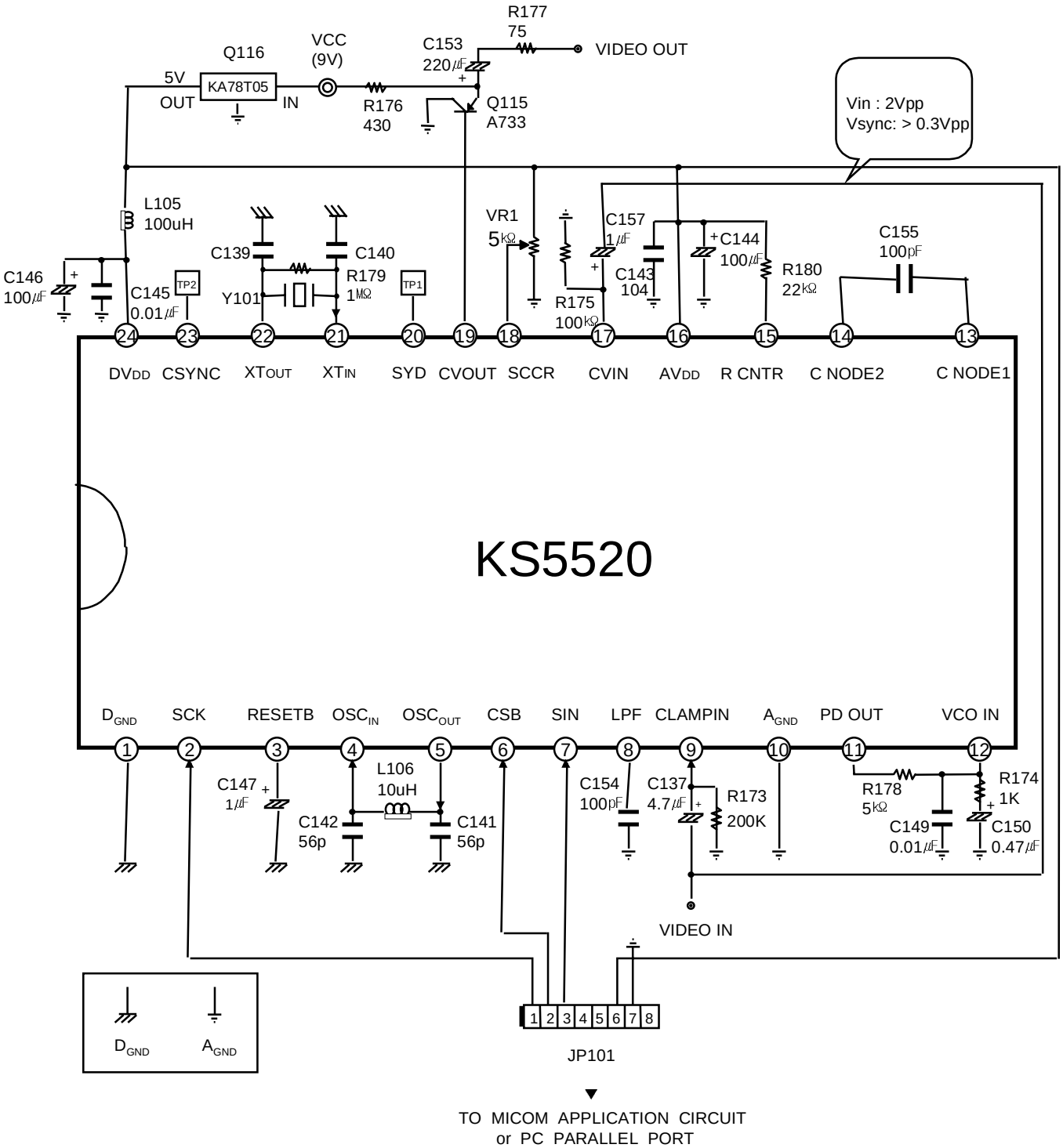
TV Screen

It can draw rectangle box. If you want to concave display, top and left side of characters are drawn black color, bottom and right side of characters are drawn white color and also want to convex display, character colors are vice versa.

It is all controlled by each RAM attribution bit, that is box1 (DAE), box0 (DAD) and box_inv (DAF).

box1 \ box0	0	1
0	BOX OFF	S
1	S	S

16-1. APPLICATION CIRCUIT (OSD BLOCK)



The circuit drawn above is for Demo Board.

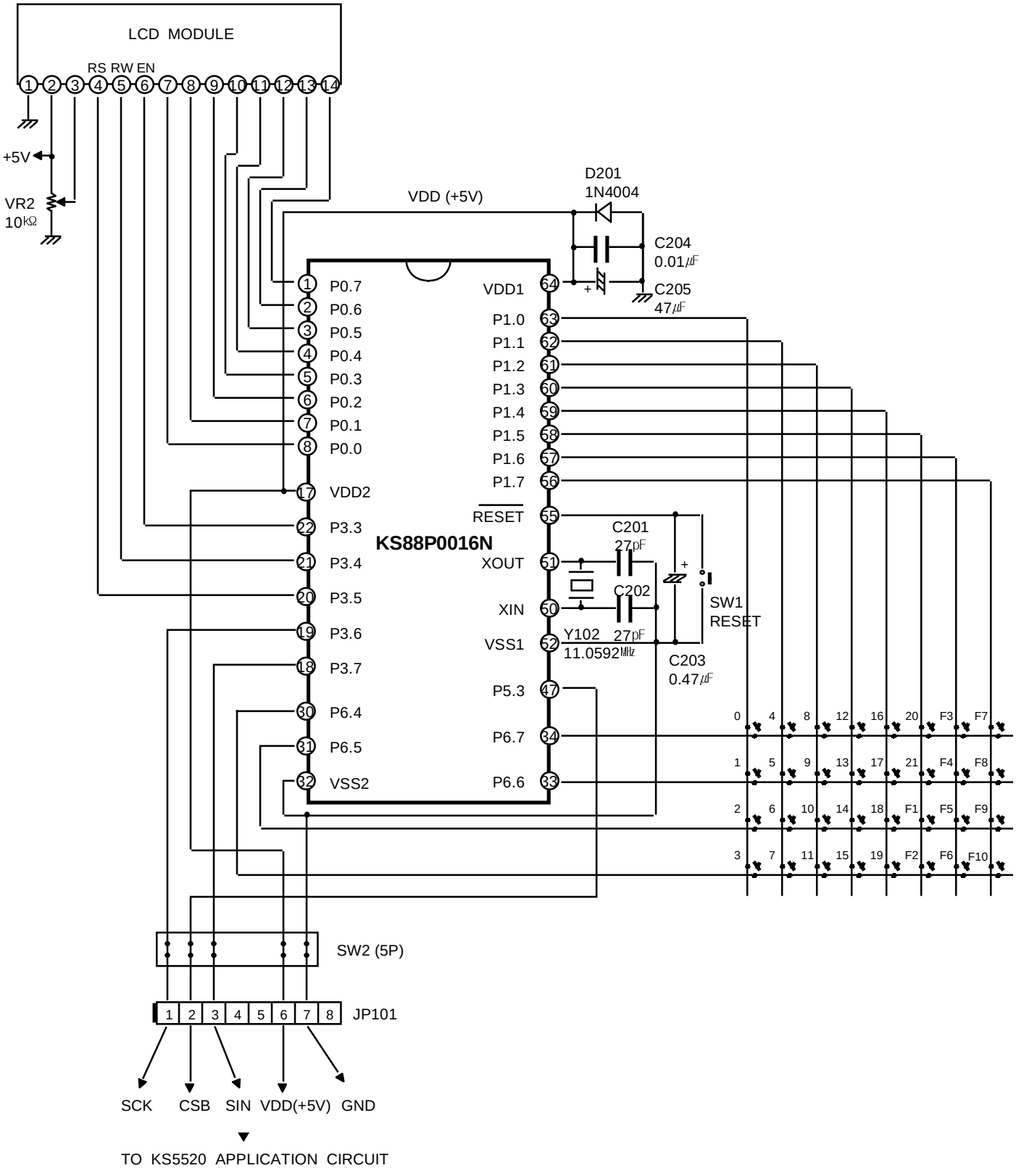
• Y101 (4fsc X-TAL) → NTSC : 14.31818MHz

PAL : 17.734475MHz

• C139 / C140 : The load CAP of X-TAL Y101 has a difference each according to its manufactures.

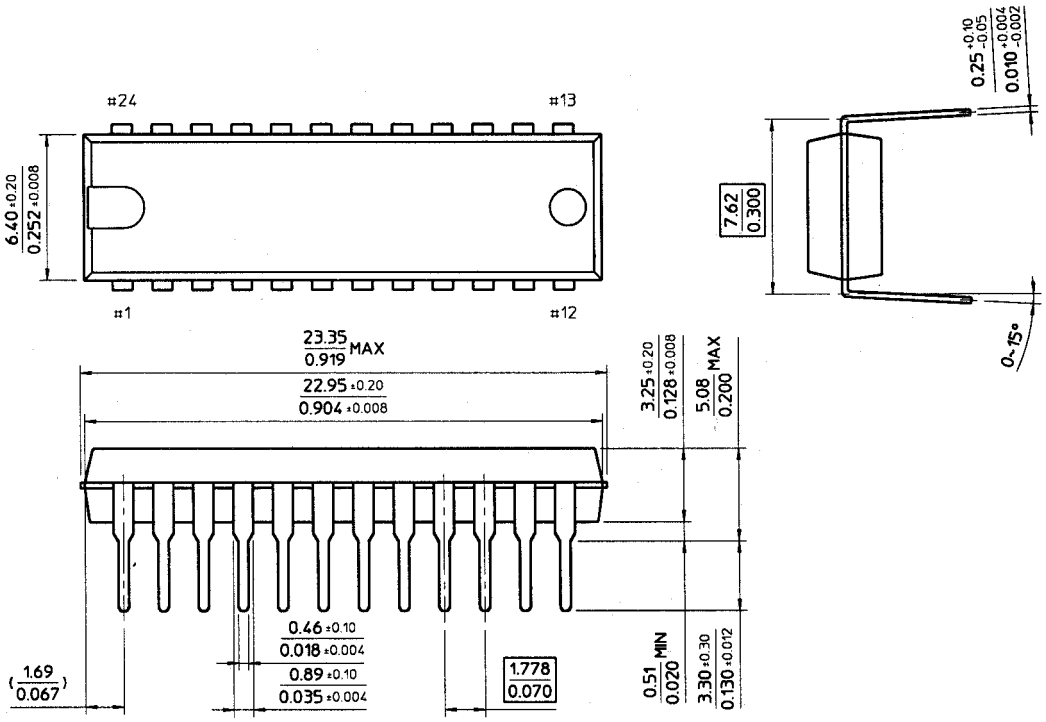
27pF typical (NTSC), 47pF typical (PAL)

16-2. APPLICATION CIRCUIT (CONTROLLER BLOCK)



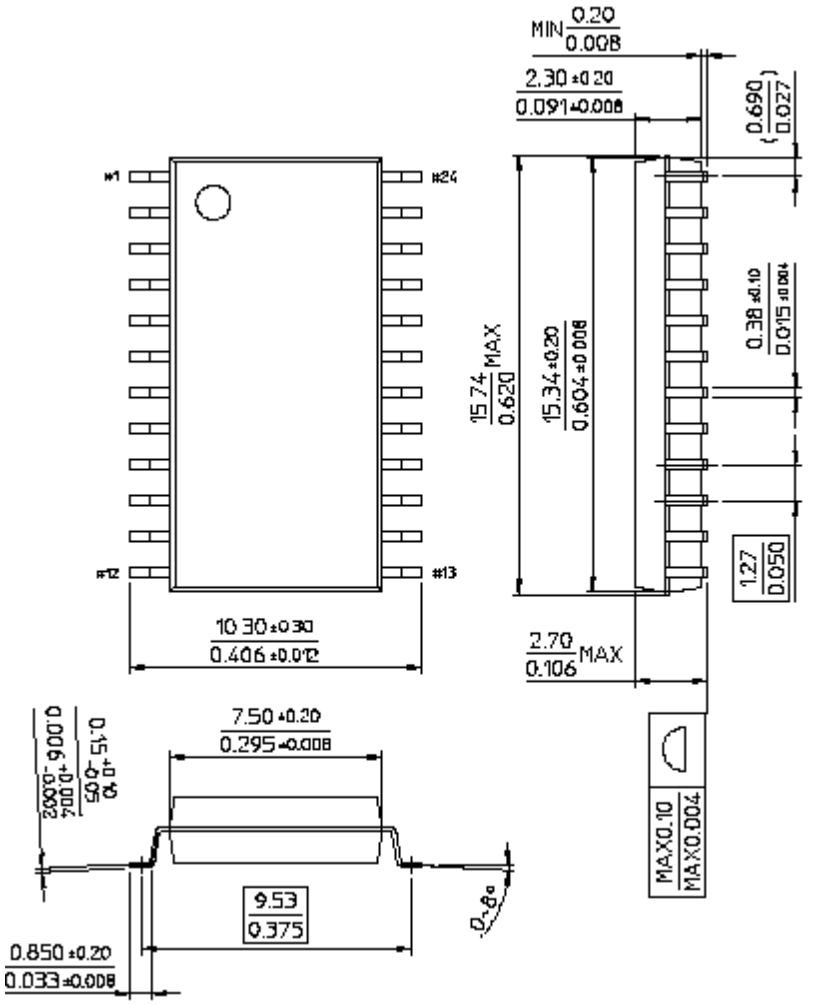
17. PACKAGE DIMENSIONS

24-SDIP-300 Dimensions in Milimeters



17. PACKAGE DIMENSIONS (Continued)

24-SOP-375 Dimensions in Milimeters



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