DCR1120F34

Phase Control Thyristor

DS6054-1 April 2011 (LN28270)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR1120F34 DCR1120F32 DCR1120F30 DCR1120F28	3400 3200 3000 2800	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 150mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} +100V respectively

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

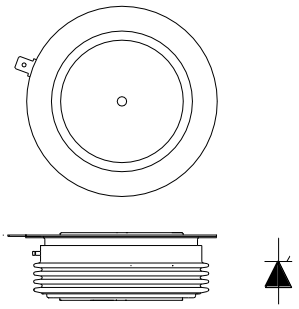
DCR1120F34

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V_{DRM}	**3400 V**
$I_{T(AV)}$	**1120 A**
I_{TSM}	**17000 A**
dV/dt*	**1000 V/µs**
dI/dt	**150 A/µs**

* **Higher dV/dt selections available**



Outline type code: F

(See Package Details for further information)

Fig. 1 Package outline

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	1120	A
$I_{T(RMS)}$	RMS value	-	1760	A
I_T	Continuous (direct) on-state current	-	1580	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	17.0	kA
I^2t	I^2t for fusing	V_R = 0	1.45	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.02	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Double side cooled	DC	-	0.005	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / $_{VRRM}$		-	125	°C
T_{stg}	Storage temperature range			-40	140	°C
F_m	Clamping force			18	26	kN

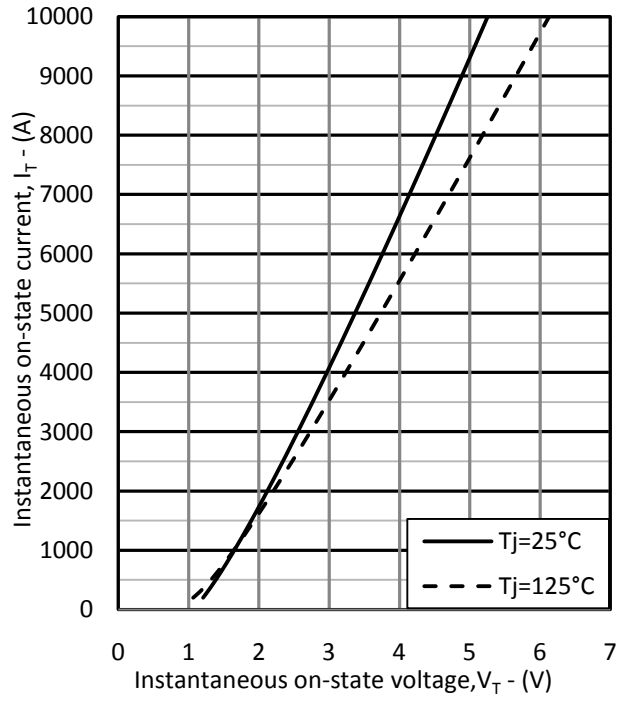
DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	150	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		1000	-	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2000A	Repetitive 50Hz	-	150	A/µs
		Gate source 30V, 10Ω, t_r < 0.5µs, T_j = 125°C	Non-repetitive	-	1000	A/µs
V_T	On-state voltage	I_T = 1500A, T_{case} = 125°C			1.92	V
$V_{T(TO)}$	Threshold voltage – Low level	T_{case} = 125°C		-	1.08	V
r_T	On-state slope resistance – Low level	T_{case} = 125°C		-	0.56	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω, t_r = 0.5µs, T_j = 25°C		-	3.0	µs
t_q	Turn-off time	T_j = 125°C, V_R = 100V, dI/dt = 10A/µs, dV_{DR}/dt = 20V/µs linear to 67% V_{DRM}		-	400	µs
Q_S	Stored charge	I_T = 2000A, tp = 1000us, T_j = 125°C, dI/dt =10A/µs,		-	4500	µC
I_{RR}	Reverse recovery current			-	180	A
I_L	Latching current	T_j = 25°C,		-	1	A
I_H	Holding current	T_j = 25°C,		-	200	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	3	V
V_{GD}	Gate non-trigger voltage	At 40% V_{DRM}, T_{case} = 125°C	TBD	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	300	mA
I_{GD}	Gate non-trigger current	At 40% V_{DRM}, T_{case} = 125°C	TBD	mA

CURVES



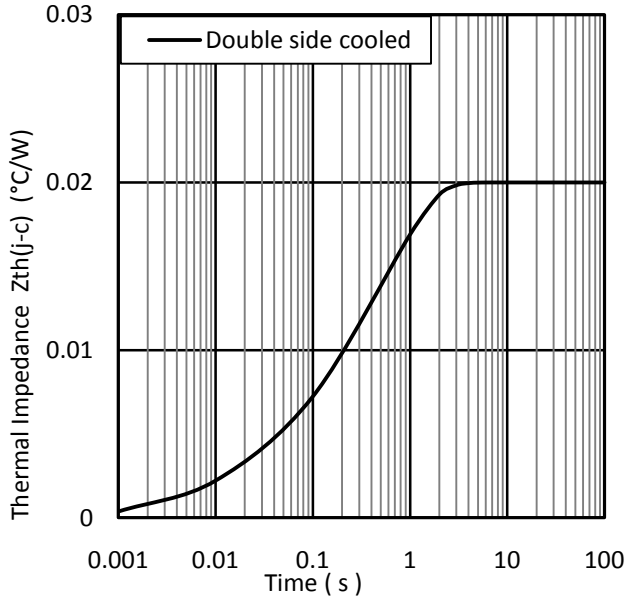
V_{TM} EQUATION

$V_{TM} = A + B\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 0.460924
B = 0.082515
C = 0.000435841
D = 0.00551769

These values are valid for T_j = 125°C

Fig.2 Maximum &minimum on-state characteristics



$$R_{thjc}(t) = \sum_{i=1}^{n} R_{thi} \cdot \left(1 - e^{-\frac{t}{\tau_i}}\right)$$

i	τ_i (s)	R_{thi} (°C/kW)
1	0.6894	13.267
2	0.0872	4.05
3	0.0217	1.585
4	0.0043	1.102

Fig.3 Maximum (limit) transient thermal impedance – junction to case (°C/W)

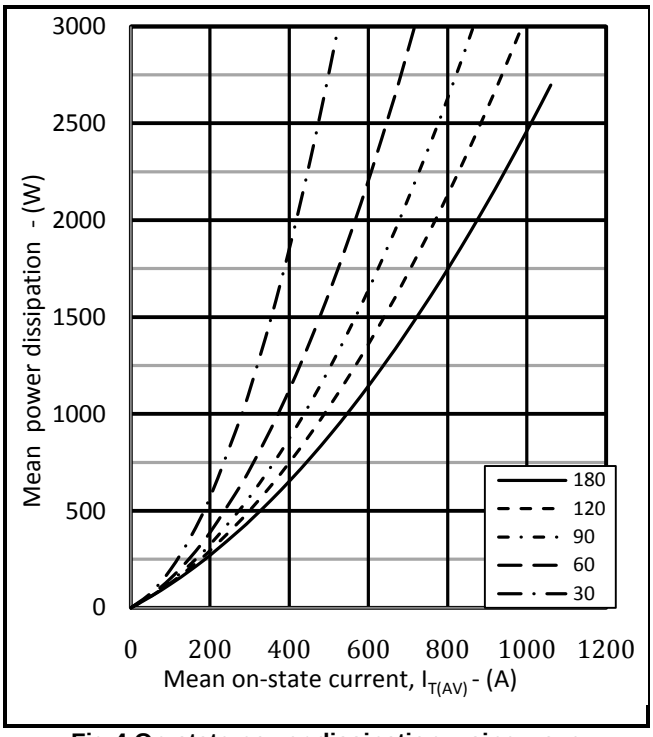


Fig.4 On-state power dissipation – sine wave

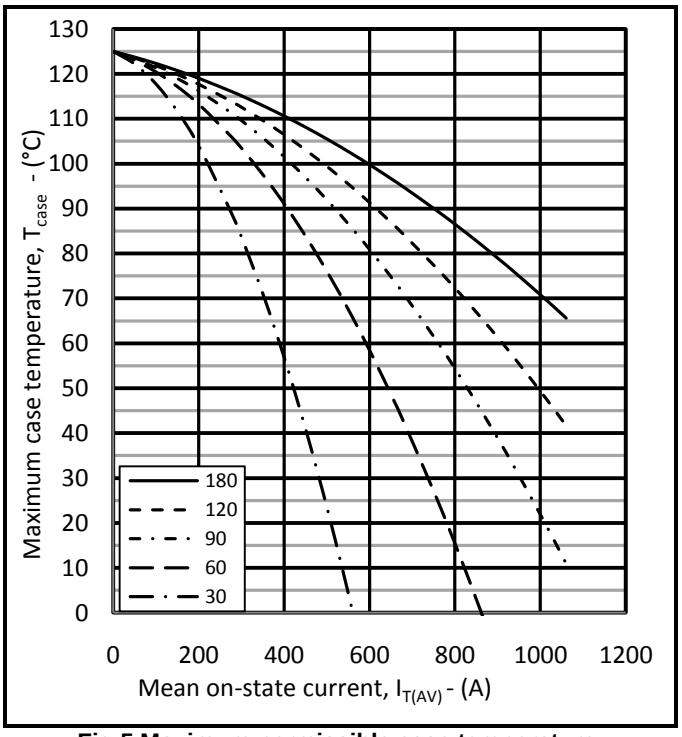


Fig.5 Maximum permissible case temperature, double side cooled – sine wave

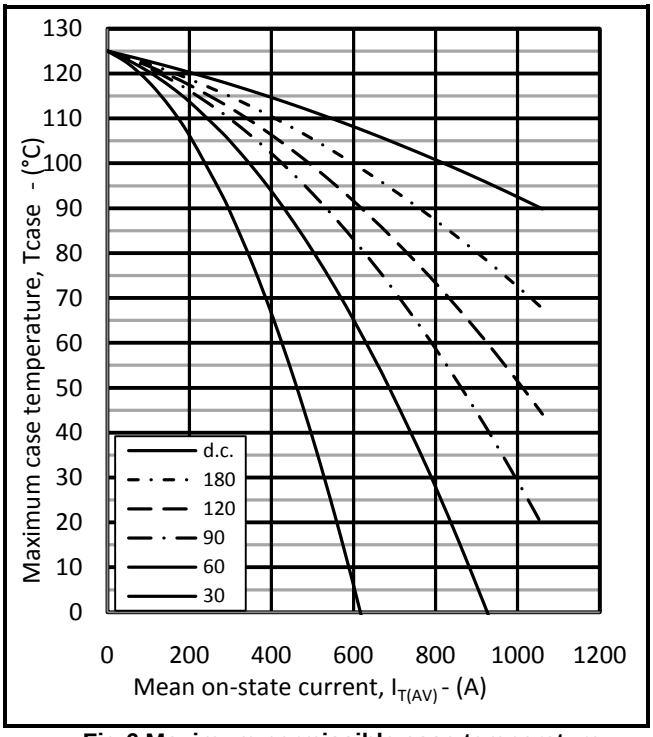


Fig.6 Maximum permissible case temperature, double side cooled – rectangular wave

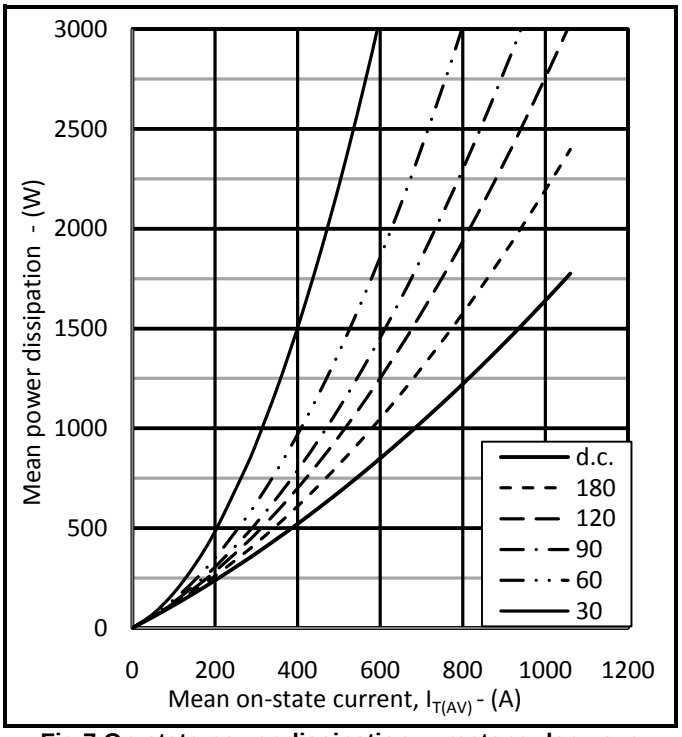


Fig.7 On-state power dissipation – rectangular wave

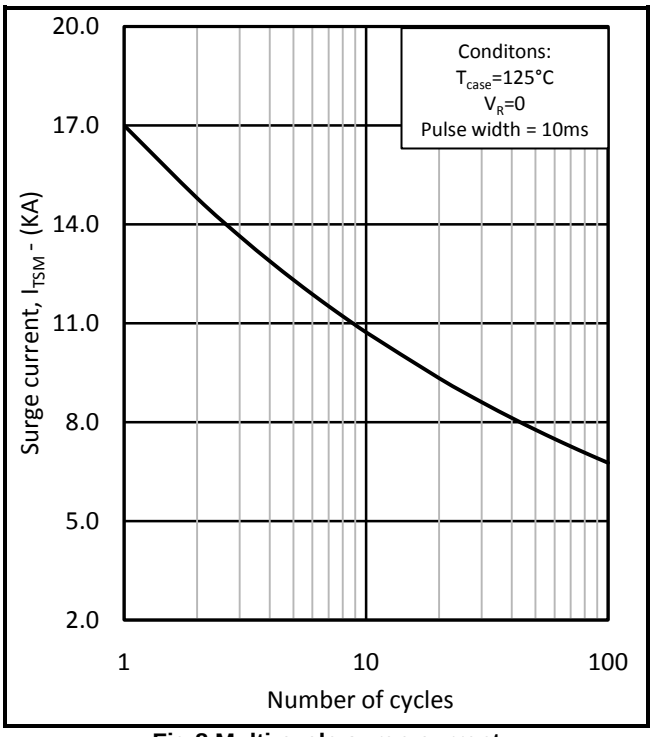


Fig.8 Multi-cycle surge current

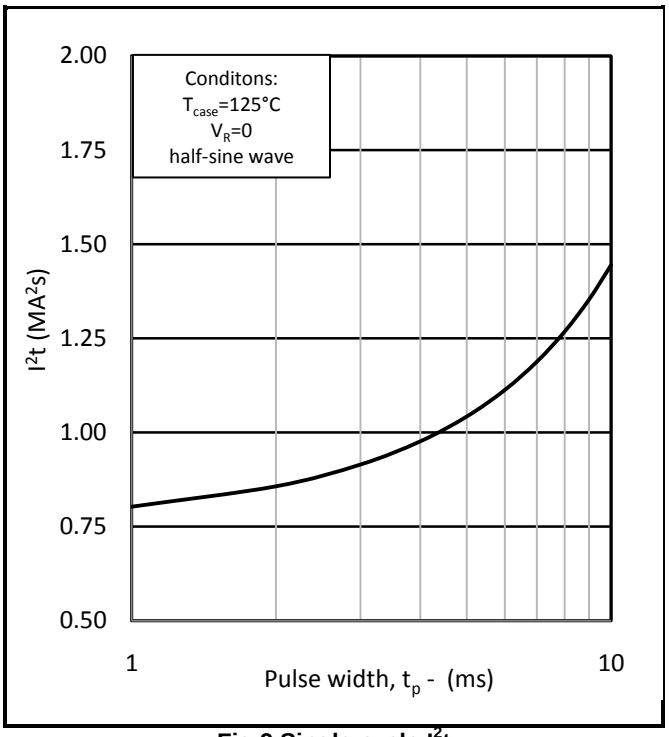


Fig.9 Single-cycle I^2t

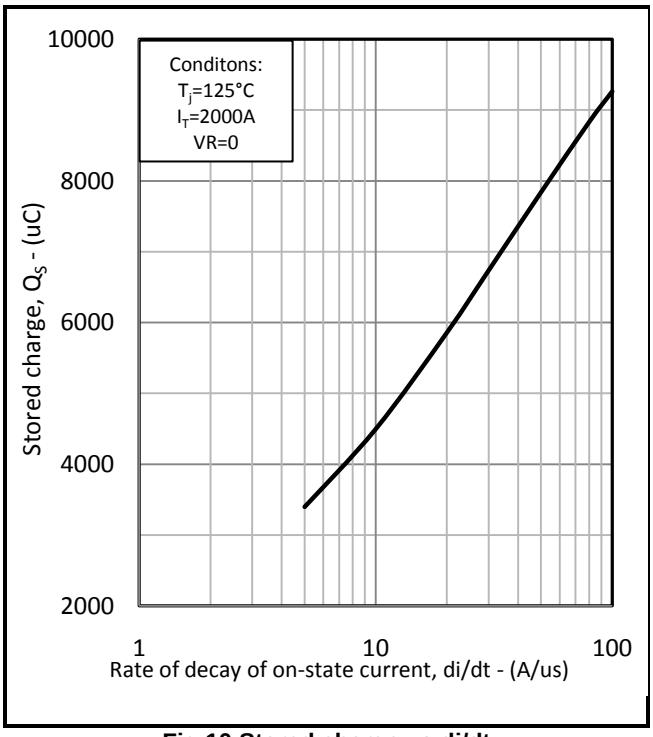


Fig.10 Stored charge vs di/dt

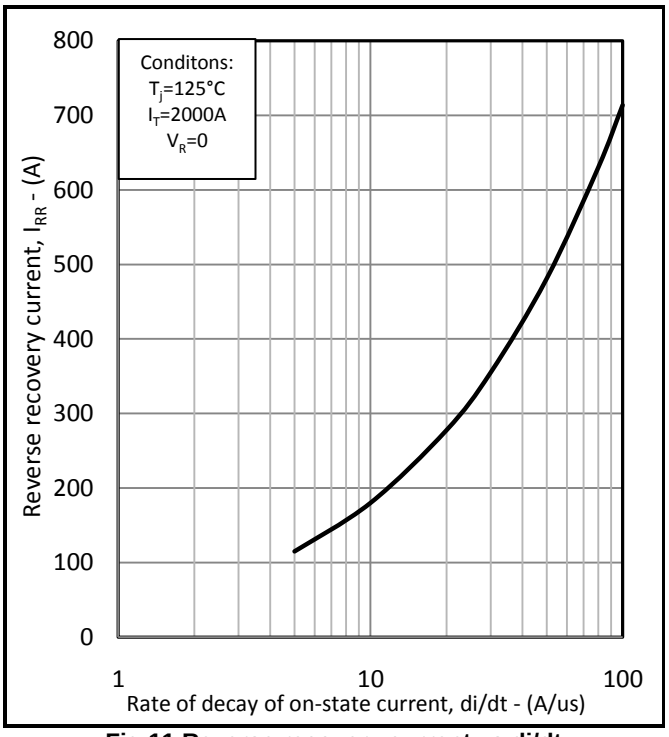


Fig.11 Reverse recovery current vs di/dt

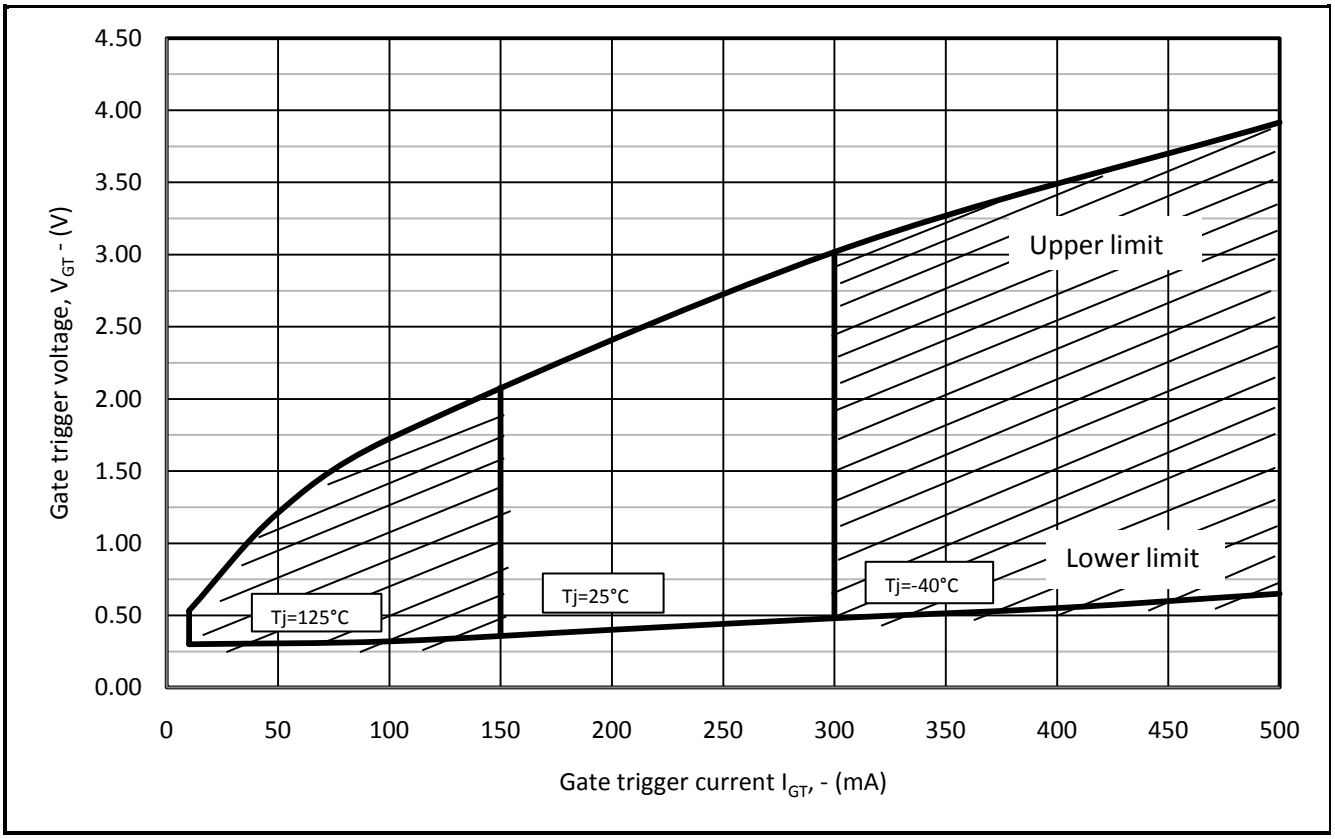


Fig.12 Gate characteristics

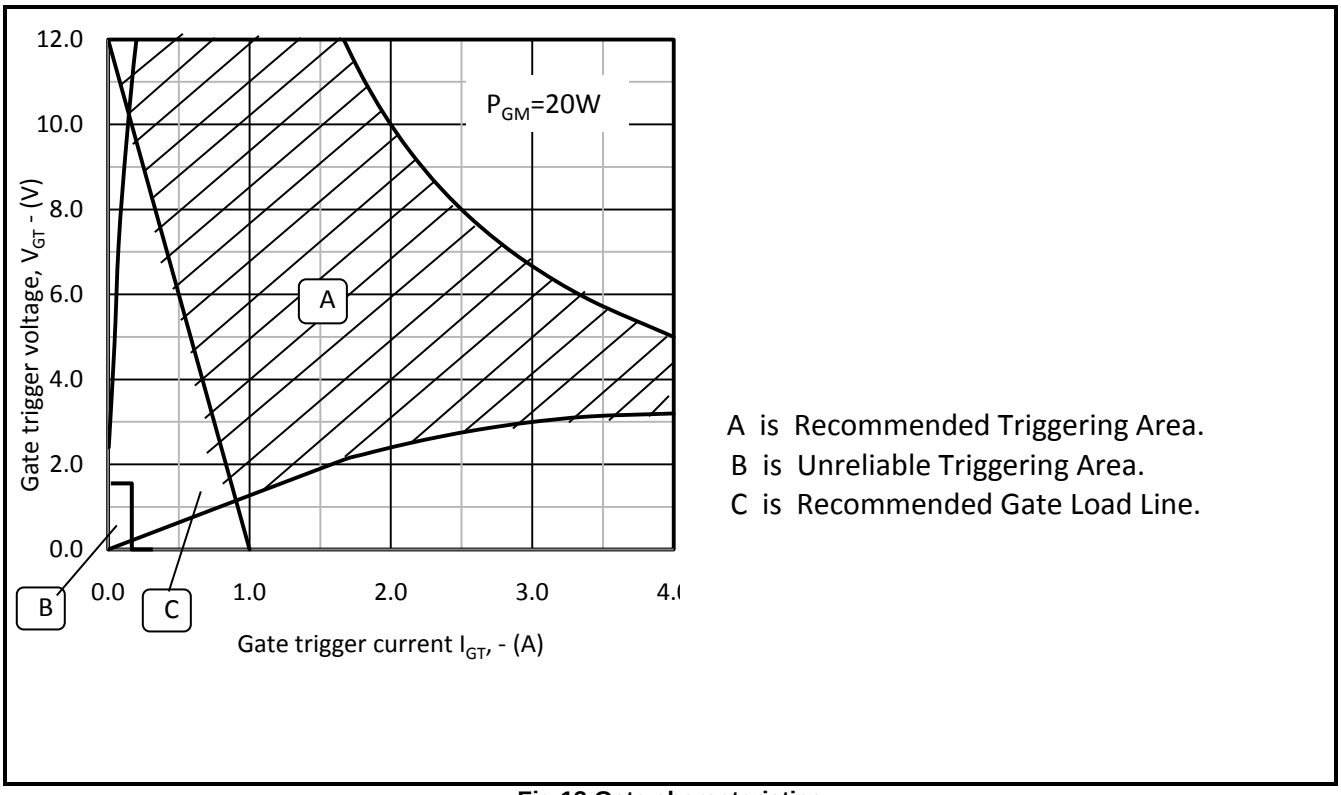
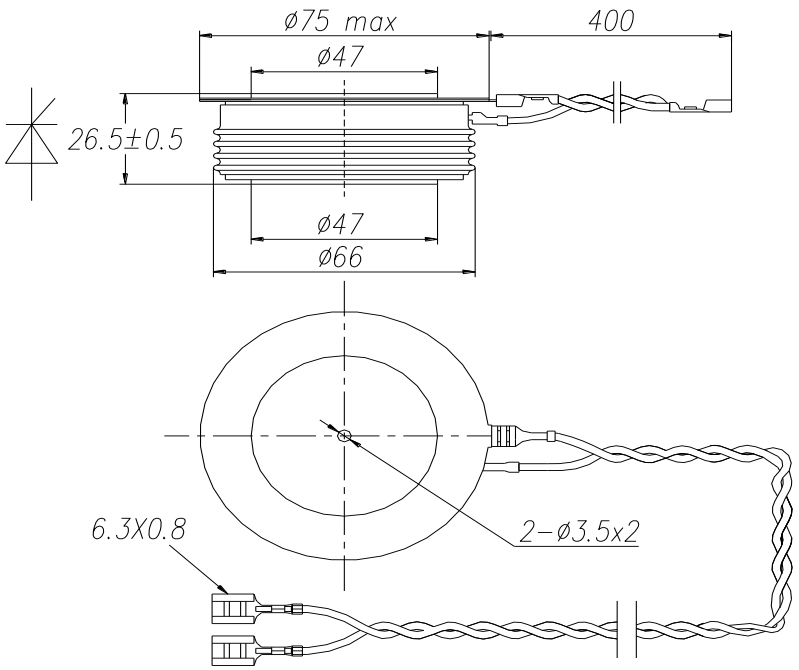


Fig.13 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Package outline type code: F

Fig.14 Package outline

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