100V, 2A Peak, Half-Bridge Driver with Tri-Level PWM Input and Adjustable Dead-Time

ISL78420

The ISL78420 is a 100V, high frequency, half-bridge MOSFET driver with a tri-level PWM input. This part is a derivative of the HIP2121 half-bridge driver. The non-automotive version of the ISL78420 is the HIP2124.

This driver is designed to work in conjunction with the ISL78220, "6-Phase Interleaved Boost PWM Controller with Light Load Efficiency Enhancement". Equally, it can be used in most applications where a half-bridge driver is used.

This driver has a programmable dead-time to ensure break-before-make operation between the high-side and low-side drivers. A resistor is used to adjust the dead-time up to 220ns.

The tri-level input allows the PWM input to also function as a disable input. When the PWM input is a logic high, the high-side bridge FET is turned on and the low-side FET is off. When the input is a logic low, the low-side bridge FET is turned on and the high-side FET is turned off. When the input voltage is midrange, both the high and low-side bridge FETs are turned off.

The enable pin (EN), when low, drives both outputs to a low state. This input is used when the controller does not utilize a tri-state output. All logic inputs are V_{DD} tolerant.

Two package options are provided. The 10 Ld 4x4 DFN package has standard pinouts. The 9 Ld 4x4 DFN package omits pin 2 to comply with 100V conductor spacing per IPC-2221.

Features

- Programmable break-before-make dead-time prevents shoot-through and is adjustable up to 220ns
- Bootstrap supply maximum voltage to 114VDC
- Wide supply voltage range (8V to 14V)
- Supply undervoltage protection
- On-chip 1Ω bootstrap diode
- Unique tri-level PWM input logic enables phase shedding when using multi-phase PWM controllers (e.g. ISL78220/225)
- 9 Ld TDFN "B" package compliant with 100V conductor spacing guidelines per IPC-2221
- AEC-Q100 Qualified

Applications

- Automotive applications
- Multi-phase boost (ISL78220/225)
- Half-bridge DC/DC converter
- Class-D amplifiers
- Forward converter with active clamp

Related Literature

- FN7668 HIP2120, HIP2121 "100V, 2A Peak, High Frequency Half-Bridge Drivers with Adjustable Dead Time Control and PWM Input"
- FN8363 HIP2124, "100V, 2A Peak, Half Bridge Driver with Tri-level Input and Adjustable Dead Time" (non-automotive)
- FN7688 ISL78220, "6-Phase Interleaved Boost PWM Controller with Light Load Efficiency Enhancement"
- FN7909 ISL78225, "4-Phase Interleaved Boost PWM Controller with Light Load Efficiency Enhancement"

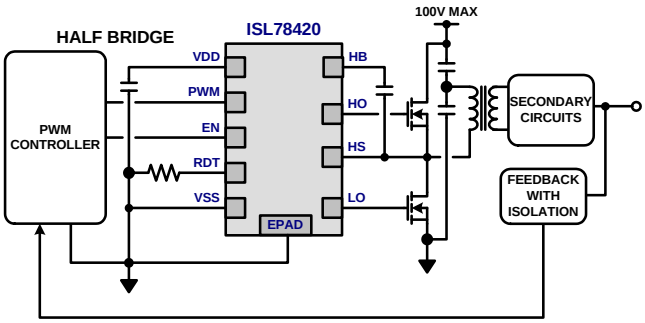


FIGURE 1. TYPICAL APPLICATION

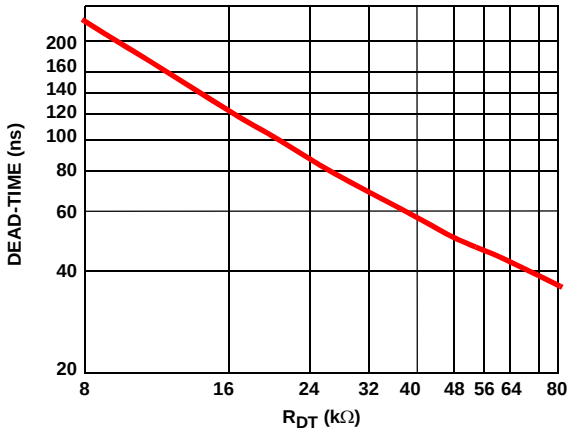
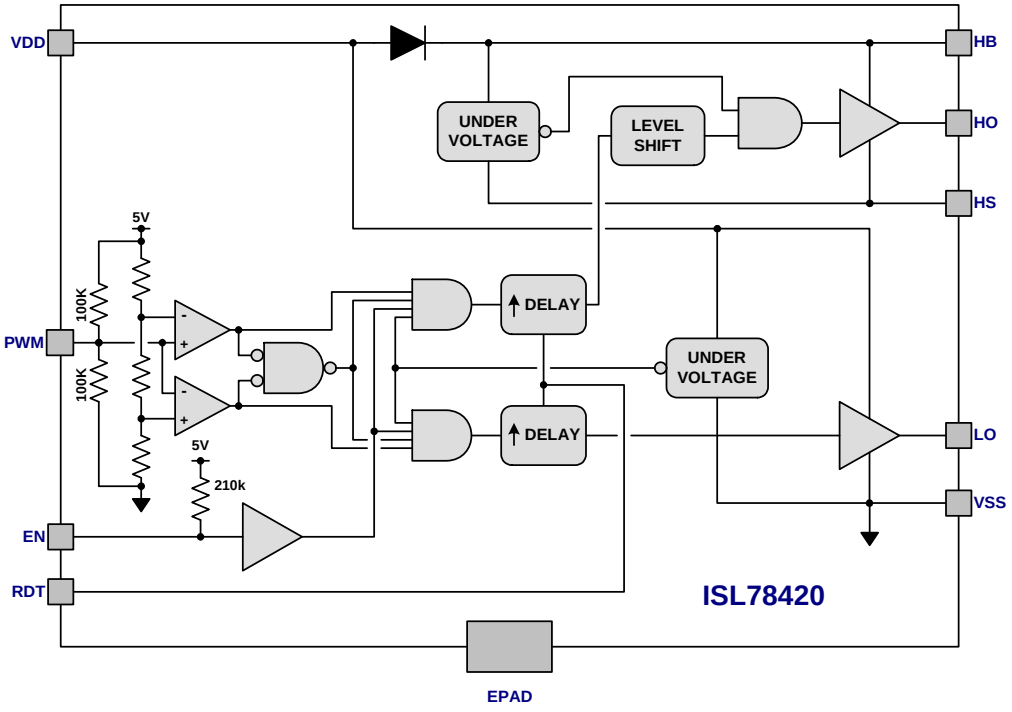


FIGURE 2. DEAD-TIME vs TIMING RESISTOR

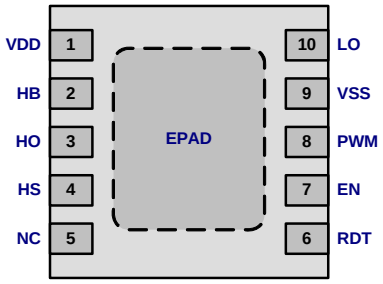
CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Block Diagram

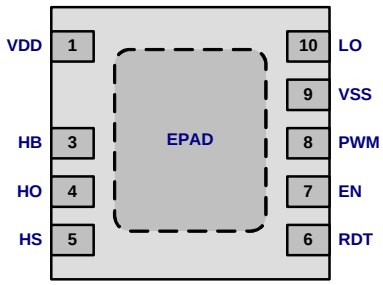


Pin Configurations

ISL78420ARTAZ
(10 LD 4X4 TDFN)
TOP VIEW



ISL78420ARTBZ
(9 LD 4X4 TDFN)
TOP VIEW



Pin Descriptions

10 LD	9 LD	SYMBOL	DESCRIPTION
1	1	VDD	Positive supply voltage for lower gate driver. Decouple this pin to ground with a 4.7µF or larger ceramic capacitor to VSS
2	3	HB	High-side bootstrap supply voltage referenced to HS. Connect bootstrap capacitor to this pin and HS.
3	4	HO	High-side output connected to gate of high-side FET.
4	5	HS	High-side source connect to source of high-side FET. Connect bootstrap capacitor to this pin and HB.
8	8	PWM	PWM input. For PWM = 5V, HO = 1, LO = 0. For PWM = 0V, HO = 0, LO = 1. For PWM = 2.5V, HO = LO = 0.
7	7	EN	Output enable, when low, HO = LO = 0
9	9	VSS	Negative voltage supply, Connected to ground.
10	10	LO	Low-side output. Connect to gate of low-side FET.
5	-	NC	No Connect. This pin is isolated from all other pins. May optionally be connected to VSS. Note that on the 9 Ld package, there is no pin present at the location normally occupied by pin 2.
6	6	RDT	A resistor connected between this pin and VSS adds dead time by adding delay time to the falling and rising edges of the PWM input.
-	-	EPAD	The epad is electrically isolated. It is recommended that the epad be connected to the VSS plane for heat removal.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	INPUT	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL78420ARTAZ	78420 AZ	5V Tri-level	-40 +125	10 Ld 4x4 TDFN	L10.4x4
ISL78420ARTBZ (Note 4)	78420 BZ	5V Tri-level	-40 +125	9 Ld 4x4 TDFN	L9.4x4

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78420. For more information on MSL please see tech brief TB363. and TB477.
4. “B” package option has alternate pin assignments for compliance with 100V Conductor Spacing Guidelines per IPC-2221. Note that Pin 2 is omitted for additional spacing between pins 1 and 3.

Absolute Maximum Ratings (Note 6)

Supply Voltage, V_{DD}, V_{HB} - V_{HS} (Notes 5) . . . . . -0.3V to 18V
PWM and EN Input Voltage . . . . . -0.3V to V_{DD} + 0.3V
Voltage on LO . . . . . -0.3V to V_{DD} + 0.3V
Voltage on HO . . . . . VHS - 0.3V to VHB + 0.3V
Voltage on HS (Continuous) . . . . . -1V to 110V
Voltage on HB 118V
Average Current in V_{DD} to HB Diode 100mA

Maximum Recommended Operating Conditions (Note 6)

Supply Voltage, V_{DD} . . . . . 8V to 14V
Voltage on HS . . . . . -1V to 100V
Voltage on HS . . . . . .(Repetitive Transient) -5V to 105V
Voltage on HB . . . . . V_{HS} + 8V to V_{HS} + 14V and
. . . . . V_{DD} - 1V to V_{DD} + 100V
HS Slew Rate. . . . . <50V/ns
Temperature . . . . . .-40°C to +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld TDFN (Notes 7, 8)	42	4
9 Ld TDFN (Notes 7, 8)	42	4

Max Power Dissipation at +25°C in Free Air
10 Ld TDFN 3.0W
9 Ld TDFN 3.1W
Storage Temperature Range. . . . . .-65°C to +150°C
Junction Temperature Range . . . . . .-55°C to +150°C
Pb-Free Reflow Profile (*) . . . . . see TB487
*Peak temperature during solder reflow . . . . . +235°C max

ESD Ratings
Human Body Model Class 2 (Tested per JESD22-A114E) 3000V
Machine Model Class B (Tested per JESD22-A115-A) 300V
Charged Device Model Class IV. 1500V
Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. The ISL78420 is capable of derated operation at supply voltages exceeding 14V. Figure 17 shows the high-side voltage derating curve for this mode of operation.
6. All voltages referenced to V_{SS} unless otherwise specified.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
8. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{DD} = V_{HB} = 12V, V_{SS} = V_{HS} = 0V, R_{DT} = 0_K, PWM = 0V, No Load on LO or HO, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_A = +25°C			T_A = -40°C to +125°C		UNITS
			MIN	TYP	MAX	MIN (Note 9)	MAX (Note 9)	
SUPPLY CURRENTS								
V_{DD} Quiescent Current	I_{DD8k}	R_{DT} = 8k	-	650	950	-	**1000**	µA
	I_{DD80k}	R_{DT} = 80k	-	1.0	2.1	-	**2.2**	mA
V_{DD} Operating Current	I_{DDO8k}	f = 500kHz, R_{DT} = 8k	-	2.5	3	-	**3**	mA
	I_{DDO80k}	f = 500kHz, R_{DT} = 80k	-	3.4	4	-	**4**	mA
Total HB Quiescent Current	I_{HB}	LI = HI = 0V	-	65	115	-	**150**	µA
Total HB Operating Current	I_{HBO}	f = 500kHz	-	2.0	2.5	-	**3**	mA
HB to V_{SS} Current, Quiescent	I_{HBS}	LI = HI = 0V; V_{HB} = V_{HS} = 114V	-	0.05	1.5	-	**10**	µA
HB to V_{SS} Current, Operating	I_{HBSO}	f = 500kHz; V_{HB} = V_{HS} = 114V	-	1.2	1.5	-	**1.6**	mA
Tri-Level PWM Input								
High Level Threshold	V_{PWMH}		-	3.6	4.0	-	**4.3**	V
High Middle Level Threshold	V_{MIDH}		3.0	3.4	-	2.9	**-**	V
Low Middle Level Threshold	V_{MIDL}		-	1.6	2.1	-	**2.2**	V
Low Level Threshold	V_{PWML}		0.8	1.1	-	0.7	-	V
PWM Mid level Pull-up Resistors	R_{mid}		-	160	-	-	-	kΩ

Electrical Specifications

$V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, $R_{DT} = 0_K$, PWM = 0V, No Load on LO or HO, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_A = +25°C			T_A = -40°C to +125°C		UNITS
			MIN	TYP	MAX	MIN (Note 9)	MAX (Note 9)	
EN Input								
Low Level Input Threshold	V_{ENL}		1.4	1.8	-	**1.2**	-	V
High Level Input Threshold	V_{ENH}		-	1.8	2.2	-	**2.4**	V
EN Pull-up Resistance	R_{pu}		-	210	-	**100**	**320**	kΩ
UNDERVOLTAGE PROTECTION								
V_{DD} Rising Threshold	V_{DDR}		6.8	7.3	7.8	**6.5**	**8.1**	V
V_{DD} Threshold Hysteresis	V_{DDH}		-	0.6	-	-	-	V
HB Rising Threshold	V_{HBR}		6.2	6.9	7.5	**5.9**	**7.8**	V
HB Threshold Hysteresis	V_{HBH}		-	0.6	-	-	-	V
BOOTSTRAP DIODE								
Low Current Forward Voltage	V_{DL}	I_{VDD-HB} = 100mA	-	0.6	0.7	-	**0.8**	V
High Current Forward Voltage	V_{DH}	I_{VDD-HB} = 100mA	-	0.7	0.9	-	**1**	V
Dynamic Resistance	R_D	I_{VDD-HB} = 100mA	-	0.8	1	-	**1.5**	Ω
LO GATE DRIVER								
Low Level Output Voltage	V_{OLL}	I_{LO} = 100mA	-	0.25	0.4	-	**0.5**	V
High Level Output Voltage	V_{OHL}	I_{LO} = -100mA, $V_{OHL} = V_{DD} - V_{LO}$	-	0.25	0.4	-	**0.5**	V
Peak Pull-Up Current	I_{OHL}	V_{LO} = 0V	-	2	-	-	-	A
Peak Pull-Down Current	I_{OLL}	V_{LO} = 12V	-	2	-	-	-	A
HO GATE DRIVER								
Low Level Output Voltage	V_{OLH}	I_{HO} = 100mA	-	0.25	0.4	-	**0.5**	V
High Level Output Voltage	V_{OHH}	I_{HO} = -100mA, $V_{OHH} = V_{HB} - V_{HO}$	-	0.25	0.4	-	**0.5**	V
Peak Pull-Up Current	I_{OHH}	V_{HO} = 0V	-	2	-	-	-	A
Peak Pull-Down Current	I_{OLH}	V_{HO} = 12V	-	2	-	-	-	A

Switching Specifications

$V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, $R_{DT} = 0k\Omega$, No Load on LO or HO, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN	TYPE	MAX	MIN (Note 9)	MAX (Note 9)	
HO Turn-Off Propagation Delay PWM Falling to HO Falling	t_{PLHO}		-	32	50	-	**60**	ns
LO Turn-Off Propagation Delay PWM Rising to LO Falling	t_{PLLO}		-	32	50	-	**60**	ns
Minimum Dead-Time Delay (Note 10) HO Falling to LO Rising	$t_{DTHLmin}$	R_{DT} = 80k, PWM 1 to 0	15	35	50	**10**	**60**	ns
Minimum Dead-Time Delay (Note 10) LO Falling to HO Rising	$t_{DTLHmin}$	R_{DT} = 80k PWM 0 to 1	15	25	50	**10**	**60**	ns
Maximum Dead-Time Delay (Note 10) HO Falling to LO Rising	$t_{DTHLmax}$	R_{DT} = 8k, PWM 1 to 0	150	220	300	-	-	ns

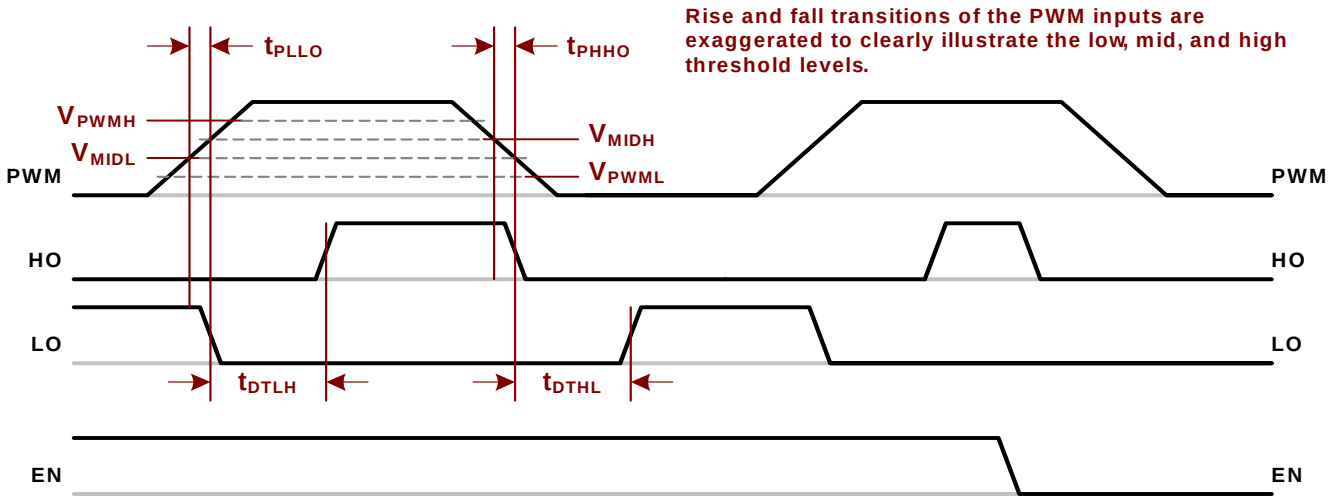
Switching Specifications $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, $R_{DT} = 0k\Omega$, No Load on LO or HO, Unless Otherwise Specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	T_J = +25°C			T_J = -40°C to +125°C		UNITS
			MIN	TYPE	MAX	MIN (Note 9)	MAX (Note 9)	
Maximum Dead-Time Delay (Note 10) LO Falling to HO Rising	$t_{DTLHmax}$	R_{DT} = 8k, PWM 0 to 1	150	220	300	-	-	ns
Either Output Rise/Fall Time (10% to 90%/90% to 10%)	t_{RC},t_{FC}	C_L = 1nF	-	10	-	-	-	ns
Bootstrap Diode Turn-On or Turn-Off Time	t_{BS}		-	10	-	-	-	ns

NOTES:

9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits are established by characterization and are not production tested.
10. Dead-Time is defined as the period of time between the LO falling and HO rising or between HO falling and LO rising.

Timing Diagram



Typical Performance Curves

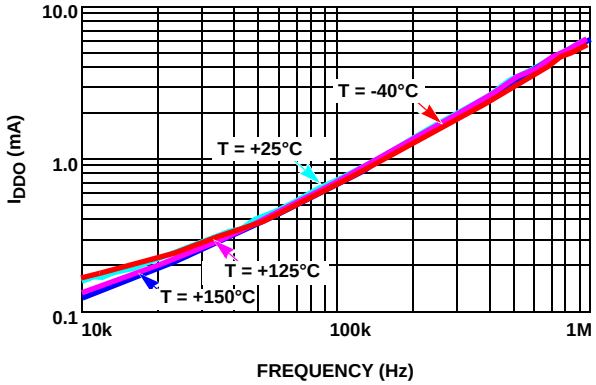


FIGURE 3. I_{DD} OPERATING CURRENT vs FREQUENCY, R_{DT} = 8K

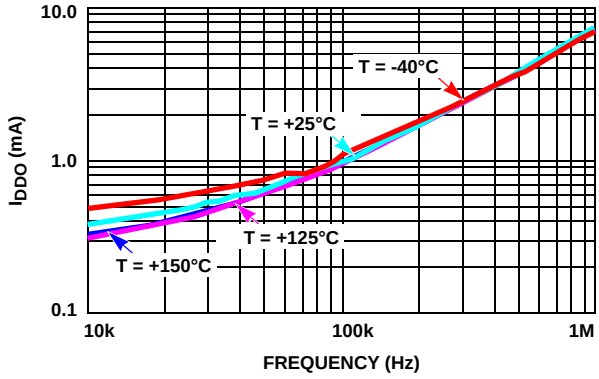


FIGURE 4. I_{DD} OPERATING CURRENT vs FREQUENCY, R_{DT} = 80k

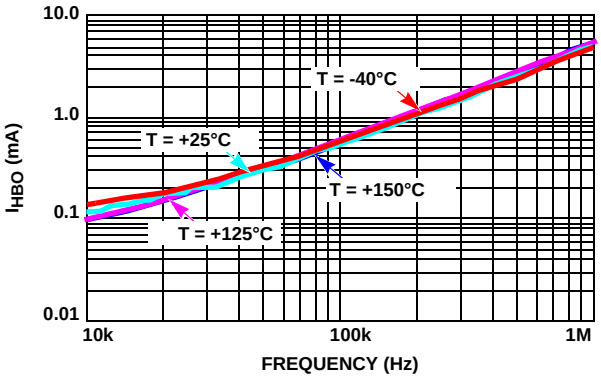


FIGURE 5. I_{HB} OPERATING CURRENT vs FREQUENCY, R_{DT} = 8k

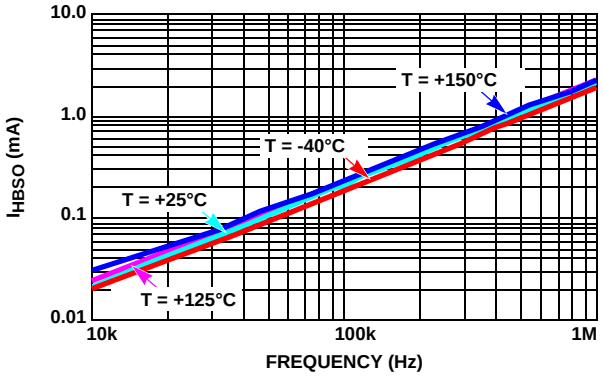


FIGURE 6. I_{HBS} OPERATING CURRENT vs FREQUENCY R_{DT} = 80k

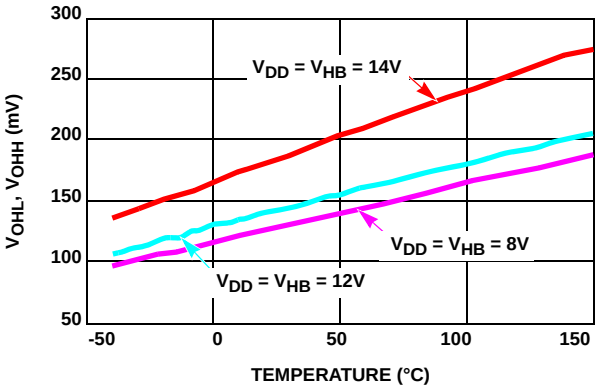


FIGURE 7. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

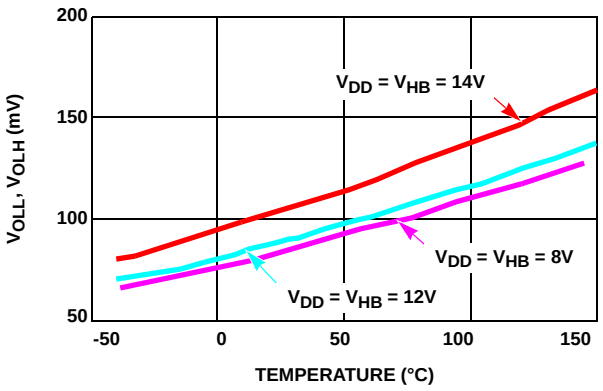


FIGURE 8. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

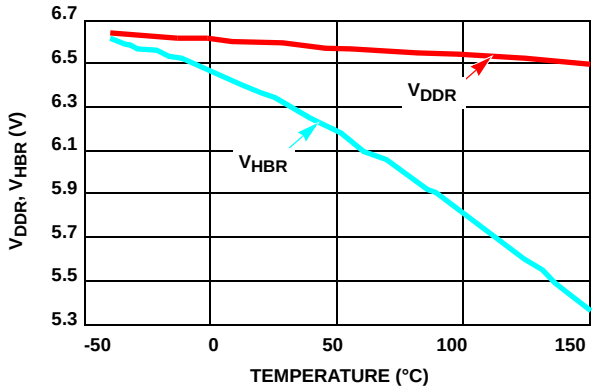


FIGURE 9. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

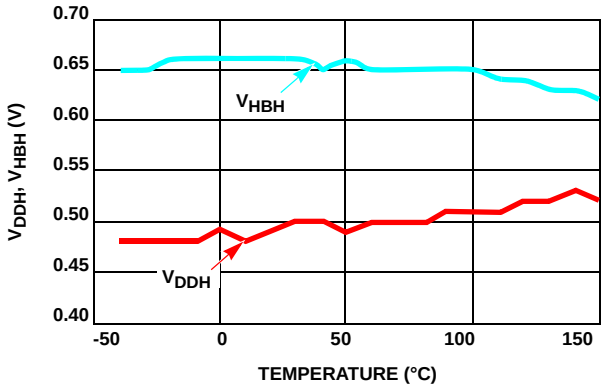


FIGURE 10. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE

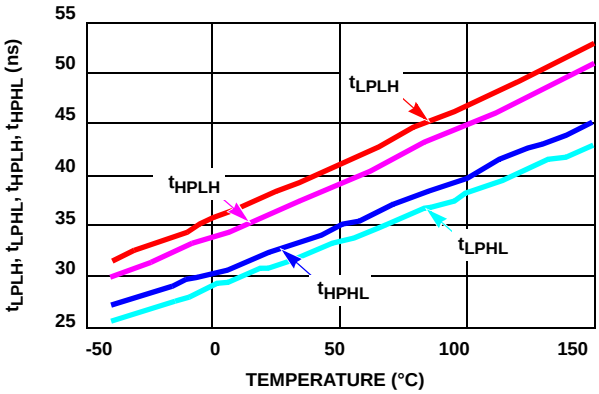


FIGURE 11. PROPAGATION DELAYS vs TEMPERATURE

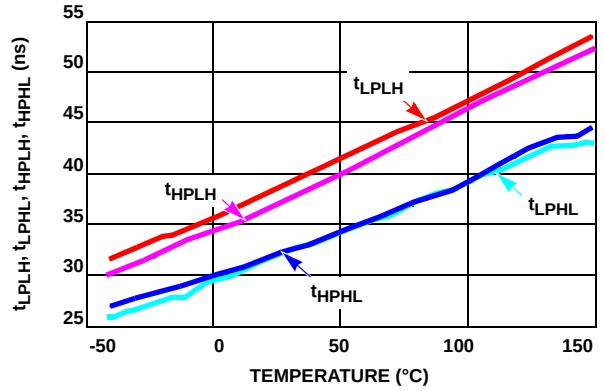


FIGURE 12. DELAY MATCHING vs TEMPERATURE

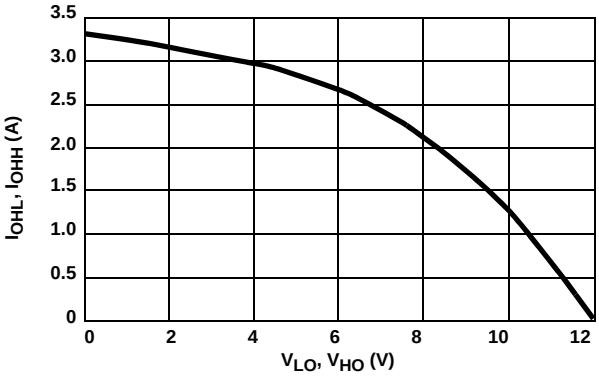


FIGURE 13. PEAK PULL-UP CURRENT vs OUTPUT VOLTAGE

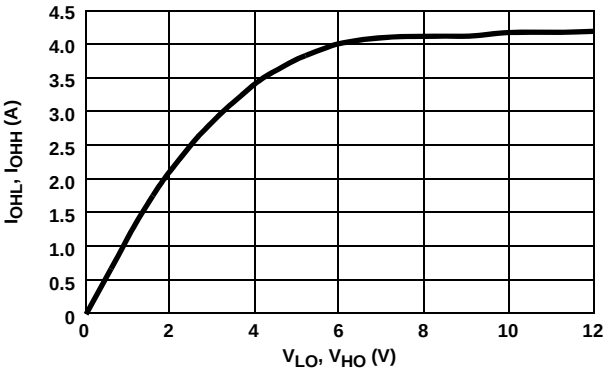


FIGURE 14. PEAK PULL-DOWN CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

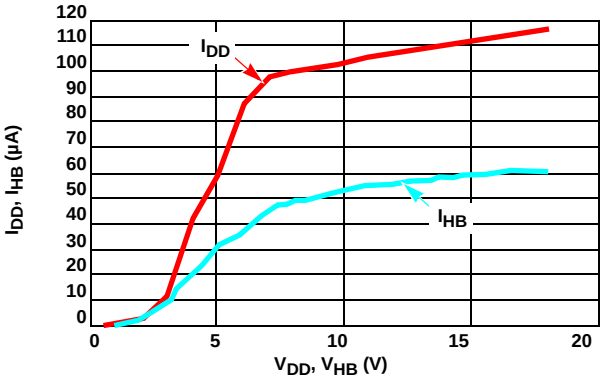


FIGURE 15. QUIESCENT CURRENT vs VOLTAGE

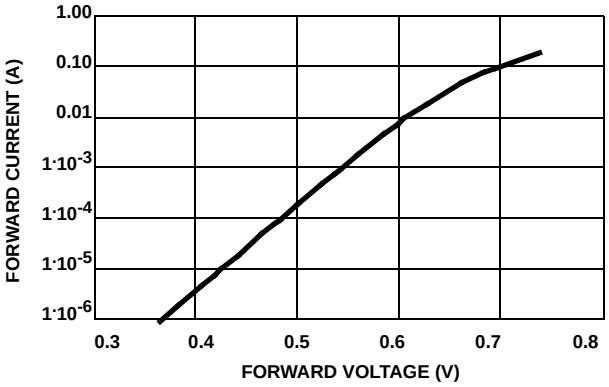


FIGURE 16. BOOTSTRAP DIODE I-V CHARACTERISTICS

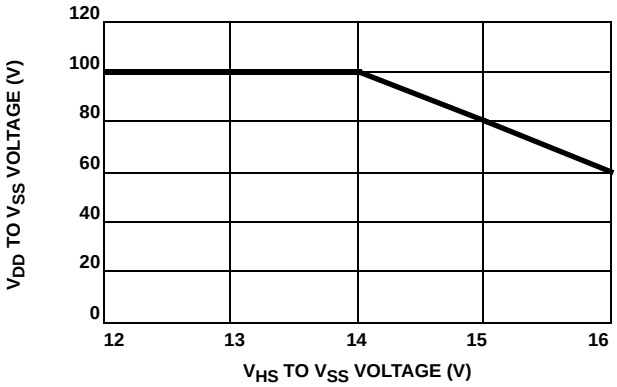


FIGURE 17. V_{HS} VOLTAGE vs V_{DD} VOLTAGE

Functional Description

Functional Overview

When connected to a half bridge, the output of the bridge on the HS node follows the PWM input. In other words, when the PWM input is high, the high-side bridge FET is turned on and the low-side FET is off. When the PWM input is low, the low-side bridge FET is turned on and the high-side is turned off. The enable pin (EN), when low, drives both outputs to a low state.

A unique feature of the ISL78420 is the tri-level logic of the PWM input. The logic thresholds of the PWM input is divided into 3 levels. A logic low ensures that the output of the low-side bridge FET is on and the high-side FET is off. A logic high ensures that the high-side bridge FET is on and the low-side FET is off. When the logic input is midrange (2.5V), both the high and low side FETs are off. This driver is designed to work in conjunction with the ISL78220, “6-Phase Interleaved Boost PWM Controller with Light Load Efficiency Enhancement”.

When the PWM input transitions high or low, it is necessary to ensure that both bridge FETS are not on at the same time to prevent shoot-through currents (break before make). The internal programmable timers delay the rising edge of either output resulting with both outputs being off before either of the bridge FETs are driven on. An 8kΩ resistor connected between R_{DT} and VSS results in a nominal dead time of 220ns. An 80kΩ results with a minimum nominal dead time of 25ns. Resistors values less than 8k and greater than 80k are not recommended.

While the voltage of the input signal to the PWM is within the boundaries of the mid-level logic, the outputs are in a dead time state because both outputs are off. The actual delay time, as programed by the R_{DT} value, begins when the high or low logic levels are transitioned. The period while the input logic in the mid-level range, is consequently added to the programmed dead time period. This may be a consideration when selecting the R_{DT} value.

The high-side driver bias is established by the boot capacitor connected between HB and HS. The charge on the boot capacitor is provided by the internal boot diode that is connected to VDD. The current path to charge the boot capacitor occurs when the low-side bridge FET is on. This charge current is limited in amplitude by the inherent resistance of the boot diode and by the drain-source voltage of the low-side FET. Assuming that the on time of the low-side FET is sufficiently long to fully charge the boot capacitor, the boot voltage will charge very close to VDD (less the boot diode drop and the on-voltage of the low-side bridge FET).

When the PWM input transitions high, the high-side bridge FET is driven on after the dead time. Because the HS node is connected

to the source of the high-side FET, the HS node will rise almost to the level of the bridge voltage (less the conduction voltage across the bridge FET). Because the boot capacitor voltage is referenced to the source voltage of the high-side FET, the HB node is V_{DD} volts above the HS node and the boot diode is reversed biased. Because the high-side driver circuit is referenced to the HS node, the HO output is now approximately VHB + VBRIDGE above ground.

During the low to high transition of the HS node, the boot capacitor sources the necessary gate charge to fully enhance the high-side bridge FET gate. After the gate is fully charged, the boot capacitor no longer sources the charge to the gate but continues to provide bias current to the high-side driver. It is clear that the charge of the boot capacitor must be substantially larger than the required charge of the high-side FET and high-side driver otherwise the boot voltage will sag excessively. If the boot capacitor value is too small for the required maximum of on-time of the high-side FET, the high-side UV lockout may engage resulting with an unexpected operation.

Application Information

Selecting the Boot Capacitor Value

The boot capacitor value is chosen not only to supply the internal bias current of the high-side driver but also, and more significantly, to provide the gate charge of the driven FET without causing the boot voltage to sag excessively. In practice, the boot capacitor should have a total charge that is approximately 20x the gate charge of the driven power FET for a 5% drop in voltage after the charge has been transferred from the boot capacitor to the gate capacitance.

The following parameters are required to calculate the value of the boot capacitor for a specific amount of voltage droop. In this example, the values used are arbitrary. They should be changed to comply with the actual application.

V_{DD} = 10V	V_{DD} can be any value between 7 and 14VDC
$V_{HB} = V_{DD} - 0.6V = V_{HO}$	High side driver bias voltage (V_{DD} - boot diode voltage) referenced to V_{HS}
Period = 1ms	This is the longest expected switching period
I_{HB} = 100µA	Worst case high side driver current when xHO = high (this value is specified for V_{DD} = 12V but the error is not significant)
R_{GS} = 100kΩ	Gate-source resistor (usually not needed)
Ripple= 5%	Desired ripple voltage on the boot cap (larger ripple is not recommended)
I_{gate_leak} = 100nA	From the FET vendor's datasheet
Qgate80V = 64nC	From Figure 18

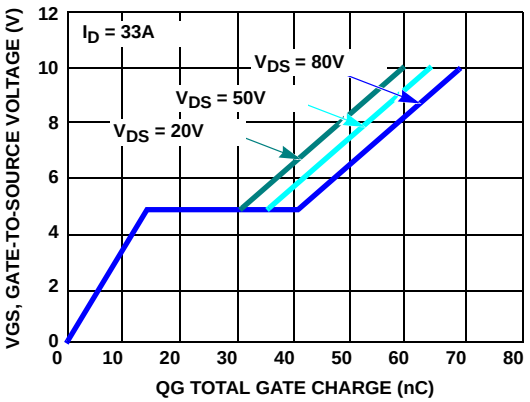


FIGURE 18. TYPICAL GATE CHARGE OF A POWER FET

The following equations calculate the total charge required for the Period. These equations assume that all of the parameters are constant during the period duration. The error is insignificant if the ripple is small.

$$Q_C = Q_{gate80V} + Period \times I_{HB} + V_{HO}/(R_{GS} + I_{gate_leak}) \quad \text{(EQ. 1)}$$

$$C_{boot} = Q_C/(Ripple*VDD) \quad \text{(EQ. 2)}$$

$$C_{boot} = 0.52\mu F$$

If the gate to source resistor is removed (R_{GS} is usually not needed or recommended), then:

C_{boot} = 0.33µF

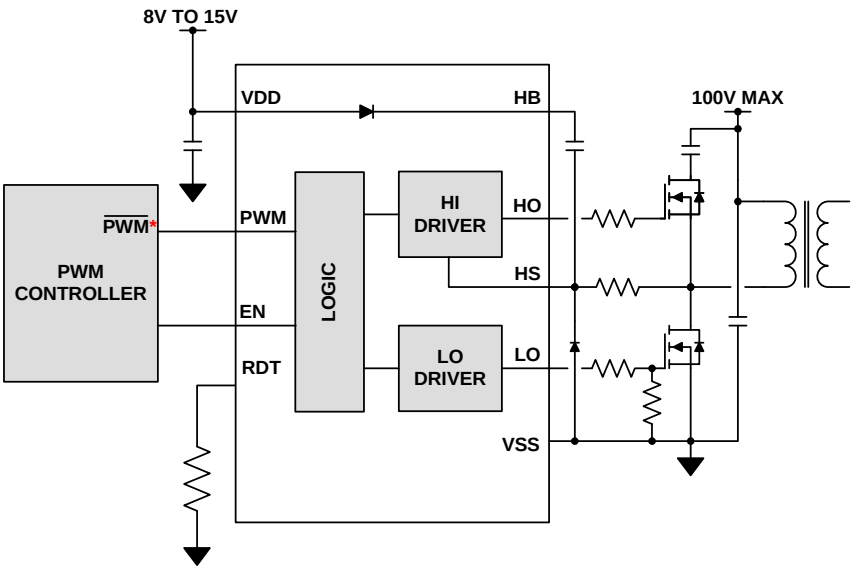


FIGURE 19. TYPICAL ACTIVE CLAMP FORWARD APPLICATION

Typical Application Circuit

Figure 19 is an example of how the ISL78420 can be configured for an active clamp forward power supply application. Note that the PWM signal from the controller must be inverted for this active clamp forward topology.

Depending on the application, the switching speed of the bridge FETs can be reduced by adding series connected resistors between the xHO outputs and the FET gates. Gate-Source resistors are recommended on the low-side FETs to prevent unexpected turn-on of the bridge should the bridge voltage be applied before VDD. Gate-source resistors on the high-side FETs are not usually required if low-side gate-source resistors are used. If relatively low value gate-source resistors are used on the high-side FETs, be aware that a larger value for the boot capacitor may be required.

Transients on HS Node

An important operating condition that is frequently overlooked by designers is the negative transient on the xHS pins that occurs when the high-side bridge FET turns off. The Absolute Maximum transient allowed on the xHS pin is -6V but it is wise to minimize the amplitude to lower levels. This transient is the result of the parasitic inductance of the low-side drain-source conductor on the PCB. Even the parasitic inductance of the low-side FET contributes to this transient.

When the high-side bridge FET turns off (see Figure 20), because of the inductive characteristics the load, the current that was flowing in the high-side FET (blue) must rapidly commutate to flow through the low-side FET (red). The amplitude of the negative transient impressed on the xHS node is (di/dt x L) where L is the total parasitic inductance of the low-side FET drain-source path and di/dt is the rate at which the high-side FET is turned off. With the increasing power levels of power supplies and motors, clamping this transient become more and more significant for the proper operation of the ISL78420.

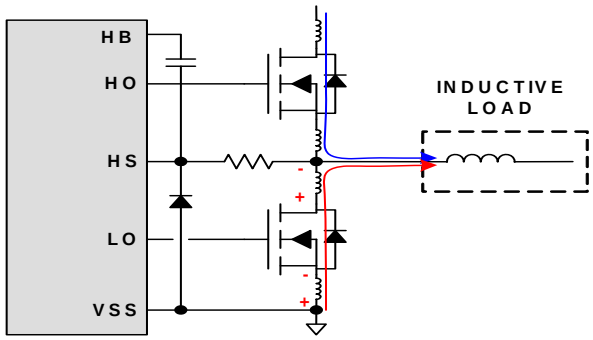


FIGURE 20. PARASITIC INDUCTANCE CAUSES TRANSIENTS ON HS NODE

There are several ways of reducing the amplitude of this transient. If the bridge FETs are turned off more slowly to reduce di/dt, the amplitude will be reduced but at the expense of more switching losses in the FETs. Careful PCB design will also reduce the value of the parasitic inductance. However, these two solutions by themselves may not be sufficient. Figure 20 illustrates a simple method for clamping the negative transient. A fast PN junction, 1A diode is connected between xHS and VSS as shown. It is important that this diode be placed as close as possible to the xHS and VSS pins to minimize the parasitic inductance of this current path. Because this clamping diode is essentially in parallel with the body diode of the low-side FET, a small value resistor is necessary to limit current when the body diode of the low-side bridge FET is conducting during the dead time. The resistor in series with HS, can be used instead of the gate resistor of the high-side FET.

Please note that a similar transient with a positive polarity occurs when the low-side FET turns off. This is less frequently a problem because xHS node is floating up toward the bridge bias voltage. The Absolute Max voltage rating for the xHS node does need to be observed when the positive transient occurs.

Power Dissipation

The dissipation of the ISL78420 is dominated by the gate charge required by the driven bridge FETs and the switching frequency. The internal bias and boot diode also contribute to the total dissipation but these losses are usually insignificant compared to the gate charge losses.

The calculation of the power dissipation of the ISL78420 is very simple.

GATE POWER (FOR THE HO AND LO OUTPUTS)

$$P_{gate} = 4 \times Q_{gate} \times Freq \times VDD \quad \text{(EQ. 3)}$$

where

Q_{gate} is the charge of the driven bridge FET at VDD, and

Freq is the switching frequency.

BOOT DIODE DISSIPATION

$$I_{diode_avg} = Q_{gate} \times Freq \quad \text{(EQ. 4)}$$

$$P_{diode} = I_{diode_avg} \times 0.6V \quad \text{(EQ. 5)}$$

where 0.6V is the diode conduction voltage

BIAS CURRENT

$$P_{bias} = I_{bias} \times VDD \quad \text{(EQ. 6)}$$

where I_{bias} is the internal bias current of the ISL78420 at the switching frequency

TOTAL POWER DISSIPATION

$P_{total} = P_{gate} + P_{diode} + P_{bias}$

OPERATING TEMPERATURES

$T_j = P_{total} \times \theta_{JA} + T_{amb}$

where T_j is the junction temperature at the operating air temperature, T_{amb}, in the vicinity of the part.

$T_j = P_{total} \times \theta_{JC} + T_{PCB}$

where T_j is the junction temperature with the operating temperature of the PCB, T_{PCB}, as measured where the EPAD is soldered.

PC Board Layout

The AC performance of the ISL78420 depends significantly on the design of the PC board. The following layout design guidelines are recommended to achieve optimum performance from the ISL78420:

- Understand well how power currents flow. The high amplitude di/dt currents of the bridge FETs will induce significant voltage transients on the associated traces.
- Keep power loops as short as possible by paralleling the source and return traces.
- Use planes where practical; they're usually more effective than parallel traces.
- Planes can also be non-grounded nodes.
- Avoid paralleling high di/dt traces with low level signal lines. High di/dt will induce currents in the low level signal lines.
- When practical, minimize impedances in low level signal circuits; the noise, magnetically induced on a 10k resistor, is 10x larger than the noise on a 1k resistor.
- Be aware of magnetic fields emanating from transformers and inductors. Core gaps in these structures are especially bad for emitting flux.
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines.
- The use of low inductance components such as chip resistors and chip capacitors is recommended.
- Use decoupling capacitors to reduce the influence of parasitic inductors. To be effective, these capacitors must also have the shortest possible lead lengths. If vias are used, connect several paralleled vias to reduce the inductance of the vias.
- It may be necessary to add resistance to dampen resonating parasitic circuits. In PCB designs with long leads on the LO and HO outputs, it may be necessary to add series gate resistors on the bridge FETs to dampen the oscillations.
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for the PWM control circuits.
- Avoid having a signal ground plane under a high dv/dt circuit. This will inject high di/dt currents into the signal ground paths.
- Do power dissipation and voltage drop calculations of the power traces. Most PCB/CAD programs have built in tools for calculation of trace resistance.
- Large power components (Power FETs, Electrolytic capacitors, power resistors, etc.) will have internal parasitic inductance, which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components.

EPAD Design Considerations

The thermal pad of the ISL78420 is electrically isolated. It's primary function is to provide heat sinking for the IC. It is recommended to tie the EPAD to V_{SS} (GND).

Figure 21 is an example of how to use vias to remove heat from the IC substrate. Depending on the amount of power dissipated by the ISL78420, it may be necessary, to connect the EPAD to one or more ground plane layers. A via array, within the area of the EPAD, will conduct heat from the EPAD to the ground plane on the bottom layer. If inner PCB layers are available, it is also be desirable to connect these additional layers with the plated-through vias.

The number of vias and the size of the GND planes required for adequate heatsinking is determined by the power dissipated by the ISL78420, the air flow, and the maximum temperature of the air around the IC.

It is important that the vias have a low thermal resistance for efficient heat transfer. Do not use "thermal relief" patterns to connect the vias.

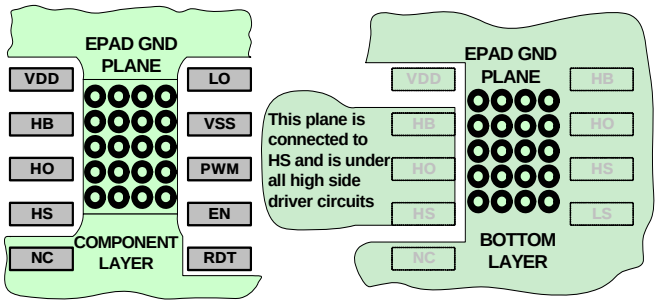


FIGURE 21. RECOMENDED PCB HEATSINK

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
September 24, 2012	FN8296.1	Initial Release

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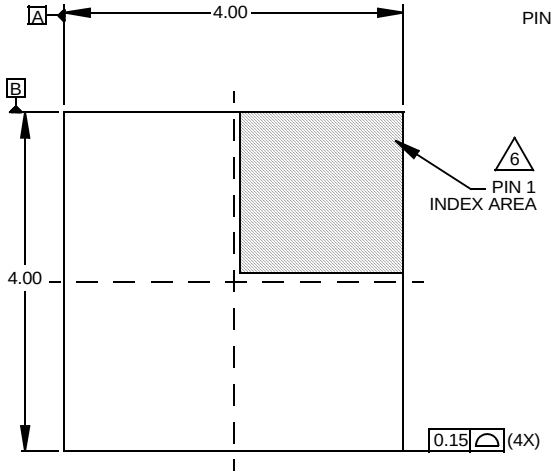
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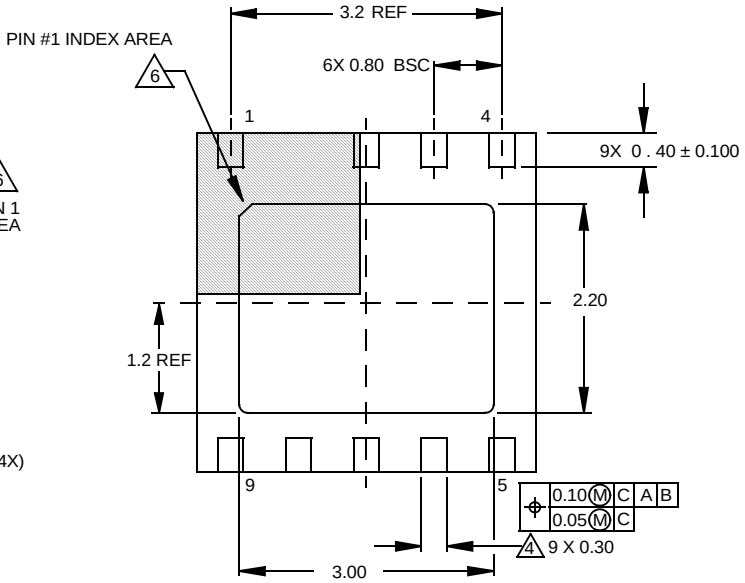
Package Outline Drawing

L9.4x4

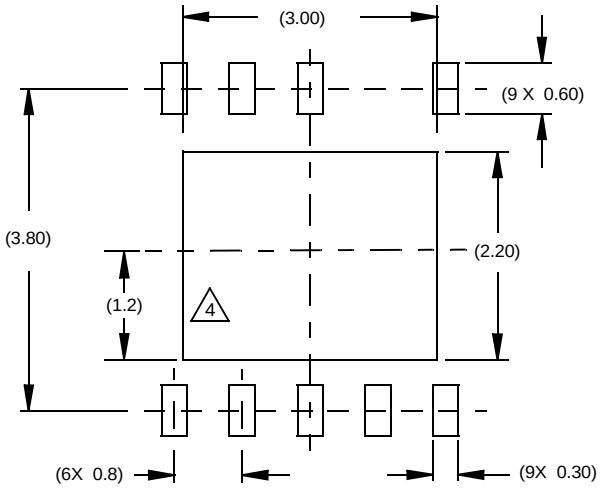
9 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 1/10



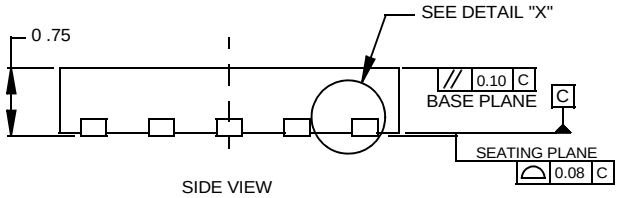
TOP VIEW



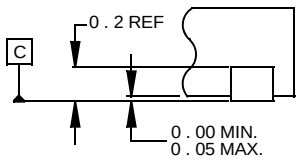
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

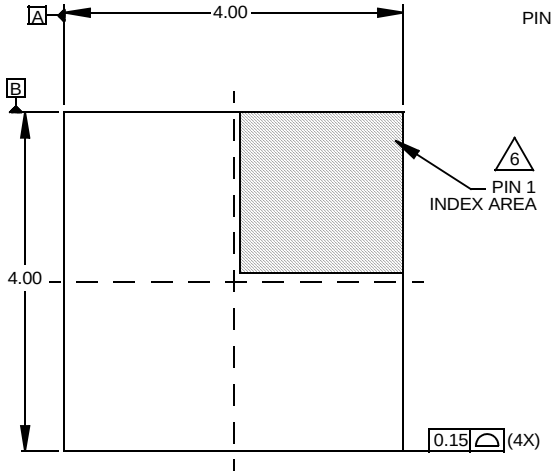
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. E-Pad is offset from center.
5. Tiebar (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

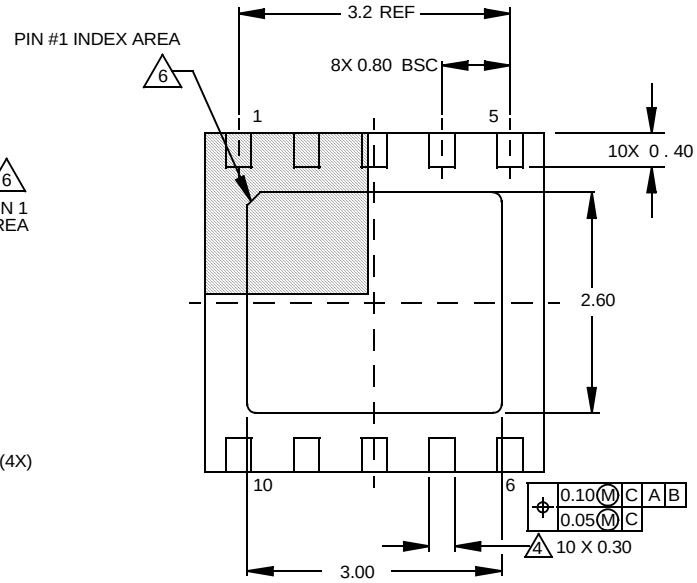
Package Outline Drawing

L10.4x4

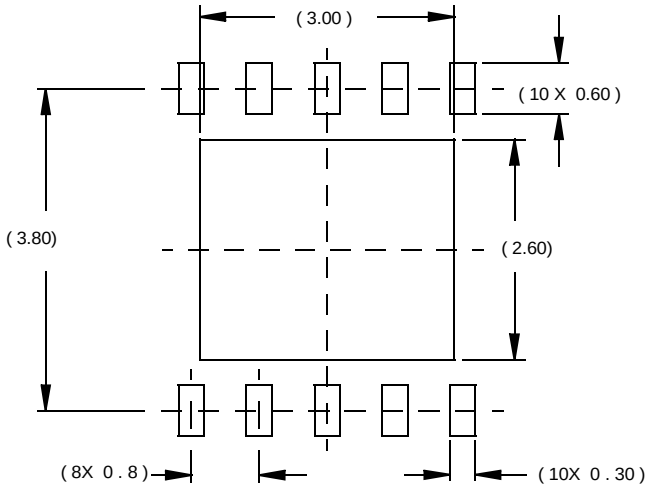
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 1/08



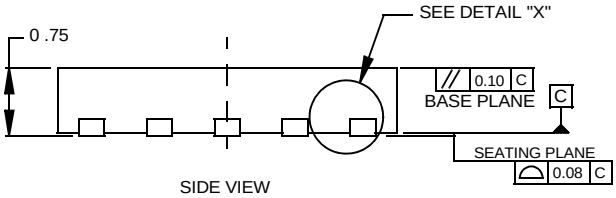
TOP VIEW



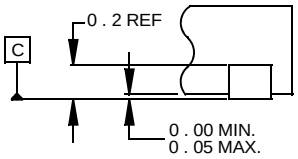
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.