Ordering number : EN5731A

CMOS IC

LC74788, 74788M, 74788JM

On-Screen Display Controller

Overview

The LC74788, LC74788M, and LC74788JM are on-screen display controller CMOS ICs that display characters and patterns on the TV screen under microprocessor control. These ICs support 12 × 18 dot characters and can display 12 lines by 24 characters of text.

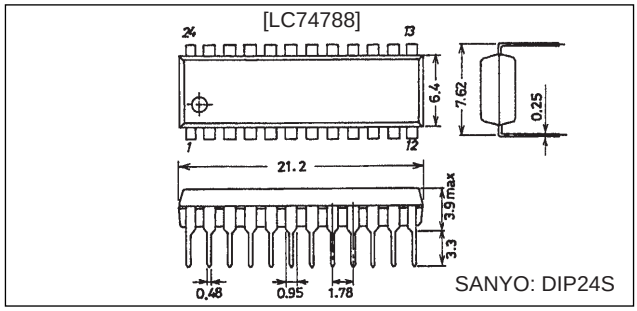
Features

- Display format: 24 characters by 12 rows (Up to 288 characters)
- Character format: 12 (horizontal) × 18 (vertical) dots
- Character sizes: Three sizes each in the horizontal and vertical directions
- Characters in font: 128 (128 characters, one spacing character, and one transparent spacing character)
- Initial display positions: 64 horizontal positions and 64 vertical positions
- Blinking: Specifiable in character units
- Blinking types: Two periods supported: About 1.0 second and about 0.5 second
- Blanking: Over the whole font (12 × 18 dots)
- Background color: 8 colors (internal synchronization mode): $2f_{SC}$ and $4f_{SC}$
- Line background color
  - — Can be set for 3 lines
  - — Line background color: 8 colors (internal synchronization mode): $2f_{SC}$ and $4f_{SC}$
- External control input: 8-bit serial input format
- On-chip sync separator circuit
- Video outputs - NTSC, PAL, PAL-N, PAL-M, NTSC 4.43, and PAL60 format composite video outputs
- Package
  - — 24-pin plastic DIP-24S (300 mil)
  - — 24-pin plastic MFP-24 (375 mil)
  - — 24-pin plastic MFP-24S (300 mil)

Package Dimensions

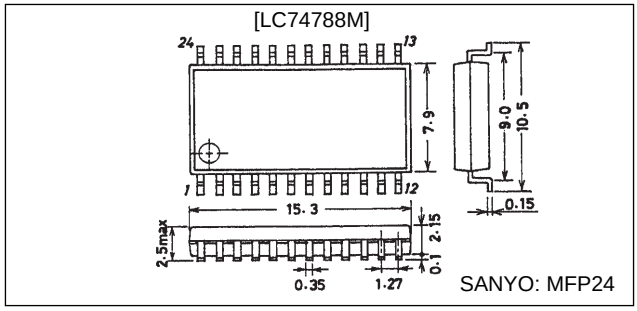
unit: mm

3067-DIP24S



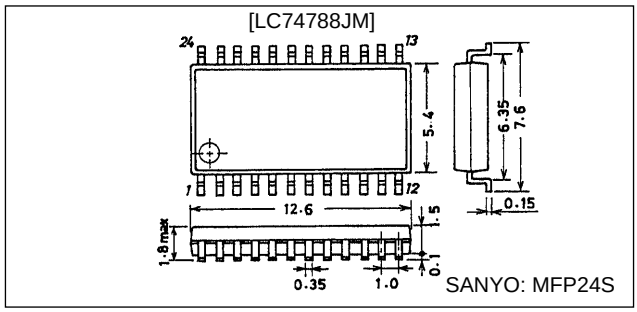
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3045B-MFP24



unit: mm

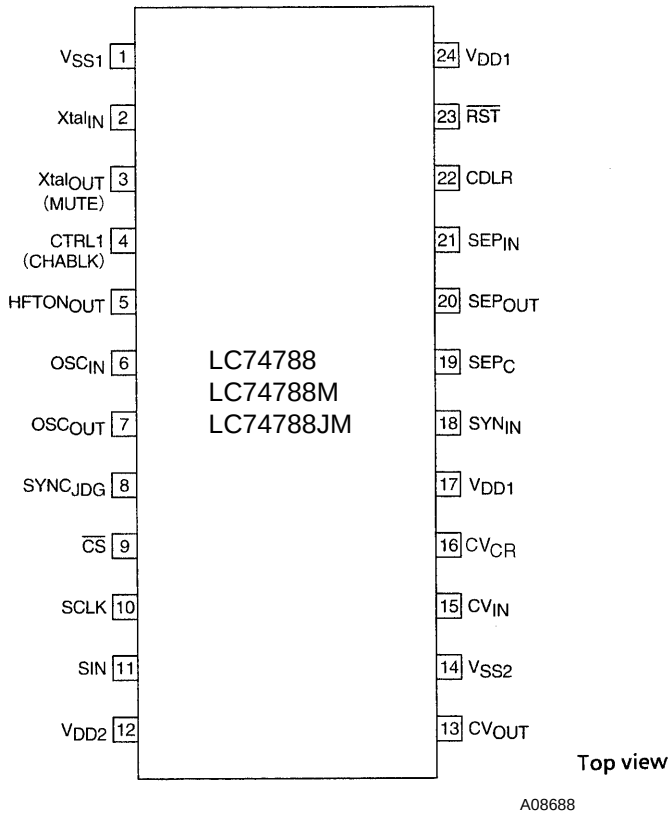
3112-MFP24S



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Pin Assignment



Pin Functions

Pin no.	Pin	Function	Notes
1	$V_{SS}1$	Ground	Ground connection (digital system ground)
2	$Xtal_{IN}$	Crystal oscillator (MUTE input)	These pins are used either to connect the crystal and capacitors used to form an external crystal oscillator circuit to generate the internal synchronizing signals, or to input an external clock signal (2fsc or 4fsc). As a mask option, the XtalOUT pin can be set to function as the MUTE input pin. When this pin is set low, the video output is held at the pedestal level. (A pull-up resistor is built in and the input has hysteresis characteristics.)
3	$Xtal_{OUT}$ (MUTE)		
4	CTRL1 (CHABLK)	Crystal oscillator input switching (CHABLK output)	Switches the mode between external clock input and crystal oscillator operation. A low level selects crystal oscillator operation and a high level selects external clock input. As a mask option, the CTRL1 input pin can be set to function as the CHABLK (character · frame) output. This is a 3-value output.
5	$HFTON_{OUT}$	Background line output	Outputs the range signal specified by LNA*, LNB*, and LNC*. Outputs the crystal oscillator clock when RST is low. (This signal is not output after a reset command is executed.)
6	OSC_{IN}	LC oscillator	Connections for the inductor and capacitor that form the character output dot clock generation oscillator.
7	OSC_{OUT}		
8	$SYNC_{JDG}$	External synchronizing signal judgment output	Outputs the state of the external synchronizing signal presence/absence judgment. Outputs a high level when synchronizing signals are present. Outputs the dot clock (LC oscillator) when RST is low. (This signal is not output on command resets.)
9	$\overline{CS}$	Enable input	Serial data input circuit enable pin. Serial data input is enabled when a low level is input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
10	SCLK	Clock input	Serial data input circuit clock input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
11	SIN	Data input	Serial data input. A pull-up resistor is built in. (This input has hysteresis characteristics.)
12	$V_{DD}2$	Power supply	Composite video signal level adjustment power supply (analog system power supply)

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Pin no.	Pin	Function	Notes
13	CV_{OUT}	Video signal output	Composite video signal output
14	$V_{SS}2$	Ground	Ground connection (analog system ground)
15	CV_{IN}	Video signal input	Composite video signal input
16	CV_{CR}	Video signal input	SECAM chrominance signal input
17	$V_{DD}1$	Power supply	Power supply (+5 V: digital system power supply)
18	SYN_{IN}	Sync separator circuit input	Video signal input to the internal sync separator circuit (Used as either the horizontal synchronizing signal or the composite synchronizing signal input when the internal sync separator circuit is not used.)
19	SEP_C	Sync separator circuit bias voltage	Internal sync separator circuit bias voltage monitor
20	SEP_{OUT}	Composite synchronizing signal output	Internal sync separator circuit composite synchronizing signal output. Can be switched to function as a signal (high, low, or ST. pulse) output by the SEL0 and MOD0 setting.
21	SEP_{IN}	Vertical synchronizing signal input	Inputs the vertical synchronizing signal created by integrating the SEP_{OUT} pin output signal. An integration circuit must be connected to the SEP_{OUT} pin. This pin must be tied to $V_{DD}1$ if unused. This pin can be switched to function as the frame signal input mode by setting SEL1 high. This is valid when CTL3 is set high. This input has hysteresis characteristics.
22	CDLR	Background color phase adjustment	Background color phase adjustment. Connect a resistor between this pin and ground.
23	$\overline{RST}$	Reset input	System reset input A pull-up resistor is built in and the input has hysteresis characteristics.
24	$V_{DD}1$	Power supply (+5 V)	Power supply (+5 V: digital system power supply)

Note: Both $V_{DD}1$ pins must be connected to the power supply.

Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max	$V_{DD}1$ and $V_{DD}2$	V_{SS}–0.3 to V_{SS}+6.5	V
Maximum input voltage	V_{IN} max	All input pins	V_{SS}–0.3 to V_{DD}+0.3	V
Maximum output voltage	V_{OUT} max	$HFTON_{OUT}$, $SYNC_{JDG}$, and SEP_{OUT}	V_{SS}–0.3 to V_{DD}+0.3	V
Allowable power dissipation	Pd max	Ta = 25°C	350	mW
Operating temperature	Topr		–30 to +70	°C
Storage temperature	Tstg		–40 to +125	°C

Allowable Operating Ranges

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	$V_{DD}1$	$V_{DD}1$	4.5	5.0	5.5	V
	$V_{DD}2$	$V_{DD}2$	4.5	5.0	$1.27V_{DD}1$	V
Input high-level voltage	$V_{IH}1$	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, SEP_{IN}, and MUTE	$0.8V_{DD}1$		$V_{DD}1$+0.3	V
	$V_{IH}2$	CTRL1	$0.7V_{DD}1$		$V_{DD}1$+0.3	V
Input low-level voltage	$V_{IL}1$	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, SEP_{IN}, and MUTE	V_{SS}–0.3		$0.2V_{DD}1$	V
	$V_{IL}2$	CTRL1	V_{SS}–0.3		$0.3V_{DD}1$	V
Pull-up resistance	R_{PU}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, and MUTE Applies to pins set up by options.	25	50	90	kΩ
Composite video signal input voltage	$V_{IN}1$	CV_{IN}: $V_{DD}1$ = 5 V		2.0		Vp-p
	$V_{IN}2$	SYN_{IN}: $V_{DD}1$ = 5 V		2.0	2.5	Vp-p
	$V_{IN}3$	CV_{CR}: $V_{DD}1$ = 5 V		2.0		Vp-p
Input voltage	$V_{IN}4$	$Xtal_{IN}$ (when used for external clock input) f_{IN} = 2fsc or 4fsc ; $V_{DD}1$ = 5 V	0.10		5.0	Vp-p
Oscillator frequencies	$F_{OSC}1$	$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (2fsc: NTSC)		7.159		MHz
		$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (4fsc: NTSC)		14.318		MHz
		$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (2fsc: PAL)		8.867		MHz
		$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (4fsc: PAL)		17.734		MHz
		$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (2fsc: PAL-M)		7.151		MHz
		$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (4fsc: PAL-M)		14.302		MHz
		$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (2fsc: PAL-N)		7.164		MHz
		$Xtal_{IN}$ and $Xtal_{OUT}$ oscillator pins (4fsc: PAL-N)		14.328		MHz
	$F_{OSC}2$	OSC_{IN} and OSC_{OUT} oscillator pins (LC oscillator)	5		10	MHz

Note: Applications must be especially cautious about noise when using the $Xtal_{IN}$ input pin in clock input mode.

Electrical Characteristics at Ta = –30 to +70°C. $V_{DD}1$ = 5 V unless otherwise specified.

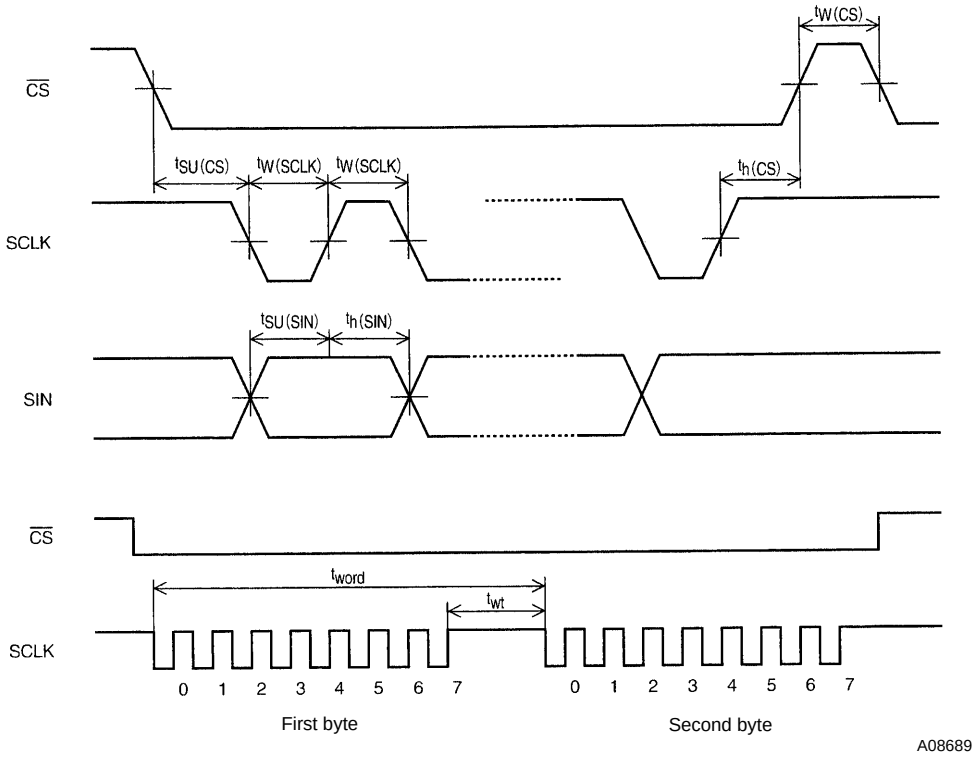
Parameter	Symbol	Pin	Conditions		Ratings min	Ratings typ	Ratings max	Unit
Input off leakage current	I_{leak1}	CV_{IN} and CV_{CR}					1	µA
Output off leakage current	I_{leak2}	CV_{OUT}					1	µA
Output high-level voltage	V_{OH1}	$HFTON_{OUT}$, $SYNC_{JDG}$, and SEP_{OUT}	$V_{DD}1$ = 4.5 V, I_{OH} = –1.0 mA		3.5			V
Output low-level voltage	$V_{OL}1$	$HFTON_{OUT}$, $SYNC_{JDG}$, and SEP_{OUT}	$V_{DD}1$ = 4.5 V, I_{OL} = –1.0 mA				1.0	V
Three-value output voltage	V_O	CHABLK	$V_{DD}1$ = 5.0 V	H	3.3		5.0	V
				M	1.8		2.3	V
				L	0		0.8	V
Input current	I_{IH}	$\overline{RST}$, $\overline{CS}$, SIN, SCLK, CTRL1, SEP_{IN}, and MUTE	V_{IN} = $V_{DD}1$				1	µA
	I_{IL}	CTRL1 and OSC_{IN}	V_{IN} = $V_{SS}1$		–1			µA
Operating mode current drain	$I_{DD}1$	$V_{DD}1$	All outputs: open Xtal:7.159 MHz LC:8 MHz				15	mA
	$I_{DD}2$	$V_{DD}2$	$V_{DD}2$ = 5 V				20	mA
SYNC level	V_{SN}	CV_{OUT} (1): When the sync level = 0.8 V (2): When the sync level = 1.0 V (3): When the sync level = 1.3 V	$V_{DD}1$ = 5.0 V $V_{DD}2$ = 5.0 V	(1)	0.70	0.82	0.94	V
				(2)	0.89	1.01	1.13	
				(3)	1.18	1.30	1.42	
Pedestal level	V_{PD}			(1)	1.32	1.44	1.56	V
				(2)	1.52	1.64	1.76	
				(3)	1.81	1.93	2.05	
Color burst low level	V_{CBL}			(1)	0.98	1.10	1.22	V
				(2)	1.17	1.29	1.41	
				(3)	1.46	1.58	1.70	
Color burst high level	V_{CBH}			(1)	1.63	1.75	1.87	V
				(2)	1.83	1.95	2.07	
				(3)	2.11	2.23	2.35	
Background color low level (other than blue)	$V_{RSL}0$			(1)	1.17	1.29	1.41	V
				(2)	1.36	1.48	1.60	
				(3)	1.65	1.77	1.89	
Background color high level (other than blue)	$V_{RSH}0$			(1)	2.33	2.45	2.57	V
				(2)	2.52	2.64	2.76	
				(3)	2.81	2.93	3.05	
Blue background 1 low level	$V_{RSL}1$			(1)	1.08	1.20	1.32	V
				(2)	1.27	1.39	1.51	
				(3)	1.56	1.68	1.80	
Blue background 2 low level	$V_{RSL}2$			(1)	1.49	1.61	1.83	V
				(2)	1.68	1.80	1.92	
				(3)	1.97	2.09	2.21	
Blue background 1 and 2 high level	$V_{RSH}1$, 2			(1)	1.97	2.09	2.21	V
				(2)	2.17	2.29	2.41	
				(3)	2.46	2.58	2.70	
Frame level 0	$V_{BK}0$			(1)	1.40	1.52	1.64	V
				(2)	1.60	1.72	1.84	
				(3)	1.89	2.01	2.13	
Frame level 1	$V_{BK}1$			(1)	1.97	2.09	2.21	V
				(2)	2.17	2.29	2.41	
				(3)	2.46	2.58	2.70	
Character level	V_{CHA}			(1)	2.55	2.67	2.79	V
				(2)	2.75	2.87	2.99	
				(3)	3.04	3.16	3.28	

Note: Blue background 1 or 2 are option settings.

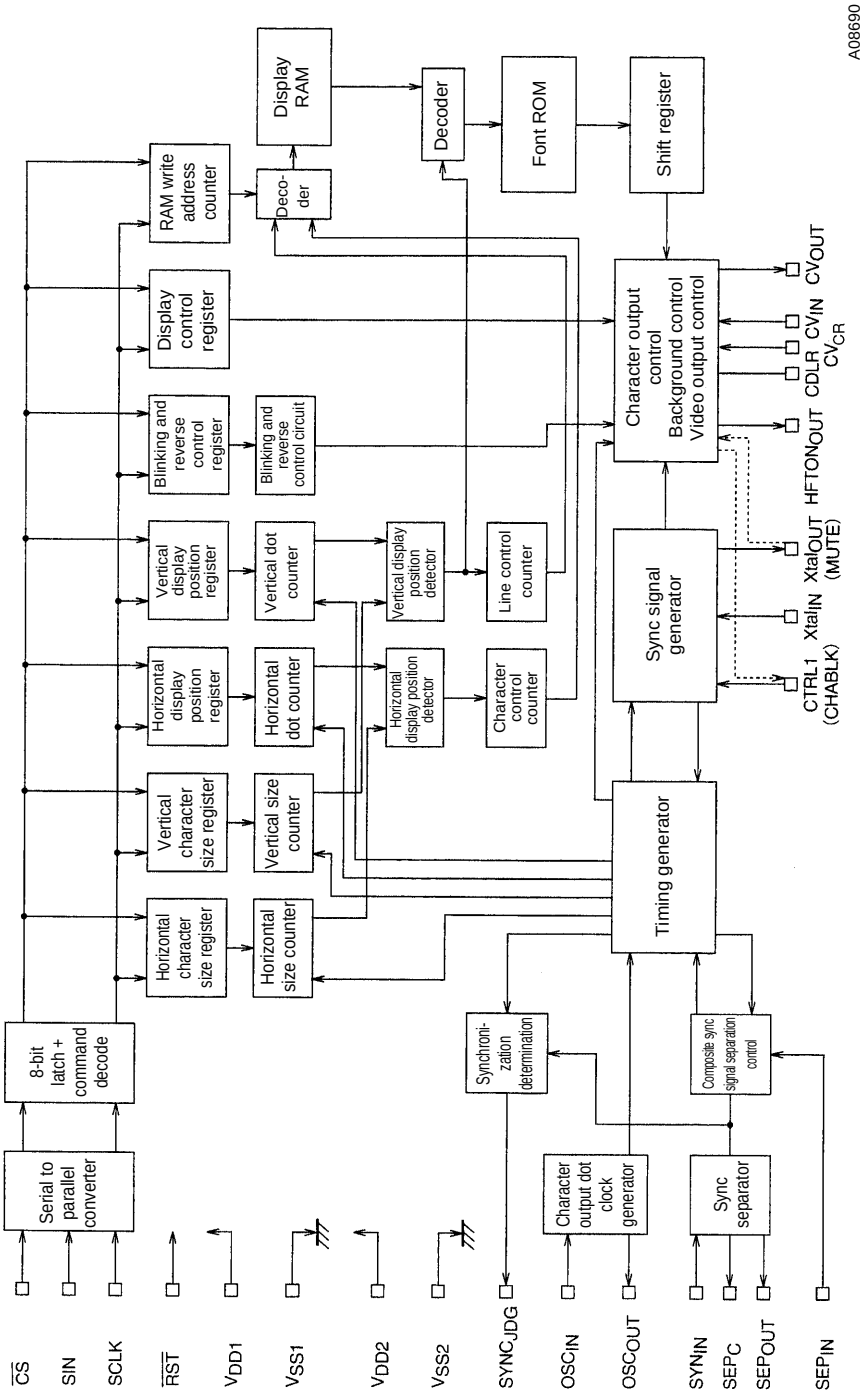
Timing Characteristics at Ta = –30 to +70°C, $V_{DD}1$ = 5 ±0.5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Minimum input pulse width	$t_{W(SCLK)}$	SCLK	200			ns
	$t_{W(CS)}$	$\overline{CS}$ (The period when $\overline{CS}$ is high)	1			µs
Data setup time	$t_{SU(CS)}$	$\overline{CS}$	200			ns
	$t_{SU(SIN)}$	SIN	200			ns
Data hold time	$t_{h(CS)}$	CS	2			µs
	$t_{h(SIN)}$	SIN	200			ns
One word write time	t_{word}	The time to write 8 bits of data	4.2			µs
	t_{wt}	The RAM data write time	1			µs

Serial Data Input Timing



System Block Diagram



Display Control Commands

Display control commands have an 8-bit format and are transferred using the serial input function. Commands consist of a command identification code in the first byte and command data in the following bytes. The following commands are supported.

1 COMMAND0: Display memory (VRAM) write address setup command
2 COMMAND1: Display character data write command
3 COMMAND2: Vertical display start position and vertical character size setup command
4 COMMAND3: Horizontal display start position and horizontal character size setup command
5 COMMAND4: Display control setup command
6 COMMAND5: Display control setup command
7 COMMAND6: Synchronizing signal detection setup command
8 COMMAND7: Display control setup command
9 COMMAND8: Display control setup command
10 COMMAND9: Display control setup command
11 COMMAND10: Display control setup command

Display Control Command Table

Command	First byte								Second byte							
	Command identification code				Data				Data							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
COMMAND0 Write address setup	1	0	0	0	V3	V2	V1	V0	0	0	0	H4	H3	H2	H1	H0
COMMAND1 Character write	1	0	0	1	0	0	0	at	c7	c6	c5	c4	c3	c2	c1	c0
COMMAND2 Vertical character size and vertical display start position	1	0	1	0	VS 21	VS 20	VS 11	VS 10	0	FS	VP 5	VP 4	VP 3	VP 2	VP 1	VP 0
COMMAND3 Horizontal character size and horizontal display start position	1	0	1	1	HS 21	HS 20	HS 11	HS 10	0	LC	HP 5	HP 4	HP 3	HP 2	HP 1	HP 0
COMMAND4 Display control	1	1	0	0	TST MOD	RAM ERS	OSC STP	SYS RST	0	BLK 2	BLK 1	BLK 0	BK 1	BK 0	RV	DSP ON
COMMAND5 Display control	1	1	0	1	NP 1	NP 0	NON	INT	0	NP 2	HLF INT	BCL	CB	PH 2	PH 1	PH 0
COMMAND6 Synchronizing signal detection	1	1	1	0	SEL 0	MOD 0	DIS LIN	MUT	0	RN 2	RN 1	RN 0	SN 3	SN 2	SN 1	SN 0
COMMAND7 Display control	1	1	1	1	0	0	SEL 1	CTL 3	0	CIN SEL	CIN CTL	VNP SEL	VSP SEL	MSK ERS	MSK SEL	EGL
COMMAND8 Display control	1	1	1	1	0	1	VSY SEL	HSY SEL	0	LNA 3	LNA 2	LNA 1	LNA 0	LPA 2	LPA 1	LPA 0
COMMAND9 Display control	1	1	1	1	1	0	LNB SEL	MOD 2	0	LNB 3	LNB 2	LNB 1	LNB 0	LPB 2	LPB 1	LPB 0
COMMAND10 Display control	1	1	1	1	1	1	LNC SEL	MOD 3	0	LNC 3	LNC 2	LNC 1	LNC 0	LPC 2	LPC 1	LPC 0

Once written, a first byte command identification code is stored until the next first byte is written. However, when the display character data write command (COMMAND1) is written, the LC74788/M/JM locks into the display character data write mode, and another first byte cannot be written.

When the $\overline{CS}$ pin is set high, the LC74788/M/JM is set to the COMMAND0 (display memory write address setup mode) state.

COMMAND0 (Display memory write address setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 0 identification code Sets the display memory write address.	
6	—	0		
5	—	0		
4	—	0		
3	V3	0	Display memory line address (0 to B hexadecimal)	
		1		
2	V2	0		
		1		
1	V1	0		
		1		
0	V0	0		
		1		

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Second byte identification code	
6	—	0		
5	—	0		
4	H4	0	Display memory column address (0 to 17 hexadecimal)	
		1		
3	H3	0		
		1		
2	H2	0		
		1		
1	H1	0		
		1		
0	H0	0		
		1		

Note: All registers are set to 0 when the LC74788/M/JM is reset by the $\overline{\text{RST}}$ pin.

COMMAND1 (Display character data write setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 1 identification code. Sets up display character data write mode.	When this command is input, the LC74788/M/JM locks in the display character data write mode until the $\overline{CS}$ pin goes high
6	—	0		
5	—	0		
4	—	1		
3	—	0		
2	—	0		
1	—	0		
0	at	0	Character attribute off	
		1	Character attribute on	

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	c7	0	Character code (00 to 7F hexadecimal) (FE (hex): spacing character) (FF (hex): transparent spacing character)	
		1		
6	c6	0		
		1		
5	c5	0		
		1		
4	c4	0		
		1		
3	c3	0		
		1		
2	c2	0		
		1		
1	c1	0		
		1		
0	c0	0		
		1		

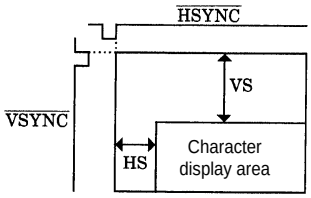
Note: All registers are set to 0 when the LC74788/M/JM is reset by the $\overline{RST}$ pin.

COMMAND2: Vertical display start position and vertical character size setup command

• First byte

<table>
<tr><th rowspan="2">DA
0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>1</td><td rowspan="4">Command 2 identification code
Sets the vertical display start position and the vertical character size</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>—</td><td>0</td></tr>
<tr><td>5</td><td>—</td><td>1</td></tr>
<tr><td>4</td><td>—</td><td>0</td></tr>
<tr><td>3</td><td>VS21</td><td>0
1</td><td rowspan="3">VS21 \ VS20 | 0 | 1
0 | 1H/dot | 2H/dot
1 | 3H/dot | 1H/dot</td><td rowspan="3">Second line vertical character size</td></tr>
<tr><td>2</td><td>VS20</td><td>0
1</td></tr>
<tr><td>1</td><td>VS11</td><td>0
1</td><td rowspan="3">VS11 \ VS10 | 0 | 1
0 | 1H/dot | 2H/dot
1 | 3H/dot | 1H/dot</td><td rowspan="3">First line vertical character size</td></tr>
<tr><td>0</td><td>VS10</td><td>0
1</td></tr>
</table>

• Second byte

<table>
<tr><th rowspan="2">DA
0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>0</td><td>Second byte identification bit</td><td></td></tr>
<tr><td>6</td><td>F_S</td><td>0
1</td><td>Crystal oscillator frequency: 2fsc
Crystal oscillator frequency: 4fsc</td><td></td></tr>
<tr><td>5</td><td>VP5
(MSB)</td><td>0
1</td><td rowspan="8">If VS is the vertical display start position then:
$VS = \alpha + H \times (2\sum_{n=0}^{5} 2^n VP_n)$
H: the horizontal synchronization pulse period
α = 20 H (in 525-line systems)
= 25 H (in 625-line systems)

</td><td rowspan="8">The vertical display start position is set by the 6 bits VP0 to VP5.
The weight of bit 1 is 2H.</td></tr>
<tr><td>4</td><td>VP4</td><td>0
1</td></tr>
<tr><td>3</td><td>VP3</td><td>0
1</td></tr>
<tr><td>2</td><td>VP2</td><td>0
1</td></tr>
<tr><td>1</td><td>VP1</td><td>0
1</td></tr>
<tr><td>0</td><td>VP0
(LSB)</td><td>0
1</td></tr>
</table>

Note: All registers are set to 0 when the LC74788/M/JM is reset by the $\overline{RST}$ pin.

COMMAND3 (Horizontal display start position and horizontal size setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1		
6	—	0	Command 3 identification code	
5	—	1	Sets the horizontal display start position and the horizontal character size.	
4	—	1		
3	HS21	0		Second line horizontal character size
		1		
2	HS20	0		
		1		
1	HS11	0		First line horizontal character size
		1		
0	HS10	0		
		1		

HS21 \ HS20	0	1
0	1 Tc/dot	2 Tc/dot
1	3 Tc/dot	1 Tc/dot

HS11 \ HS10	0	1
0	1 Tc/dot	2 Tc/dot
1	3 Tc/dot	1 Tc/dot

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LC	0	Use the LC oscillator for the dot clock	Selects the dot clock used for character display in the horizontal direction.
		1	Use the crystal oscillator for the dot clock	
5	HP5 (MSB)	0	If HS is the horizontal start position then:	
		1	$HS = Tc \times (2\sum_{n=0}^{5} 2^n HP_n)$	
4	HP4	0	Tc: Period of the oscillator connected to OSCIN/OSCOUT in operating mode.	
		1		
3	HP3	0		The horizontal display start position is set by the 6 bits HP0 to HP5.
		1		
2	HP2	0		The weight of bit 1 is 2Tc.
		1		
1	HP1	0		
		1		
0	HP0 (LSB)	0		
		1		

Note: All registers are set to 0 when the LC74788/M/JM is reset by the $\overline{RST}$ pin.

COMMAND4 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 4 identification code. Display character data write setup.	
6	—	1		
5	—	0		
4	—	0		
3	TSTMOD	0	Normal operating mode	This bit must be set to 0.
		1	Test mode	
2	RAMERS	0		Erasing RAM takes about 500 µs. (This operation must be executed in the DSPOFF state.)
		1	Erase display RAM. (The RAM data is set to FF hexadecimal.)	
1	OSCSTP	0	Do not stop the crystal and LC oscillators.	Valid in external synchronization mode when character display is off.
		1	Stop the crystal and LC oscillators.	
0	SYSRST	0		The registers are reset when the $\overline{CS}$ pin is low, and the reset state is cleared when $\overline{CS}$ is set high.
		1	Reset all registers and turn display off.	

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	BLK2	0	Character display area	Specifies the size for complete fill in
		1	Video display area	
5	BLK1	0		Changes the blanking size
		1		
4	BLK0	0		
		1		
3	BK1	0	Blinking period: About 0.5 s	Switches the blinking period
		1	Blinking period: About 1.0 s	
2	BK0	0	Blinking off	Blinking in reverse video mode switches the display between normal character display and reverse video display.
		1	Blinking on	
1	RV	0	Reverse video off	
		1	Reverse video on	
0	DSPON	0	Character display off	
		1	Character display on	

BLK1 \ BLK0	0	1
0	Blanking off	Character size
1	Frame size	Complete fill in

Note: All registers are set to 0 when the LC74788/M/JM is reset by the $\overline{RST}$ pin.

COMMAND5 (Display control setup command)

• First byte

<table>
<tr><th rowspan="2">DA
0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>1</td><td rowspan="4">Command 5 identification code
Display control setup</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>—</td><td>1</td></tr>
<tr><td>5</td><td>—</td><td>0</td></tr>
<tr><td>4</td><td>—</td><td>1</td></tr>
<tr><td>3</td><td>NP1</td><td>0
1</td><td rowspan="2"><table><tr><th>NP2</th><th>NP1</th><th>NP0</th><th>Format</th></tr><tr><td>0</td><td>0</td><td>0</td><td>NTSC</td></tr><tr><td>0</td><td>0</td><td>1</td><td>PAL-M</td></tr><tr><td>0</td><td>1</td><td>0</td><td>PAL</td></tr><tr><td>0</td><td>1</td><td>1</td><td>PAL-N</td></tr><tr><td>1</td><td>0</td><td>0</td><td>NTSC4.43</td></tr><tr><td>1</td><td>0</td><td>1</td><td>PAL60</td></tr></table></td><td rowspan="2">Switches between the NTSC, PAL, PAL-N, PAL-M, NTSC 4.43, and PAL60 formats.</td></tr>
<tr><td>2</td><td>NP0</td><td>0
1</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">NON</td><td>0</td><td>Interlaced</td><td rowspan="2">Switches between interlaced and noninterlaced video.</td></tr>
<tr><td>1</td><td>Noninterlaced</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">INT</td><td>0</td><td>External synchronization</td><td rowspan="2">Switches between external and internal synchronization</td></tr>
<tr><td>1</td><td>Internal synchronization</td></tr>
</table>

• Second byte

<table>
<tr><th rowspan="2">DA
0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>0</td><td>Second byte identification bit</td><td></td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">NP2</td><td>0</td><td></td><td rowspan="2">Set with NP0 and NP1.</td></tr>
<tr><td>1</td><td></td></tr>
<tr><td rowspan="2">5</td><td rowspan="2">HLFINT</td><td>0</td><td>Normal mode</td><td rowspan="2"></td></tr>
<tr><td>1</td><td>Half internal synchronization mode</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">BCL</td><td>0</td><td>Background color on</td><td rowspan="2">Only valid in internal synchronization mode.</td></tr>
<tr><td>1</td><td>No background color (Only the background level is set)</td></tr>
<tr><td rowspan="2">3</td><td rowspan="2">CB</td><td>0</td><td>Color burst signal output.</td><td rowspan="2">Only valid when BCL is high.</td></tr>
<tr><td>1</td><td>Color burst signal output stopped.</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">PH2</td><td>0
1</td><td rowspan="6"><table><tr><th>PH2</th><th>PH1</th><th>PH0</th><th>Background color (phase)</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Cyan</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Yellow</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Cyan blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Green</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Orange</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Magenta</td></tr></table></td><td rowspan="6">Background color specification</td></tr>
<tr><td rowspan="2">1</td><td rowspan="2">PH1</td><td>0
1</td></tr>
<tr><td rowspan="2">0</td><td rowspan="2">PH0</td><td>0
1</td></tr>
</table>

Note: All registers are set to 0 when the LC74786/M/JM is reset by the $\overline{\text{RST}}$ pin.

COMMAND6 (Synchronizing signal detection setup command)

• First byte

<table>
<tr><th rowspan="2">DA
0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>1</td><td rowspan="4">Command 6 identification code.
Sets up synchronizing signal control.</td><td rowspan="4"></td></tr>
<tr><td>6</td><td>—</td><td>1</td></tr>
<tr><td>5</td><td>—</td><td>1</td></tr>
<tr><td>4</td><td>—</td><td>0</td></tr>
<tr><td>3</td><td>SEL0</td><td>0
1</td><td rowspan="2"><table><tr><th>SEL0</th><th>MOD</th><th>SEPOUT output</th></tr><tr><td>0</td><td>0</td><td>Sync separator signal</td></tr><tr><td>0</td><td>1</td><td>Low-level output</td></tr><tr><td>1</td><td>0</td><td>High-level output</td></tr><tr><td>1</td><td>1</td><td>ST pulse signal</td></tr></table></td><td>Switches the SEP_{OUT} (pin 19) output</td></tr>
<tr><td>2</td><td>MOD0</td><td>0
1</td><td></td></tr>
<tr><td>1</td><td>DISLIN</td><td>0
1</td><td>12 lines
10 lines</td><td>Switches the number of lines displayed</td></tr>
<tr><td>0</td><td>MUT</td><td>0
1</td><td>Normal output
CV_{IN} is cut and CV_{OUT} is held at the pedestal level.</td><td>CV_{OUT} switching</td></tr>
</table>

• Second byte

<table>
<tr><th rowspan="2">DA
0 to 7</th><th rowspan="2">Register</th><th colspan="2">Contents</th><th rowspan="2">Notes</th></tr>
<tr><th>State</th><th>Function</th></tr>
<tr><td>7</td><td>—</td><td>0</td><td>Second byte identification bit</td><td></td></tr>
<tr><td>6</td><td>RN2</td><td>0
1</td><td rowspan="3"><table><tr><th>RN2</th><th>RN1</th><th>RN0</th><th>Number of times HSYNC detected</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0 times</td></tr><tr><td>0</td><td>0</td><td>1</td><td>4 times</td></tr><tr><td>0</td><td>1</td><td>0</td><td>8 times</td></tr><tr><td>1</td><td>0</td><td>0</td><td>16 times</td></tr></table></td><td rowspan="3">External synchronizing signal detection control.
Signal absent → signal present transition detection
Sets the sampling period in which SYNC can be detected continuously in the horizontal synchronizing signal period (1H).</td></tr>
<tr><td>5</td><td>RN1</td><td>0
1</td></tr>
<tr><td>4</td><td>RN0</td><td>0
1</td></tr>
<tr><td>3</td><td>SN3</td><td>0
1</td><td rowspan="3"><table><tr><th>SN3</th><th>SN2</th><th>SN1</th><th>SN0</th><th>Number of times HSYNC detected</th></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Not detected</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>32 times</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>64 times</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>128 times</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>256 times</td></tr></table></td><td rowspan="3">External synchronizing signal detection control.
Signal present → signal absent transition detection
Sets the sampling period in which SYNC cannot be detected continuously in the horizontal synchronizing signal period (1H).</td></tr>
<tr><td>2</td><td>SN2</td><td>0
1</td></tr>
<tr><td>1</td><td>SN1</td><td>0
1</td></tr>
<tr><td>0</td><td>SN0</td><td>0
1</td><td></td></tr>
</table>

Note: All registers are set to 0 when the LC74788/M/JM is reset by the $\overline{RST}$ pin.

COMMAND7 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 7 identification code. Display control setup.	
6	—	0		
5	—	0		
4	—	1		
3	—	0	Extended command 0 identification code	
2	—	0		
1	SEL1	0	Vertical synchronizing signal (external V separation) input	Switches the SEP_{IN} (pin 20) input. Only valid when CTL3 is high.
		1	Frame signal input	
0	CTL3	0	Use internal V separation	Switches V separation.
		1	Do not use internal V separation	

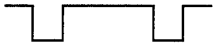
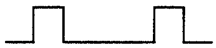
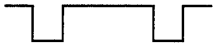
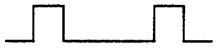
• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	CINSEL	0	Blanking area (The logical OR of the character and frame signals)	CV_{CR} on signal switching
		1	Video signal display area	
5	CINCTL	0	CV_{CR}: off	CV_{CR} on/off setting
		1	CV_{CR}: on	
4	VNPSEL	0	V falling edge detection	Switches the V acquisition polarity in external mode when internal V separation is used.
		1	V rising edge detection	
3	VSPSEL	0	VSEP: about 8.9 µs (for NTSC)	Switches the internal V separation period.
		1	VSEP: about 17.8 µs (for NTSC)	
2	MSKERS	0	Mask valid	Clears the HSYNC and VSYNC masks.
		1	Mask invalid	
1	MSKSEL	0	3H (for NTSC)	Switches the VSYNC mask.
		1	20H (for NTSC)	
0	EGL	0	Frame level 0 only (V_{BK0})	Switches the frame level.

Note: All registers are set to 0 when the LC74786/M/JM is reset by the $\overline{RST}$ pin.

COMMAND8 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 8 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	0	Extended command 1 identification code	
2	—	1		
1	VSYSEL	0	Negative polarity 	SEP_{IN} input polarity switching. Only valid when CTL3 is high.
		1	Positive polarity 	
0	HSYSEL	0	Negative polarity 	SYN_{IN} (only valid when the sync separator circuit is not used) and SEP_{OUT} input and output polarity switching
		1	Positive polarity 	

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LNA3	0		Specifies the line whose background is to be changed. (If the same line is specified to have different background colors with LNA*, LNB*, and LNC*, then the setting specified by the last command issued will be valid. The previously specified registers (LN* and LP*) will all be reset to 0.)
		1		
5	LNA2	0		
		1		
4	LNA1	0		
		1		
3	LNA0	0		
		1		
2	LPA2	0		Specifies the background color
		1		
1	LPA1	0		
		1		
0	LPA0	0		
		1		

LNA3	LNA2	LNA1	LNA0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	—	—	Line 12

LPA2	LPA1	LPA0	Line background color (phase)
0	0	0	Cyan
0	0	1	Yellow
0	1	0	Red
0	1	1	Blue
1	0	0	Cyan blue
1	0	1	Green
1	1	0	Orange
1	1	1	Magenta

Note: All registers are set to 0 when the LC74788/M/JM is reset by the $\overline{RST}$ pin.

COMMAND9 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 9 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended command 2 identification code	
2	—	0		
1	LNBSEL	0	Normal line background color operation	Switches the RV mode background color for the line specified by LNB* for characters specified for RV display.
		1	RV characters have the background color specified by PH* or the RV character background color is white.	
0	MOD2	0	The LNBSEL: 1 setting specifications	Valid when LNBSEL is high
		1	RV characters have the background color specified by PH*, characters are white.	

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LNB3	0		Specifies the line whose background is to be changed. (If the same line is specified to have different background colors with LNA*, LNB*, and LNC*, then the setting specified by the last command issued will be valid. The previously specified registers (LN* and LP*) will all be reset to 0.)
		1		
5	LNB2	0		
		1		
4	LNB1	0		
		1		
3	LNB0	0		
		1		
2	LPB2	0		Specifies the background color
		1		
1	LPB1	0		
		1		
0	LPB0	0		
		1		

LNB3	LNB2	LNB1	LNB0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	—	—	Line 12

LPB2	LPB1	LPB0	Line background color (phase)
0	0	0	Cyan
0	0	1	Yellow
0	1	0	Red
0	1	1	Blue
1	0	0	Cyan blue
1	0	1	Green
1	1	0	Orange
1	1	1	Magenta

Note: All registers are set to 0 when the LC74788/M/JM is reset by the $\overline{\text{RST}}$ pin.

COMMAND10 (Display control setup command)

• First byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	1	Command 10 identification code. Display control setup.	
6	—	1		
5	—	1		
4	—	1		
3	—	1	Extended command 3 identification code	
2	—	1		
1	LNCSEL	0	Normal line background color operation	Switches the RV mode background color for the line specified by LNC* for characters specified for RV display.
		1	RV characters have the background color specified by PH* or the RV character background color is white.	
0	MOD3	0	The LNCSEL: 1 setting specifications	Valid when LNCSEL is high
		1	RV characters have the background color specified by PH*, characters are white.	

• Second byte

DA 0 to 7	Register	Contents		Notes
		State	Function	
7	—	0	Second byte identification bit	
6	LNC3	0		Specifies the line whose background is to be changed. (If the same line is specified to have different background colors with LNA*, LNB*, and LNC*, then the setting specified by the last command issued will be valid. The previously specified registers (LN* and LP*) will all be reset to 0.)
		1		
5	LNC2	0		
		1		
4	LNC1	0		
		1		
3	LNC0	0		
		1		
2	LPC2	0		Specifies the background color.
		1		
1	LPC1	0		
		1		
0	LPC0	0		
		1		

LNC3	LNC2	LNC1	LNC0	Specified line
0	0	0	0	Do not change the line background
0	0	0	1	Line 1
0	0	1	0	Line 2
0	0	1	1	Line 3
0	1	0	0	Line 4
0	1	0	1	Line 5
0	1	1	0	Line 6
0	1	1	1	Line 7
1	0	0	0	Line 8
1	0	0	1	Line 9
1	0	1	0	Line 10
1	0	1	1	Line 11
1	1	—	—	Line 12

LPC2	LPC1	LPC0	Line background color (phase)
0	0	0	Cyan
0	0	1	Yellow
0	1	0	Red
0	1	1	Blue
1	0	0	Cyan blue
1	0	1	Green
1	1	0	Orange
1	1	1	Magenta

Note: All registers are set to 0 when the LC74788/M/JM is reset by the $\overline{\text{RST}}$ pin.

Display Screen Structure

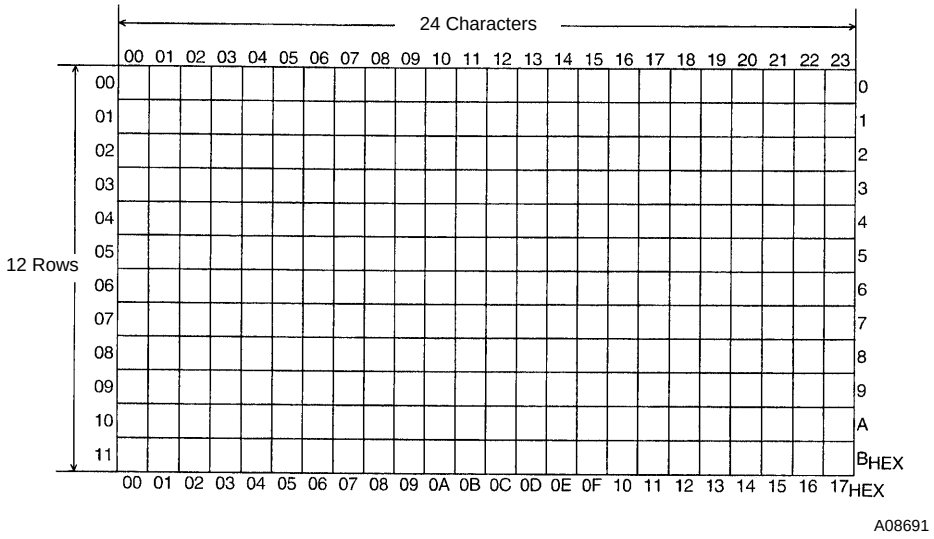
The display consists of 12 lines of 24 characters.

Up to 288 characters can be displayed.

The number of characters that can be displayed is reduced when enlarged characters are displayed.

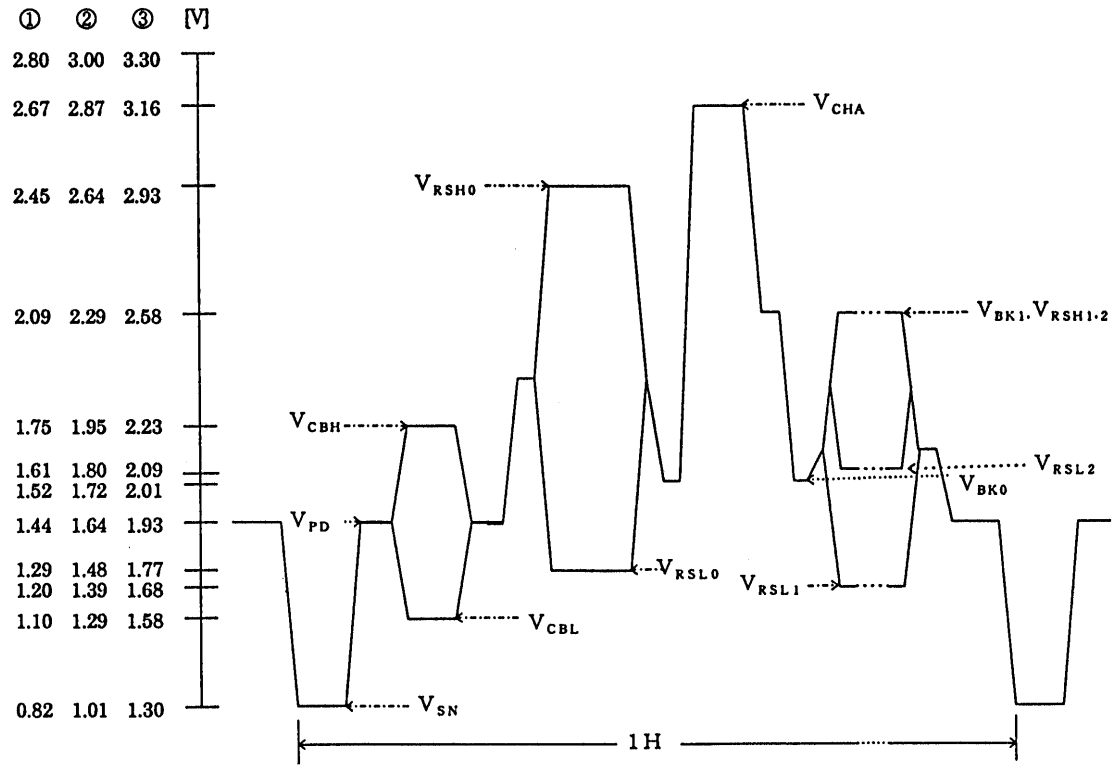
Display memory addresses are specified as row (0 to 11 decimal) and column (0 to 23 decimal) addresses.

Display Screen Structure (display memory addresses)



Composite Video Signal Output Levels (internally generated levels)

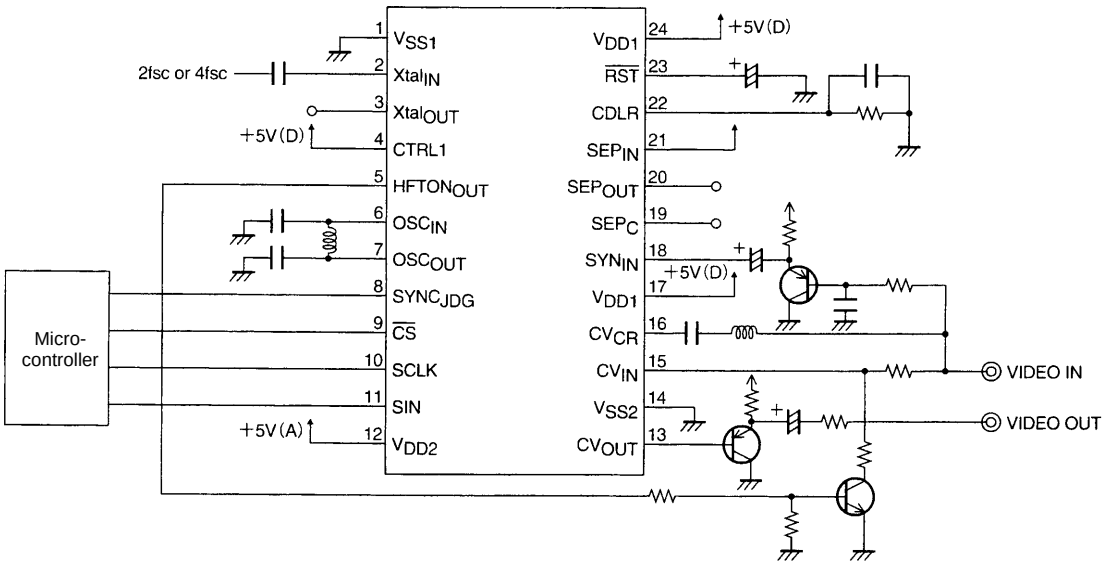
CV_{OUT} output level waveform ($V_{DD}2$ = 5.0 V)



Output level	Output voltage (1) [V]	Output voltage (2) [V]	Output voltage (3) [V]
V_{CHA} : Character	2.67	2.87	3.16
$V_{RH}0$: Background color (other than blue) high	2.45	2.64	2.93
$V_{RSH}1, 2$: Blue background color 1 and 2 high	2.09	2.29	2.58
$V_{Bk}1$: Frame 1	2.09	2.29	2.58
V_{CBH} : Color burst high	1.75	1.95	2.23
$V_{RSL}2$: Blue background color 2 low	1.61	1.80	2.09
$V_{BK}0$: Frame 0	1.52	1.72	2.01
V_{PD} : Pedestal	1.44	1.64	1.93
$V_{RSL}0$: Background color (other than blue) low	1.29	1.48	1.77
$V_{RSL}1$: Blue background color 1 low	1.20	1.39	1.68
V_{CBL} : Color burst low	1.10	1.29	1.58
V_{SN} : Sync	0.82	1.01	1.30

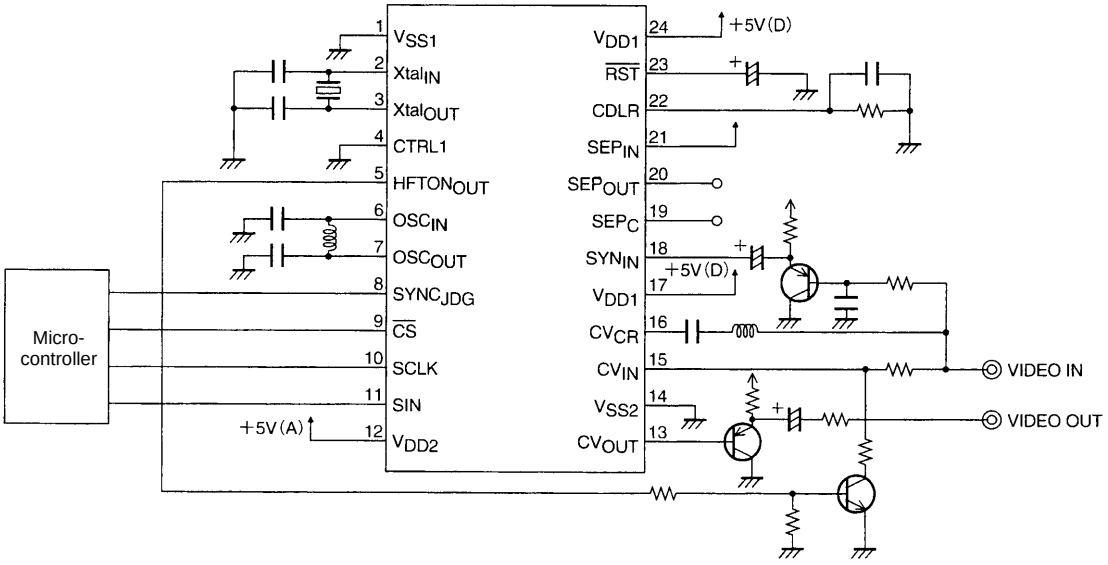
Sample Application Circuits (When the LC74788/M/JM is used in conjunction with a single-chip Y/C circuit.)

• Circuit Using an External System Clock Input



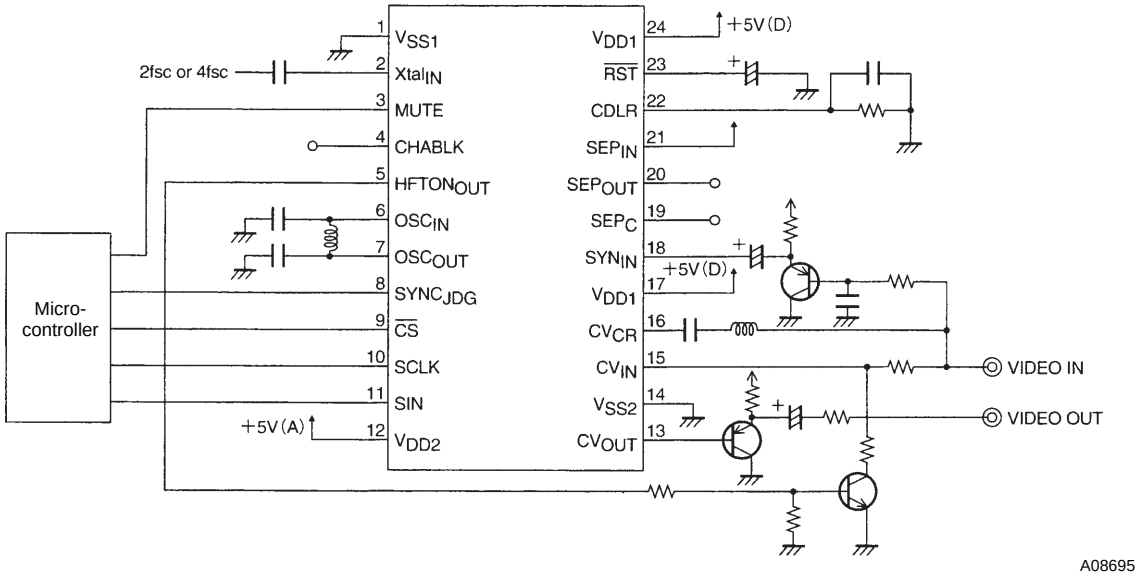
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• Circuit Using a Crystal Oscillator



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• Circuit Using an External System Clock Input (when the pin 3 and 4 functions are modified by mask options)



Note: When a sync tip level of 1.3 V DC (CV_{IN} input signal: sync tip = 1.3 V) is selected for the internal generated video signals by option settings, the electrolytic capacitor connected to SYN_{IN} must be connected with the correct polarity.

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