512MB DDR SDRAM SO-DIMM

200 PIN SO-DIMM

SDN06464L1BF1MT-xxR

512MByte in FBGA Technology

RoHS compliant

Options:

- Data Rate / Latency — Marking
  DDR 333 MT/s CL2.5 — -60
  DDR 400 MT/s CL3.0 — -50
- Module density
  512MByte with 8 dies and 1 rank
- Standard Grade (T_A) 0°C to 70°C
  (T_C) 0°C to 85°C

*) The refresh rate has to be doubled when 85°C<T_C<95°C

Environmental Requirements:

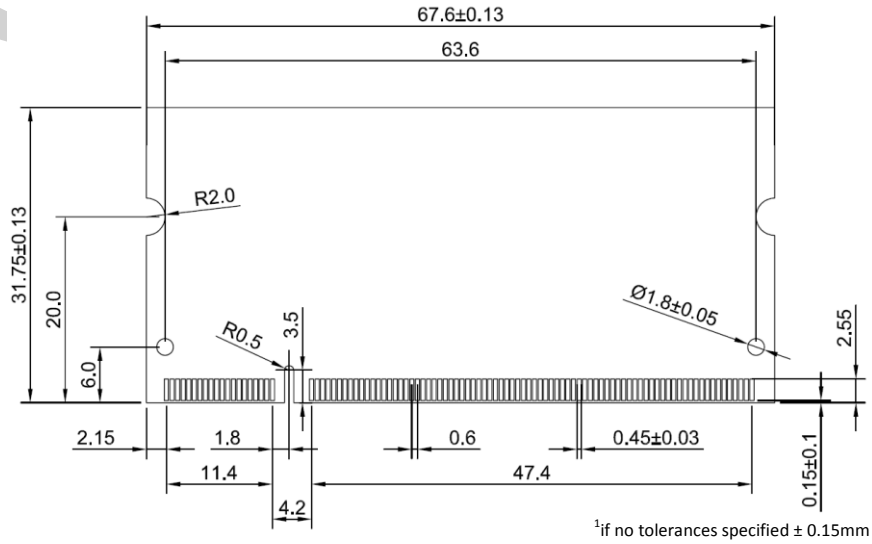
- Operating temperature (ambient)
  Standard Grade 0°C to 70°C
- Operating Humidity
  10% to 90% relative humidity, noncondensing
- Operating Pressure
  105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
  -55°C to 100°C
- Storage Humidity
  5% to 95% relative humidity, noncondensing
- Storage Pressure
  1682 PSI (up to 5000 ft.) at 50°C

Features:

- 200-pin 64-bit DDR1 Small Outline Dual-In-Line Double Data Rate Synchronous DRAM module
- Module organization: single rank 64M x 64
- V_{DD} = 2.5V ±0.2V, V_{DDQ} 2.5V ±0.2V
- V_{DD} = 2.6V ±0.1V, V_{DDQ} 2.6V ±0.1V (DDR400)
- 2.5V I/O (SSTL_2 compatible)
- Serial Presence Detect with EEPROM
- Gold-contact pads
- This module is fully pin and functional compatible to the JEDEC PC-3200 spec. and JEDEC- Standard MO-224. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

- **DDR1 - SDRAM component Micron MT46V64M8BN-6:F**
- 64Mx8 DDR1 SDRAM in 60-ball FBGA package
- Internal, pipelined double-data-rate (DDR)
- 2n pre-fetch architecture
- DLL to align DQ and DQS transitions with CK
- Bidirectional data strobe (DQS) transmitted/received with data, source-synchronous data capture
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data
- Programmable burst length: 2,4 or 8
- Adjustable data-output drive strength
- Auto Refresh (CBR) and Self Refresh, 8k Refresh every 64ms

Figure: mechanical dimensions[1]



[1]if no tolerances specified ± 0.15mm

This Swissbit module family is industry standard 200-pin 8-byte Double Date rate synchronous SDRAM Small Outline Dual-In-line Memory Modules (SO-DIMMs), which are organized as x64 high speed memory arrays designed for use in non-parity applications. These SO-DIMMs are assembled in FBGA Technology. The passive devices and the EEPROM are SMD components.
The SO-DIMMs use serial presence detects (SPD) implemented via serial EEPROM using the two-pin-I^2C protocol. The first 128 bytes are utilized by the SO-DIMM manufacturer and the second 128 bytes are available to the end user.

All Swissbit DDR1 SO-DIMMs provide a high performance, flexible 8-byte interface in a 67.6 mm long footprint.

All modules of the extended temperature grade have seen special tests during the manufacturing process to ensure proper operation according to the field of operation as stated in the environmental conditions.

Module Configuration

Organization	DDR SDRAMs used	Row Addr.	Bank Select	Col. Addr.	Refresh	Module Dimensions in mm
64M x 64	8 x 64M x 8	13	BA0, BA1	11	8k	67.60 x 31.75 x 3.80 max

Product Spectrum

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SDN06464L1BF1MT-60R	512MB	2.7 GB/s	6.0ns/333MT/s	2.5-3-3
SDN06464L1BF1MT-50R	512MB	3.2 GB/s	5.0ns/400MT/s	3.0-3-3

Pin Name

A0 – A9, A11 – A12	Address Inputs
A10/AP	Address Input/Autoprecharge
BA0, BA1	Bank Selects
DQ0 – DQ63	Data Input/Output
DM0 – DM7	Data Masks
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Read / Write Enable
CKE0	Clock Enable
CK0	Clock Inputs, positive line
CK0#	Clock Inputs, negative line
DQS0 – DQS7	Data strobes

S0#	Chip Select
V_{DD}	Power (2.5V± 0.2V)
V_{DDQ}	Power (2.5V±0.2V)
V_{DDID}	V_{DD}, V_{DDQ} level detection
V_{DDSPD}	SPD Power
V_{REF}	Input/Output Reference
V_{SS}	Ground
SCL	Clock for Serial Presence Detect
SDA	Serial Data Out for Serial Presence Detect
NC	No Connection

Pin Configuration

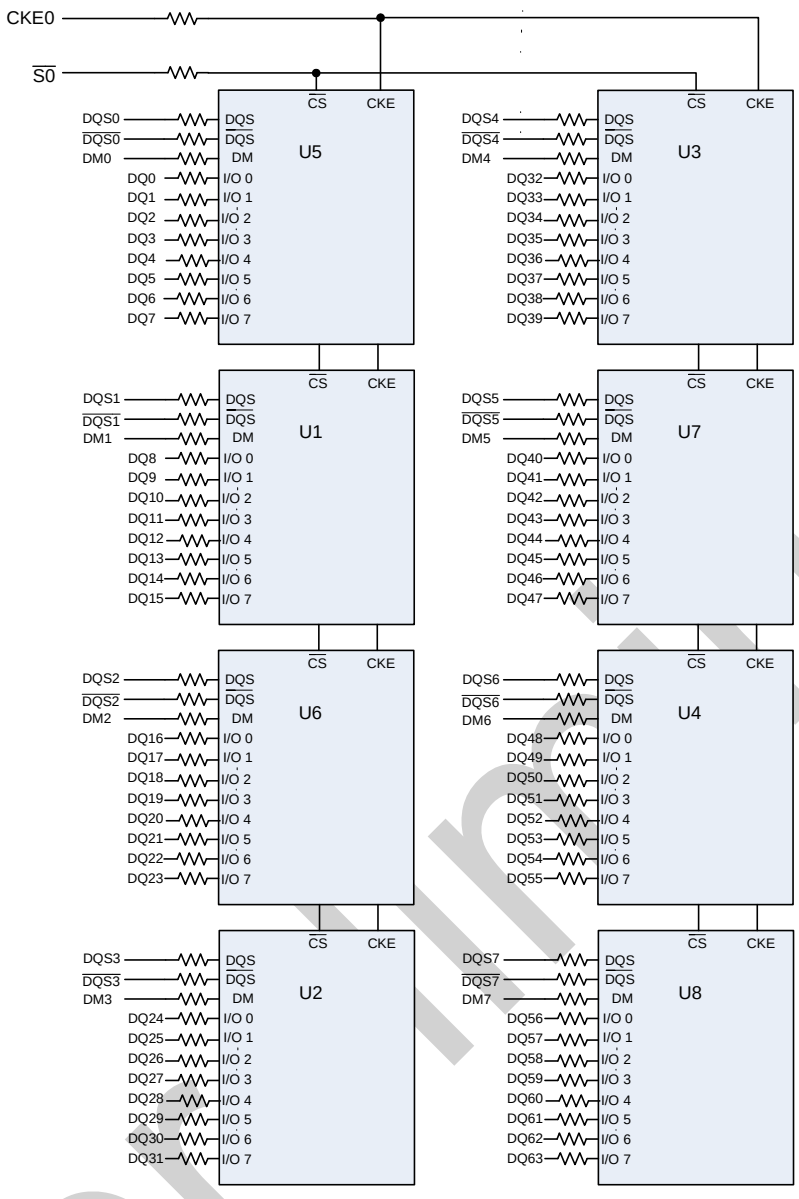
PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
1	V_{REF}	2	V_{REF}	101	A9	102	A8
3	V_{SS}	4	V_{SS}	103	V_{SS}	104	V_{SS}
5	DQ0	6	DQ4	105	A7	106	A6
7	DQ1	8	DQ5	107	A5	108	A4
9	VDD	10	V_{DD}	109	A3	110	A2
11	DQS0	12	DM0	111	A1	112	A0
13	DQ2	14	DQ6	113	V_{DD}	114	V_{DD}
15	V_{SS}	16	V_{SS}	115	A10/AP	116	BA1
17	DQ3	18	DQ7	117	BA0	118	RAS#
19	DQ8	20	DQ12	119	WE#	120	CAS#
21	V_{DD}	22	V_{DD}	121	S0#	122	NC(S1#)
23	DQ9	24	DQ13	123	NC/(A13)	124	NC
25	DQS1	26	DM1	125	V_{SS}	126	V_{SS}
27	V_{SS}	28	V_{SS}	127	DQ32	128	DQ36
29	DQ10	30	DQ14	129	DQ33	130	DQ37
31	DQ11	32	DQ15	131	V_{DD}	132	V_{DD}
33	V_{DD}	34	V_{DD}	133	DQS4	134	DM4
35	CK0	36	V_{DD}	135	DQ34	136	DQ38
37	CK0#	38	V_{SS}	137	V_{SS}	138	V_{SS}
39	V_{SS}	40	V_{SS}	139	DQ35	140	DQ39
41	DQ16	42	DQ20	141	DQ40	142	DQ44
43	DQ17	44	DQ21	143	V_{DD}	144	V_{DD}
45	V_{DD}	46	V_{DD}	145	DQ41	146	DQ45
47	DQS2	48	DM2	147	DQS5	148	DM5
49	DQ18	50	DQ22	149	V_{SS}	150	V_{SS}
51	V_{SS}	52	V_{SS}	151	DQ42	152	DQ46

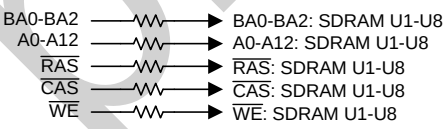
(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

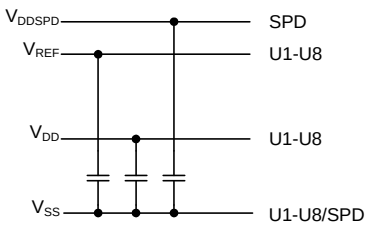
PIN #	Front Side	PIN #	Back Side	PIN #	Front Side	PIN #	Back Side
53	DQ19	54	DQ23	153	DQ43	154	DQ47
55	DQ24	56	DQ28	155	V_{DD}	156	V_{DD}
57	V_{DD}	58	V_{DD}	157	V_{DD}	158	NC(CK1#)
59	DQ25	60	DQ29	159	V_{SS}	160	NC(CK1)
61	DQS3	62	DM3	161	V_{SS}	162	V_{SS}
63	V_{SS}	64	V_{SS}	163	DQ48	164	DQ52
65	DQ26	66	DQ30	165	DQ49	166	DQ53
67	DQ27	68	DQ31	167	V_{DD}	168	V_{DD}
69	V_{DD}	70	V_{DD}	169	DQS6	170	DM6
71	NC/(CB0)	72	NC/(CB4)	171	DQ50	172	DQ54
73	NC/(CB1)	74	NC/(CB5)	173	V_{SS}	174	V_{SS}
75	V_{SS}	76	V_{SS}	175	DQ51	176	DQ55
77	NC/(DQS8)	78	NC/(DM8)	177	DQ56	178	DQ60
79	NC/(CB2)	80	NC/(CB6)	179	V_{DD}	180	V_{DD}
81	V_{DD}	82	V_{DD}	181	DQ57	182	DQ61
83	NC/(CB3)	84	NC/(CB7)	183	DQS7	184	DM7
85	NC	86	NC/(RESET)	185	V_{SS}	186	V_{SS}
87	V_{SS}	88	V_{SS}	187	DQ58	188	DQ62
89	NC/(CK2)	90	V_{SS}	189	DQ59	190	DQ63
91	NC/(CK2#)	92	V_{DD}	191	V_{DD}	192	V_{DD}
93	V_{DD}	94	V_{DD}	193	SDA	194	SA0
95	NC(CKE1)	96	CKE0	195	SCL	196	SA1
97	NC	98	NC/(BA2)	197	V_{DD_SPD}	198	SA2
99	A12	100	A11	199	V_{DD_ID}	200	NC

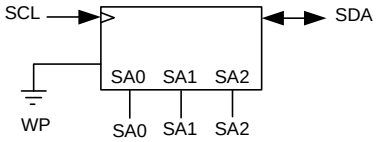
(Sig): Signal in brackets may be routed to the socket connector, but is not used on the module

FUNCTIONAL BLOCK DIAGRAMM 512MB DDR SDRAM SODIMM 1RANK; NON-ECC









DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(0°C ≤ T_A ≤ + 70°C; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Supply Voltage	V_{DD}	2.3	2.7	V
I/O Supply Voltage	V_{DDQ}	2.3	2.7	V
I/O Reference Voltage	V_{REF}	0.49 x V_{DDQ}	0.51x V_{DDQ}	V
I/O Termination Voltage (system)	V_{TT}	V_{REF} – 0.04	V_{REF} + 0.04	V
Input High (Logic 1) Voltage	$V_{IH (DC)}$	V_{REF} + 0.15	V_{DD} + 0.3	V
Input Low (Logic 0) Voltage	$V_{IL (DC)}$	-0.3	V_{REF} – 0.15	V
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{DD}, V_{REF} pin 0V ≤ V_{IN} ≤1.35V (All other pins not under test = 0V)	I_I	-16	16	µA
OUTPUT LEAKAGE CURRENT (DQ_S are disabled; 0V ≤ V_{OUT} ≤ V_{DDQ})	I_{OZ}	-40	40	µA
OUTPUT LEVELS: High Current (V_{OUT} = V_{DDQ}-0.373V,minimum V_{REF}, minimum V_{TT}) Low Current (V_{OUT} =0.373V, maximum V_{REF}, maximum V_{TT})	I_{OH} I_{OL}	-16.8 16.8	- -	mA mA

AC INPUT OPERATING CONDITIONS

(0°C ≤ T_A ≤ + 70°C; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH (AC)}$	V_{REF} + 0.310	-	V
Input Low (Logic 0) Voltage	$V_{IL (AC)}$	-	V_{REF} - 0.310	V
I/O Reference Voltage	$V_{REF(AC)}$	0.49 x V_{DDQ}	0.51x V_{DDQ}	V

CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input/Output Capacitance: DQ, DQS	C_{10}	4.0	5.0	pF
Input Capacitance: Command and Address	C_{11}	18.0	27.0	pF
Input Capacitance: /S 0,1	C_{11}	18.0	27.0	pF
Input Capacitance: CK, /CK	C_{12}	10.0	14.0	pF
Input Capacitance: CKE	C_{13}	18.0	27.0	pF

I_{DD} Specifications AND CONDITIONS

(0°C ≤ T_A ≤ + 70°C; V_{DDQ} = +2.5V ± 0.2V, V_{DD} = +2.5V ± 0.2V) see Note 1 on Page 9

Parameter & Test Condition	Symbol	max.		Unit
		3200-3.033	2700-2.533	
OPERATING CURRENT; *) : One device bank; Active-Precharge; t_{RC}= t_{RC} (Min); t_{CK} = t_{CK} (Min); DQ, DM and DQS inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I_{DD0}	1240	1040	mA
OPERATING CURRENT;*) One device bank; Active-Read-Precharge; Burst = 2; t_{RC}= t_{RC} (Min); t_{CK} = t_{CK} (Min);I_{OUT} = 0mA; Address and control inputs changing once per clock cycle	I_{DD1}	1480	1280	mA
PRECHARGE POWER-DOWN STANDBY CURRENT; All device banks idle; Power-down mode; t_{CK} = t_{CK} (Min); CKE = (LOW)	I_{DD2P}	40	40	mA
IDLE STANDBY CURRENT; CS# = HIGH; All device banks idle; t_{CK} = t_{CK} (Min); CKE= HIGH; Address and other control inputs changing once per clock cycle. V_{IN} = V_{REF} for DQ, DQS, and DM	I_{DD2F}	440	360	mA
PRECHARGE QUIET STANDBY CURRENT; CS# > V_{IH}(min); All banks idle; CKE >= V_{IH}(min); t_{CK}=6ns for DDR333, 5ns for DDR400; Address and other control iputs stable at >=V_{IH}(min) or =< V_{IL}(max); V_{IN}=V_{REF} for DQ, DQS and DM	I_{DD2Q}	N/A	N/A	mA
ACTIVE POWER-DOWN STANDBY CURRENT; One device bank active; Power-down mode; t_{CK} = t_{CK} (Min);CKE = LOW	I_{DD3P}	360	280	mA
ACTIVE STANDBY CURRENT; CS# = HIGH; CKE = HIGH; One device bank; Active-Precharge; t_{RC}= t_{RAS} (Max); t_{CK} = t_{CK} (Min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	I_{DD3N}	480	400	mA
OPERATING CURRENT; Burst = 2; Reads; Continous burst; One bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (Min); I_{OUT} = 0mA	I_{DD4R}	1520	1320	mA
OPERATING CURRENT; Burst = 2; Writes; Continuous burst; One device bank active; Address and control inputs changing once per clock cycle; t_{CK} = t_{CK} (Min); DQ, DM, and DQS inputs changing twice per clock cycle	I_{DD4W}	1560	1400	mA
AUTO REFRESH CURRENT; t_{RC} = t_{RC} (Min)	I_{DD5}	2760	2320	mA
SELF REFRESH CURRENT; CKE ≤ 0.2V;External clock on; Tck=6ns for DDR333, 5ns for DDR400	$I_{DD6(normal)}$	40	40	mA
	$I_{DD6(Low\ power)}$	N/A	N/A	mA
OPERATING CURRENT – FOUR BANK OPERATION; Four bank interleaving with BL=4	I_{DD7A}	3600	3240	mA

***) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.**

DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$; $V_{DDQ} = +2.5V \pm 0.2V$, $V_{DD} = +2.5V \pm 0.2V$) see Note 1 on Page 9

AC CHARACTERISTICS			3200-3.0-3-3		2700-2.5-3-3		
PARAMETER		**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**Unit**
Access window of DQS CK/CK#		t_{AC}	-0.65	+0.65	-0.65	+0.65	ns
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	t_{CK}
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	t_{CK}
Clock cycle time	CL=2.0	$t_{CK\ (2.0)}$	7.5	13.0	7.5	13.0	ns
	CL=2.5	$t_{CK(2.5)}$	6.0	13.0	6.0	13.0	
	CL=3.0	$t_{CK\ (3.0)}$	5.0	13.0	-	-	
DQ and DM input hold time relative to DQS		t_{DH}	0.40	-	0.45	-	ns
DQ and DM input setup time relative to DQS		t_{DS}	0.40	-	0.45	-	ns
DQ and DM input pulse width (for each input)		t_{DIPW}	1.75	-	1.75	-	ns
Access window of DQS from CK/CK#		t_{DQSCK}	-0.6	+0.6	-0.6	+0.6	ns
DQS input high pulse width		t_{DQSH}	0.35	-	0.35	-	t_{CK}
DQS input low pulse width		t_{DQSL}	0.35	-	0.35	-	t_{CK}
DQS –DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	-	0.40	-	0.45	ns
Write command to first DQS latching transition		t_{DQSS}	0.72	1.28	0.75	1.25	t_{CK}
DQS falling edge to CK rising- setup time		t_{DSS}	0.2	-	0.2	-	t_{CK}
DQS falling edge from CK rising- hold time		t_{DSH}	0.2	-	0.2	-	t_{CK}
Half clock period		t_{HP}	t_{CH}, t_{CL}	-	t_{CH}, t_{CL}	-	ns
Data-out high-impedance window from CK/CK#		t_{HZ}	-0.7	+0.7	-0.7	+0.7	ns
Data-out low-impedance window from CK/CK#		t_{LZ}	-0.7	+0.7	-0.7	+0.7	ns
Address and control input hold time (fast slew rate)		t_{IHF}	0.6	-	0.75	-	ns
Address and control input setup time (fast slew rate)		t_{ISF}	0.6	-	0.75	-	ns
Address and control input hold time (slow slew rate)		t_{IHS}	0.7	-	0.8	-	ns
Address and control input setup time (slow slew rate)		t_{ISS}	0.6	-	0.8	-	ns
LOAD MODE REGISTER command cycle time		t_{MRD}	10	-	12	-	ns
Adress and control input pulse width (for each input)		t_{IPW}	2.2	-	2.2	-	ns
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}		t_{HP} - t_{QHS}		ns
Data hold skew factor		t_{QHS}	-	0.5	-	0.6	ns

AC CHARACTERISTICS		3200-3.0-3-3		2700-2.5-3-3		
PARAMETER	**SYMBOL**	**MIN**	**MAX**	**MIN**	**MAX**	**Unit**
ACTIVE to PRECHARGE command	t_{RAS}	40	70'000	42	70'000	ns
ACTIVE to READ with Auto precharge command	t_{RAP}	15	-	15	-	ns
ACTIVE to ACTIVE/AUTO REFRESH command period	t_{RC}	55	-	60	-	ns
AUTO REFRESH command period	t_{RFC}	70	-	72	-	ns
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	18	-	ns
PRECHARGE command period	t_{RP}	15	-	18	-	ns
DQS read preamble	t_{RPRE}	0.9	1.1	0.9	1.1	t_{CK}
DQS read postamble	t_{RPST}	0.4	0.6	0.4	0.6	t_{CK}
ACTIVE bank *a* to ACTIVE bank *b* command	t_{RRD}	10	-	12	-	ns
DQS write preamble	t_{WPREH}	0.25	-	0.25	-	t_{CK}
DQS write preamble setup time	t_{WPRES}	0	-	0	-	ns
DQS write postamble	t_{WPST}	0.4	0.6	0.4	0.6	t_{CK}
Write recovery time	t_{WR}	15	-	15	-	ns
Internal WRITE to READ command delay	t_{WTR}	2	-	1	-	t_{CK}
Data valid output window	N/A	t_{QH} - t_{DQSQ}		t_{QH} - t_{DQSQ}		ns
REFRESH to REFRESH command interval	t_{REFC}	-	70.3	-	70.3	µs
Average periodic refresh interval 0 °C ≤ T_{CASE} ≤ 85°C	t_{REFI}	-	7.8	-	7.8	µs
85 °C < T_{CASE} ≤ 95°C	$t_{REFI\ (IT)}$		3.9		3.9	
Terminating voltage delay to V_{DD}	t_{VTD}	0	-	0	-	ns
Exit SELF REFRESH to non-READ command	t_{XSNR}	70	-	75	-	ns
Exit SELF REFRESH to READ command	t_{XSRD}	200	-	200	-	t_{CK}

Note 1: Values for AC timing, IDD, and electrical AC and DC characteristics might have been collected within the standard temperature range and at nominal reference/supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified and for the corresponding field of operation according to the actual temperature grade of the module (extended E, I or W; refer to the environmental conditions for more details).

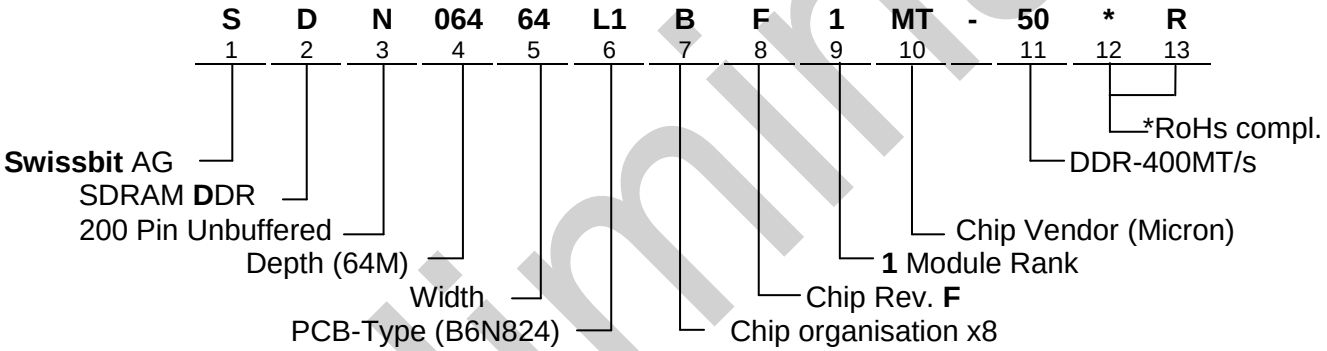
SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	3200-3.0-3-3	2700-2.5-3-3
0	NUMBER OF SPD BYTES USED	0x80	
1	TOTAL NUMBER OF BYTES IN SPD DEVICE	0x08	
2	FUNDAMENTAL MEMORY TYPE	0x07	
3	NUMBER OF ROW ADDRESSES ON ASSEMBLY	0x0D	
4	NUMBER OF COLUMN ADDRESSES ON ASSEMBLY	0x0B	
5	NUMBER OF PHYSICAL BANKS ON DIMM	0x01	
6	MODULE DATA WIDTH	0x40	
7	MODULE DATA WIDTH (continued)	0x00	
8	MODULE VOLTAGE INTERFACE LEVELS (V_{DDQ})	0x04	
9	SDRAM CYCLE TIME, (t_{CK}) (CAS LATENCY =2.5 (2700, 2100) ; CL=3* (3200)	0x50	0x60
10	SDRAM ACCESS FROM CLOCK, (t_{AC}) (CAS LATENCY =2.5 (2700, 2100); CL=3* (3200))	0x70	
11	MODULE CONFIGURATION TYPE	0x00	
12	REFRESH RATE/ TYPE	0x82	
13	SDRAM DEVICE WIDTH (PRIMARY SDRAM)	0x08	
14	ERROR- CHECKING SDRAM DATA WIDTH	0x00	
15	MINIMUM CLOCK DELAY, BACK- TO- BACK RANDOM COLUMN ACCESS	0x01	
16	BURST LENGTHS SUPPORTED	0x0E	
17	NUMBER OF BANKS ON SDRAM DEVICE	0x04	
18	CAS LATENCIES SUPPORTED	0x1C	0x0C
19	CS LATENCY	0x01	
20	WE LATENCY	0x02	
21	SDRAM MODULE ATTRIBUTES	0x20	
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0xC0	
23	SDRAM CYCLE TIME, (t_{CK}) (CAS LATENCY=2(2700, 2100) CL=2,5*(3200))	0x60	0x75
24	SDRAM ACCESS FROM CK, (t_{AC}) (CAS LATENCY=2(2700, 2100) CL=2.5*(3200)	0x70	
25	SDRAM CYCLE TIME, (t_{CK}) (CAS LATENCY=1.5(2700, 2100) CL=2*(3200))	0x75	0x00
26	SDRAM ACCESS FROM CK, (t_{AC}) (CAS LATENCY=1.5(2700, 2100) CL=2*(3200)	0x75	0x00
27	MINIMUM ROW PRECHARGE TIME, (t_{RP})	0x3C	0x48
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, (t_{RRD})	0x28	0x30
29	MINIMUM RAS# TO CAS# DELAY, (t_{RCD})	0x3C	0x48
30	MINIMUM RAS# PULSE WIDTH, (t_{RAS})	0x28	0x2A
31	MODULE BANK DENSITY	0x80	
32	ADDRESS AND COMMAND SETUP TIME, (t_{IS})	0x60	0x80
33	ADDRESS AND COOMAND HOLD TIME, (t_{IH})	0x60	0x80
34	DATA/DATA MASK INPUT SETUP TIME, (t_{DS})	0x40	0x45
35	DATA/DATA MASK INPUT HOLD TIME, (t_{DH})	0x40	0x45
36-40	RESERVED	0x00	
41	MIN ACTIVE AUTO REFRESH TIME (t_{RC})	0x37	0x3C
42	MINIMUM AUTO REFRESH TO ACTIVE/ AUTO REFRESH COMMAND PERIOD, (t_{RFC})	0x46	0x48
43	SDRAM DEVICE MAX CYCLE TIME (t_{CKMAX})	0x30	
44	SDRAM DEVICE MAX DQS-DQ SKEW TIME (t_{DQSQ})	0x28	0x2D
45	SDRAM DEVICE MAX READ DATA HOLD SKEW FACTOR (t_{QHS})	0x50	0x55

SERIAL PRESENCE-DETECT MATRIX (continued)

BYTE	DESCRIPTION	3200-3.0-3-3	2700-2.5-3-3
46-61	RESERVED	0x00	
62	SPD REVISION	0x11	
63	CHECKSUM FOR BYTES 0-62	0xC0	0x68
64	MANUFACTURER`S JEDEC ID CODE	7F	
65	MANUFACTURER`S JEDEC ID CODE(continued)	7F	
66	MANUFACTURER`S JEDEC ID CODE(continued)	7F	
67	MANUFACTURER`S JEDEC ID CODE(continued)	DA	
72	MANUFACTURING LOCATION	CH = 0x01 / GE = 0x02 / US = 0x03	
73-90	MODULE PART NUMBER (ASCII)	"SDN06464L1BF1MT-xx"	
91	PCB IDENTIFICATION CODE	X	
92	PCB IDENTIFICATION CODE (continued)	X	
93	YEAR OF MANUFACTURE IN BCD	X	
94	WEEK OF MANUFACTURE IN BCD	X	
95-98	MODULE SERIAL NUMBER	X	
99-127	MANUFACTURER-SPECIFIC DATA (RSVD)	X	

Part Number Code



* optional / additional information

Revision History		
Revision	Changes	Date
0.9	Preliminary Version	31.07.2013

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CE Declaration of Conformity

We

Manufacturer: **Swissbit AG**
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declare under our sole responsibility that the product

Product Type: **512MB DDR1 SODIMM**
Brand Name: **SWISSMEMORY™**
Product Series: **DDR1 SODIMM**
Part Number: **SDN06464L1BF1MT-xxxR**

to which this declaration relates is in conformity with the following directives:

2002/96/EC Category 3 (WEEE)

following the provisions of Directive

Restriction of the use of certain hazardous substances 2011/65/EU

Swissbit AG, July 2013

Manuela Kögel
Head of Quality Management