M64892AFP/GP

SERIAL INPUT PLL FREQUENCY SYNTHESIZER FOR TV/VCR

DESCRIPTION

The M64892 is a semiconductor integrated circuit consisting of PLL frequency synthesizer for TV/VCR using Bip process. It contains the prescaler with operating up to 1.0GHz, 4 band drivers and Op. Amp for direct tuning.

FEATURES

- 4 integrated PNP band drivers (Io=40mA,Vsat=0.2V typ@V_{CC1} to 13.2V)
- Built-in Op. Amp for direct tuning voltage output (33V)
- Low power dissipation (Icc=20mA, V_{CC1}=5V)
- Built-in prescaler with input amplifier (Fmax=1.0GHz)
- PLL lock/unlock status display out put (Built-in pull up resistor)
- X'tal 4MHz is used to realize 3 type of tuning steps (Division ratio 1/512, 1/640, 1/1024)
- Serial data input. (3 wire bus)
- Software and pin compatible with M64092/M64892
- Automatic switching of tuning step according to the number of data bits (62.5kHz at 18bits, 31.25kHz at 19bits)
- Built-in Power on reset system
- 16-pin small SOP/SSOP package

APPLICATION

TV, VCR tuners

RECOMMENDED OPERATING CONDITION

Supply voltage range.....V_{CC1}=4.5 to 5.5V

V_{CC2}=V_{CC1} to 13.2V

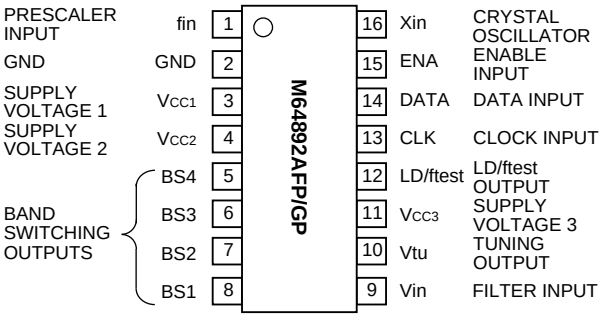
V_{CC3}=28 to 35V

Rated supply voltage.....V_{CC1}=5V

V_{CC2}=12V

V_{CC3}=33V

PIN CONFIGURATION (TOP VIEW)

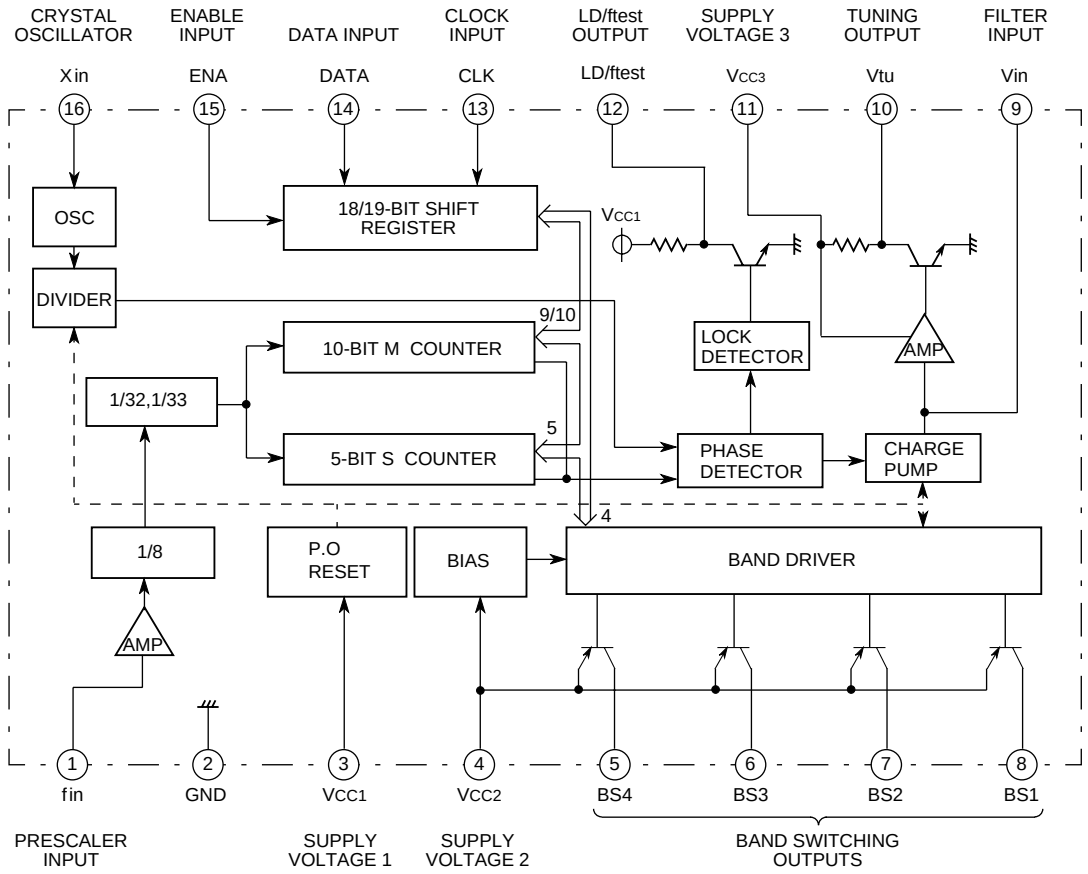


Outline 16P2S-A (AFP)
16P2Z-A (AGP)

FUNCTION

- 2-modulus prescaler (1/32 and 1/33)
- Built-in 4MHz crystal oscillator and reference divider
- Programmable divider (10-bit M counter, 5-bit S counter)
- Tri-state phase comparator
- Lock detector
- Band switch driver
- Op. Amp for direct tuning

BLOCK DIAGRAM



DESCRIPTION OF PIN

Pin No.	Symbol	Pin name	Function
1	fin	Prescaler input	Input for the VCO frequency.
2	GND	GND	Ground to 0V.
3	V_{CC1}	Power supply voltage 1	Power supply voltage terminal. 5.0V±0.5V
4	V_{CC2}	Power supply voltage 2	Power supply for band switching, V_{CC1} to 13.2V
5 6 7 8	BS4 BS3 BS2 BS1	Band switching outputs	PNP open collector method is used. When the band switching data is "H", the output is ON. When it is "L", the output is OFF.
9	Vin	Filter input (Charge pump output)	This is the output terminal for the LPF input and charge pump output. When the phase of the programmable divider output (f1/N) is ahead compared to the reference frequency (fref), the "source" current state becomes active. If it is behind, the "sink" current becomes active. If the phases are the same, the high impedance state becomes active.
10	Vtu	Tuning output	This supplies the tuning voltage.
11	V_{CC3}	Power supply voltage 3	Power supply voltage for tuning voltage 28 to 35V
12	LD/ftest	Lock detect/Test port	When 18/19 bit data is input, lock detector is output. When 27 bit data is input, lock detector is output, the programmable freq. Divider output and reference freq. Output is selected by the test mode.
13	CLK	Clock input	Data is read into the shift register when the clock signal falls.
14	DATA	Data input	Input for band SW and programmable freq. divider set up.
15	ENA	Enable input	This is normally at a "L". When this is at "H", data and clock signals are received. Data is read into the latch when the enable signal after the 18th signal of the clock signal falls or when the 19th pulse of the clock signal falls.
16	Xin	This is connected to the crystal oscillator	4.0MHz crystal oscillator is connected.

ABSOLUTE MAXIMUM RATINGS (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage 1	Pin3	6.0	V
V_{CC2}	Supply voltage 2	Pin4	14.4	V
V_{CC3}	Supply voltage 3	Pin11	36.0	V
V_I	Input voltage	Not to exceed V_{CC1}	6.0	V
V_O	Output voltage	LD output	6.0	V
V_{BSOFF}	Voltage applied when the band output is OFF		14.4	V
I_{BSON}	Band output current	Per 1 band output circuit	50.0	mA
t_{BSON}	ON the time when the band output is ON	50mA per 1 band output circuit 3circuits are pn at same time	10	sec
P_d	Power dissipation	Ta=+75°C (SOP/SSOP)	FP: 450 (GP: 470)	mW
T_{opr}	Operating temperature		-20 to +75	°C
T_{stg}	Storage temperature		-40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (Ta=-20°C to +75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC1}	Supply voltage 1		4.5 to 5.5	V
V_{CC2}	Supply voltage 2		V_{CC1} to 13.2	V
V_{CC3}	Supply voltage 3		28 to 35	V
f_{opr1}	Operating frequency (1)	Crystal oscillation circuit	4.0	MHz
f_{opr2}	Operating frequency (2)		80 to 1,000	MHz
I_{BDL}	Band output current 5 to 8	Normally 1 circuit is ON. 2 circuits on at the same time is max. It is prohibited to have 3 or more circuits turned on at the same time.	0 to 40	mA

ELECTRICAL CHARACTERISTICS (Ta=-20°C to +75°C, V_{CC1}=5.0V, V_{CC2}=12V, V_{CC3}=33V, unless otherwise noted)

Symbol	Parameter		Test pin	Test conditions	Limits			Unit
					Min.	Typ.	Max.	
V_{IH}	Input pin	"H" input voltage	13 to 15		3.0	–	V_{CC1}+0.3	V
V_{IL}		"L" input voltage	13 to 15		–	–	1.5	V
I_{IH}		"H" input current	13 to 15	V_{CC1}=5.5V, Vi=4.0V	–	–	10	µA
I_{IL}		"L" input current	13, 15	V_{CC1}=5.5V, Vi=0.4V	–	-6	-20	µA
		"L" input current	14	V_{CC1}=5.5V, Vi=0.4V	–	-18	-30	µA
V_{OH}	Lock output	"H" output voltage	12	V_{CC1}=5.5V	5.0	–	–	V
V_{OL}		"L" output voltage	12	V_{CC1}=5.5V	–	0.3	0.5	V
V_{BS}	Band SW	Output voltage	5 to 8	V_{CC2}=12V, Io=-40mA	11.6	11.8	–	V
I_{OLK1}		Leak current	5 to 8	V_{CC2}=12V band SW is OFF	–	–	-10	µA
V_{TOH}	Tuning output	Output voltage "H"	10	V_{CC3}=33V	32.5	–	–	V
V_{TOL}		Output voltage "L"	10	V_{CC3}=33V	–	0.2	0.4	V
I_{OH}	Charge pump	"H" output current	9	V_{CC1}=5.0V, Vo=2.5V	–	±270	±370	µA
I_{OL}		"L" output current	9	V_{CC1}=5.0V, Vo=2.5V	–	±70	±110	µA
I_{CPLK}		Leak current	9	V_{CC1}=5.0V, Vo=2.5V	–	–	±50	nA
I_{CC1}	Supply current 1		3	V_{CC1}=5.5V	–	20	30	mA
I_{CC2A}	Supply current 2	4 circuits: OFF	4	V_{CC2}=12V	–	–	0.3	mA
I_{CC2B}		1 circuits: ON, Output: OPEN	4	V_{CC2}=12V	–	6.0	8.0	mA
I_{CC2C}		1 circuits: ON, Output current 40mA	4	V_{CC2}=12V Io=-40mA	–	46.0	48.0	mA
I_{CC3}	Supply current 3		11	V_{CC3}=33V Output ON	–	3.0	4.0	mA

Note. Typical values are measured at V_{CC1}=5.0V, V_{CC2}=12V, V_{CC3}=33V and Ta=+25°C.

SWITCHING CHARACTERISTICS (Ta=-20°C to +75°C, V_{CC1}=5.0V, V_{CC2}=12V, V_{CC3}=33V, unless otherwise noted)

Symbol	Parameter	Test pin	Test conditions		Limits			Unit
					Min.	Typ.	Max.	
f_{opr}	Prescaler operating frequency	1	V_{CC1}=4.5 to 5.5V Vin=Vinmin to Vinmax		80	–	1000	MHz
Vin	Operating input voltage	1	V_{CC1}=4.5 to 5.5V	80 to 100MHz	-24	–	4	dBm
				100 to 200MHz	-27	–	4	
				200 to 800MHz	-30	–	4	
				800 to 1000MHz	-27	–	4	
t_{PWC}	Clock pulse width	13	V_{CC1}=4.5 to 5.5V		1	–	–	µs
$t_{SU\ (D)}$	Data setup time	14	V_{CC1}=4.5 to 5.5V		2	–	–	µs
$t_{H\ (D)}$	Data hold time	14	V_{CC1}=4.5 to 5.5V		1	–	–	µs
$t_{SU\ (E)}$	Enable setup time	15	V_{CC1}=4.5 to 5.5V		3	–	–	µs
$t_{H\ (E)}$	Enable hold time	15	V_{CC1}=4.5 to 5.5V		3	–	–	µs
t_{INT}	Enable data interval time	15, 14	V_{CC1}=4.5 to 5.5V		1	–	–	µs
t_r	Rise time	13, 14, 15	V_{CC1}=4.5 to 5.5V		–	–	1	µs
t_f	Fall time	13, 14, 15	V_{CC1}=4.5 to 5.5V		–	–	1	µs
t_{bt}	Next enable prohibit time	15	V_{CC1}=4.5 to 5.5V		5	–	–	µs
t_{bcl}	Next clock prohibit time	13, 15	V_{CC1}=4.5 to 5.5V		5	–	–	µs

METHOD OF SETTING DATA

The frequency demultiplying ratio uses 15bits. Setting up the band switching output uses 4bits.

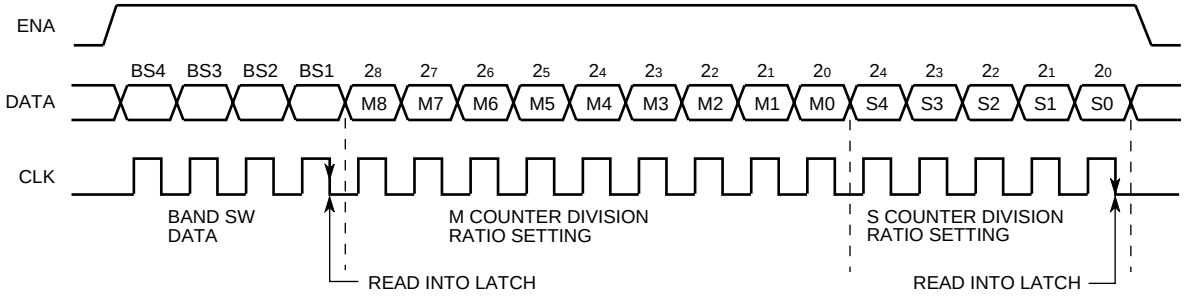
The test mode data uses 8bits. The total bits used is 27bits. Data is read in when the enable signal is "H" and the clock signal falls.

The band switching data is read in at the 4th pulse of the clock signal. The program counter data is read into the latch by the fall of the enable signal after the 18th pulse of the clock signal or the fall of the 19th pulse of the clock signal. When the enable signal goes to "L" before the 18th pulse of the enable signal, only the band SW data is updated and other data is ignored.

The shift register is equipped with the 18/19 bit automatic decision function. When the 18th bit data is used, the M9 bit of the program counter is reset and the 1/512 division of the reference frequency is set. In case of the 19th bit, 1/1024 division of the reference frequency is set.

(1) Transfer of the 18th bit data

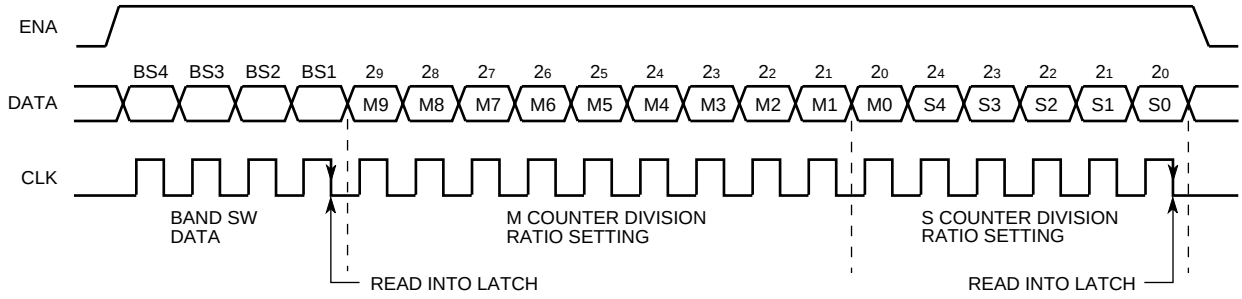
Data is latched by the fall of the enable signal after the 18th clock signal. At this time, the division of the 1/512 of the reference frequency is used.



(2) Transfer of the 19th bit data

The data is latched at the 19th pulse of the clock signal. At this time, 1/1024 frequency division ratio is used. Clock signals after the above are invalid.

Notice) To change reference frequency, set up as ENA in "L" after 19th pulse of clock signal by all means



METHOD OF SET THE DIVIDING RATIO OF THE PROGRAMMABLE DIVIDER

(1) Transfer of the 18th bit data

Total division N is given by the following formulas in addition to the prescaler used in the previous stage.

N=8 (32M+S) M:9 bit main counter division

S:5 bit swallow counter division

The M and S counters are binary the possible ranges of division are as follows.

32≤M≤511

0≤S≤31

Therefore, the range of division N is 8,192 to 131,064.

The tuning frequency f_{VCO} is given in the following equations.

$f_{VCO} = f_{REF} \times N$

$= 7.8125 \times 8 \times (32M+S)$

$= 62.5 \times (32M+S)$ [kHz]

Therefore, the tuning frequency range is 64MHz to 1023.9375MHz.

(2) Transfer of the 19th bit data

Total division N is given by the following formulas in addition to the prescaler used in the previous stage.

N=8 (32M+S) M:10 bit main counter division

S:5 bit swallow counter division

The M and S counters are binary the possible ranges of division are as follows.

32≤M≤1023

0≤S≤31

Therefore, the range of division N is 8,192 to 262,136.

The tuning frequency f_{VCO} is given in the following equations.

$f_{VCO} = f_{REF} \times N$

$= 3.90625 \times 8 \times (32M+S)$

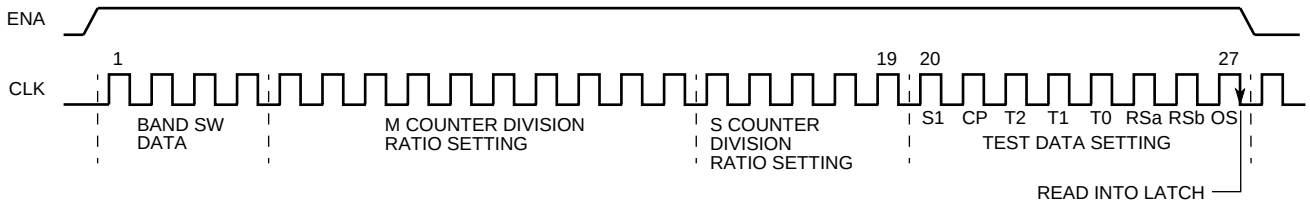
$= 31.25 \times (32M+S)$ [kHz]

Therefore, the tuning frequency range is 32MHz to 1023,9687MHz.

TEST MODE DATA SET UP METHOD

The data for the test mode uses 20 to 27bits. Data is latched when the 27th clock signal falls.

(1) When transferring 3-wire 27bit data



(2)Test mode bit set up

X :Random, 0 or 1. normal “0”
CP :Set up the charge pump current value
T0, T1, and T2 :Set up test modes
RSa, RSb :Set up for the reference frequency division ratio
OS :Set up the tuning amplifier
SI :1 only (It is prohibit to “0”)

Setting up the charge pump current of the phase comparator

CP	Charge pump current	Mode
0	70μA	Test
1	270μA	Normal

Setting up for the test mode

T2	T1	T0	Charge pump	12 pin output	Mode
0	0	X	Normal operation	LD	Normal operation
0	1	X	High impedance	LD	Test mode
1	1	0	Sink	LD	Test mode
1	1	1	Source	LD	Test mode
1	0	0	High impedance	f_{REF}	Test mode
1	0	1	High impedance	f1/N	Test mode

∗ Built-in pull up resistor, and the resistor is unnecessary.

Set up for the reference frequency division ratio

RSa	RSb	Frequency ratio
1	1	1/512
0	1	1/1024
X	0	1/640

Set up the tuning amplifier

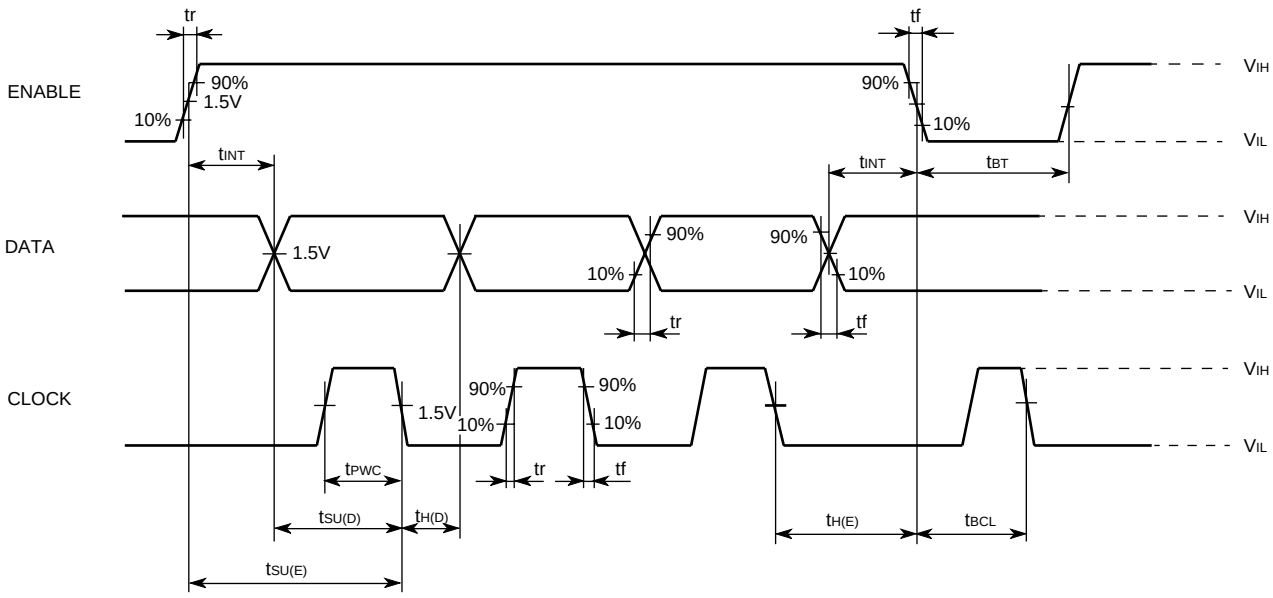
OS	Tuning voltage output	Mode
0	ON	Normal
1	OFF	Test

POWER ON RESET OPERATION

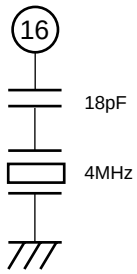
(Initial state the power is turned ON)

BS4 to BS1 : OFF
Charge pump : High impedance
Tuning amplifier : OFF
Charge pump current : 270μA
Frequency division ratio : 1/1024
Lock detect : “H”

TIMING DIAGRAM

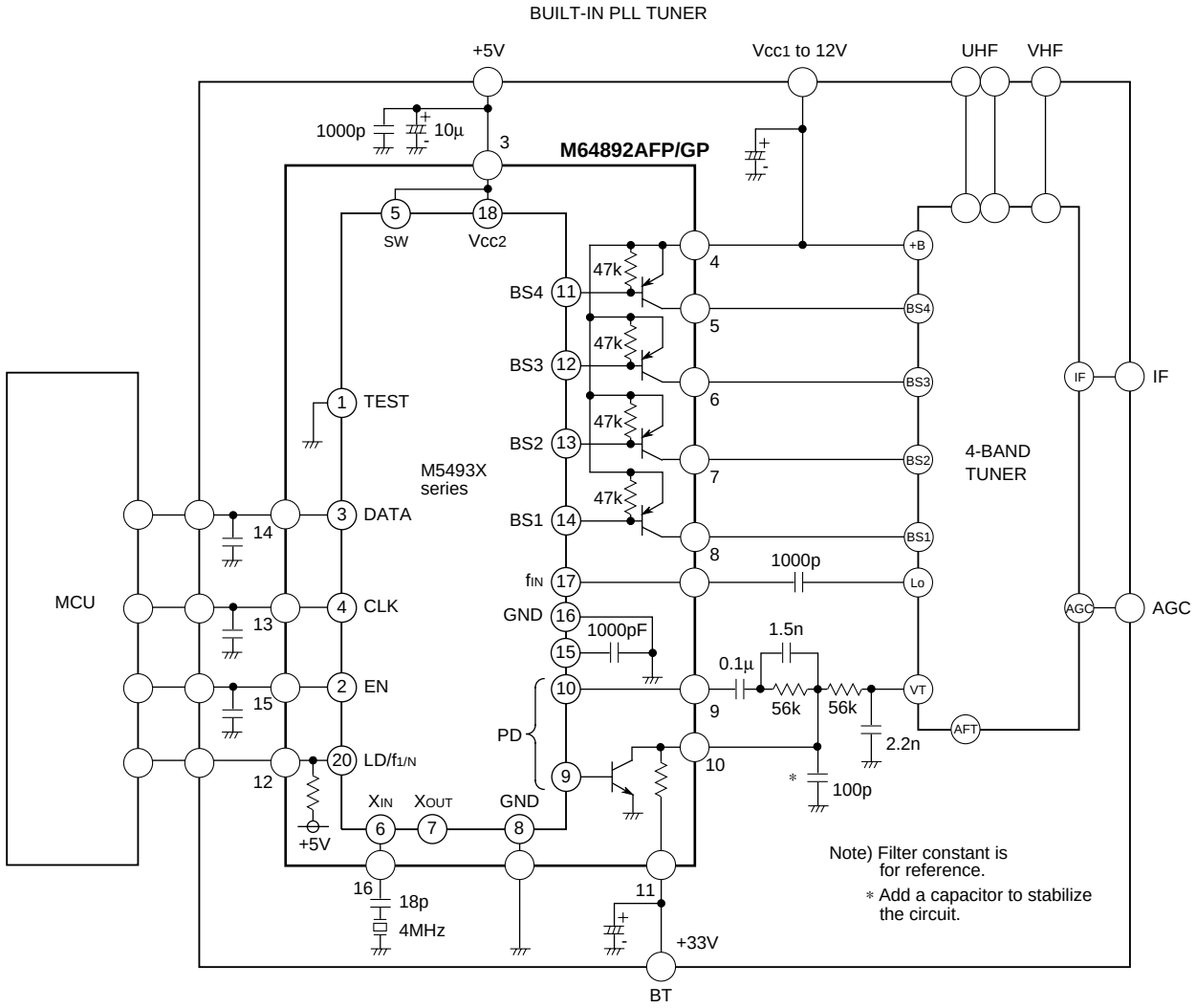


CRYSTAL OSCILLATOR CONNECTION DIAGRAM



Crystal oscillator characteristics
Actual resistance: less then 300Ω
Load capacitance : 20pF

APPLICATION EXAMPLE



Units Resistance : Ω
Capacitance : F