Data Sheet April 1999 File Number 2269.2

## 16A, 50V, 0.047 Ohm, Logic Level, N-Channel Power MOSFETs

These are N-Channel logic level power MOSFETs manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use with logic level (5V) driving sources in applications such as programmable controllers, automotive switching, switching regulators, switching converters, motor relay drivers and emitter switches for bipolar transistors. This performance is accomplished through a special gate oxide design which provides full rated conductance at gate biases in the 3V to 5V range, thereby facilitating true on-off power control directly from logic circuit supply voltages.

Formerly developmental type TA09871.

## Ordering Information

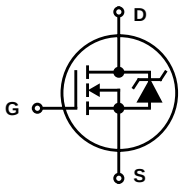
| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| RFD16N05L | TO-251AA | RFD16N05L |
| RFD16N05LSM | TO-252AA | RFD16N05LSM |

NOTE: When ordering, include the entire part number. Add the suffix 9A to obtain the TO-252AA variant in tape and reel, i.e. RFD16N05LSM9A

## Features

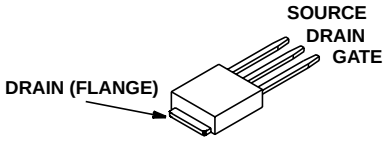
- 16A, 50V
- $r_{DS(ON)} = 0.047\Omega$
- UIS SOA Rating Curve (Single Pulse)
- Design Optimized for 5V Gate Drives
- Can be Driven Directly from CMOS, NMOS, TTL Circuits
- Compatible with Automotive Drive Requirements
- SOA is Power Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device
- Related Literature
  - TB334 “Guidelines for Soldering Surface Mount Components to PC Boards”

## Symbol

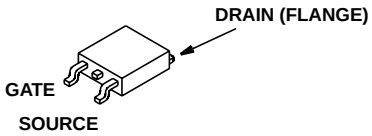



## Packaging

**JEDEC TO-251AA**




**JEDEC TO-252AA**






CAUTION: These devices are sensitive to electrostatic discharge; follow proper ESD Handling Procedures.
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## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | RFD16N05L, RFD16N05LSM | UNITS |
|---|---|---|---|
| Drain to Source Voltage (Note 1) | $V_{DS}$ | 50 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) | $V_{DGR}$ | 50 | V |
| Continuous Drain Current | $I_D$ | 16 | A |
| Pulsed Drain Current (Note 3) | $I_{DM}$ | 45 | A |
| Gate to Source Voltage | $V_{GS}$ | ±10 | V |
| Maximum Power Dissipation | $P_D$ | 60 | W |
| Derate Above $25^oC$ | | 0.48 | $W/^oC$ |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | -55 to 150 | $^oC$ |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | $^oC$ |
| Package Body for 10s, See Techbrief 334 | $T_{pkg}$ | 260 | $^oC$ |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $T_J = 25^oC$ to $125^oC$.

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 250mA, $V_{GS}$ = 0V, Figure 10 | | 50 | - | - | V |
| Gate to Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D$ = 250mA, Figure 9 | | 1 | - | 2 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 40V, $V_{GS}$ = 0V | | - | - | 1 | µA |
| | | $T_C = 150^oC$ | | - | - | 50 | µA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±10V, $V_{DS}$ = 0V | | - | - | 100 | nA |
| Drain to Source On Resistance (Note 2) | $r_{DS(ON)}$ | $I_D$ = 16A, $V_{GS}$ = 5V | | - | - | 0.047 | Ω |
| | | $I_D$ = 16A, $V_{GS}$ = 4V | | - | - | 0.056 | Ω |
| Turn-On Time | $t_{(ON)}$ | $V_{DD}$ = 25V, $I_D$ = 8A, $V_{GS}$ = 5V, $R_{GS}$ = 12.5Ω Figures 15, 16 | | - | - | 60 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 14 | - | ns |
| Rise Time | $t_r$ | | | - | 30 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 42 | - | ns |
| Fall Time | $t_f$ | | | - | 14 | - | ns |
| Turn-Off Time | $t_{(OFF)}$ | | | - | - | 100 | ns |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS}$ = 0V to 10V | $V_{DD}$ = 40V, $I_D$ = 16A, $R_L$ = 2.5Ω Figures 17, 18 | - | - | 80 | nC |
| Gate Charge at 5V | $Q_{g(5)}$ | $V_{GS}$ = 0V to 5V | | - | - | 45 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS}$ = 0V to 1V | | - | - | 3 | nC |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | | | - | - | 2.083 | $^oC/W$ |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | | | - | - | 100 | $^oC/W$ |

## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Diode Voltage | $V_{SD}$ | $I_{SD}$ = 16A | - | - | 1.5 | V |
| Diode Reverse Recovery Time | $t_{rr}$ | $I_{SD}$ = 16A, $dI_{SD}/dt$ = 100A/µs | - | - | 125 | ns |

NOTES:

2. Pulse Test: Pulse Width ≤ 300ms, Duty Cycle ≤ 2%.
3. Repetitive Rating: Pulse Width limited by max junction temperature.

## Typical Performance Curves Unless Otherwise Specified

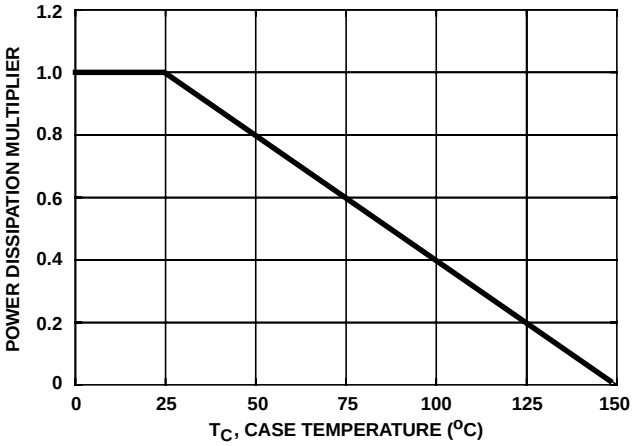



FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

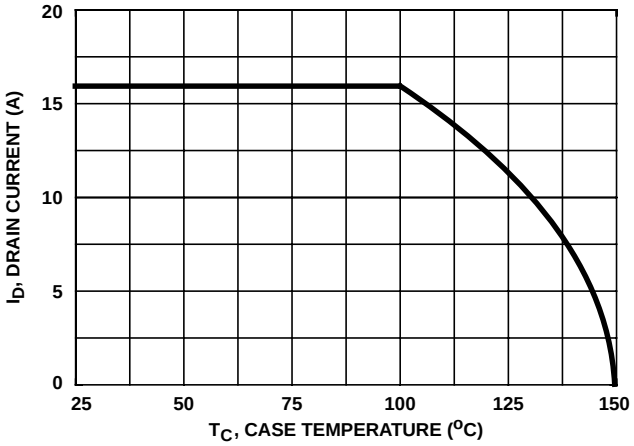



FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

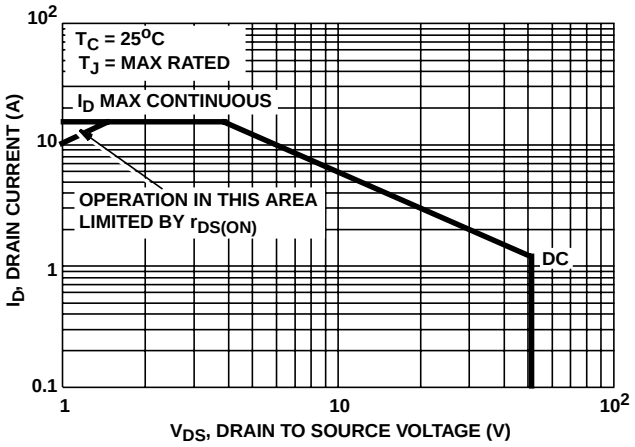



FIGURE 3. FORWARD BIAS SAFE OPERATING AREA

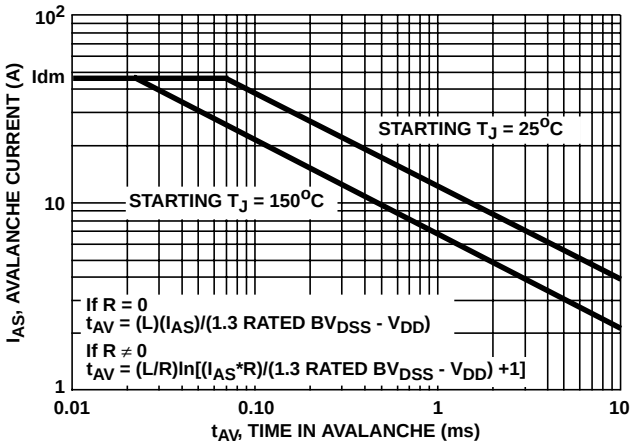



FIGURE 4. UNCLAMPED INDUCTIVE SWITCHING SOA (SINGLE PULSE UIS SOA)

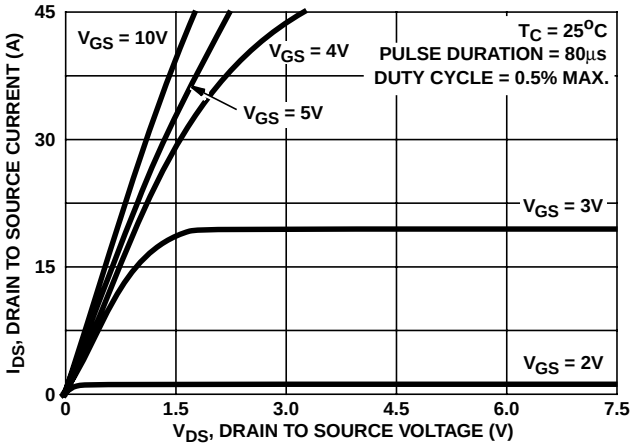



FIGURE 5. SATURATION CHARACTERISTICS

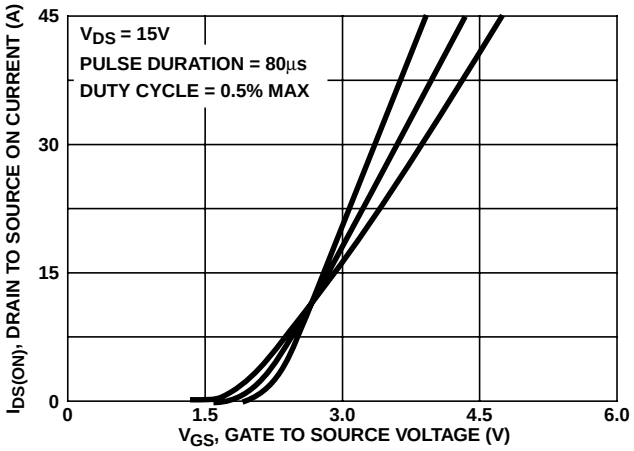



FIGURE 6. TRANSFER CHARACTERISTICS

## Typical Performance Curves Unless Otherwise Specified (Continued)

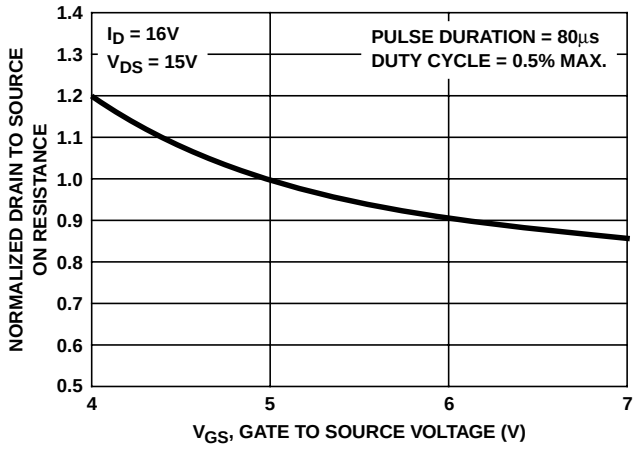



FIGURE 7. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

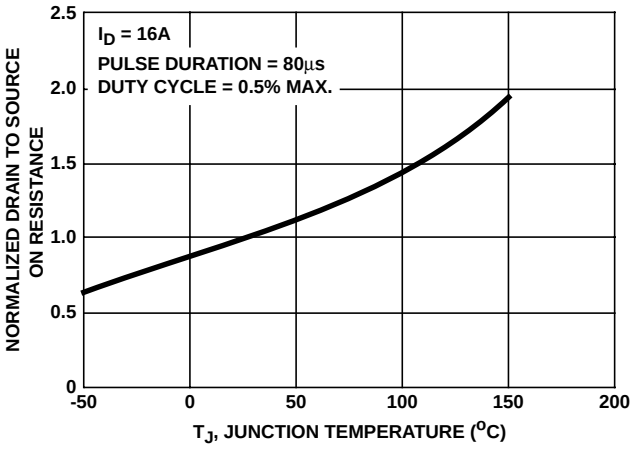



FIGURE 8. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

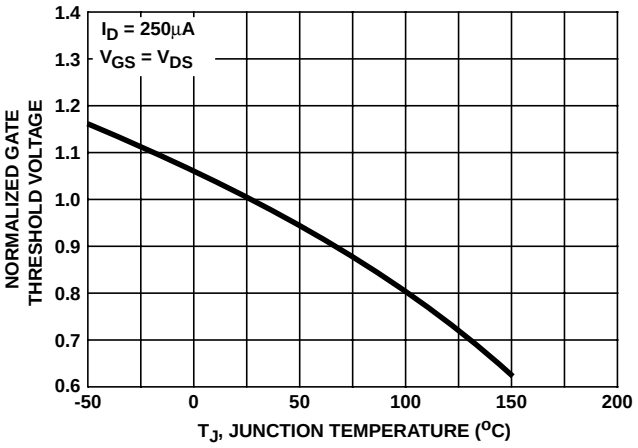



FIGURE 9. NORMALIZED GATE THRESHOLD vs JUNCTION TEMPERATURE

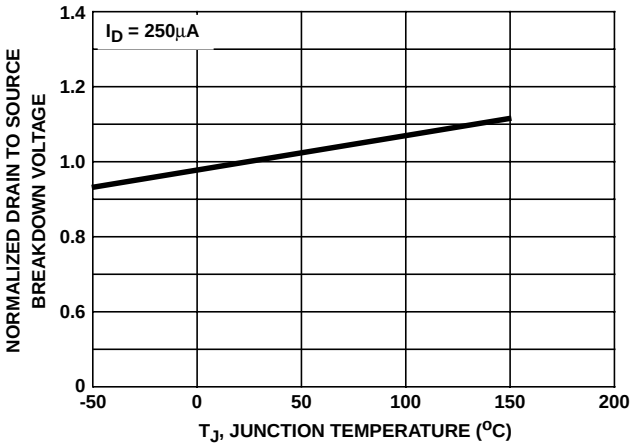



FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

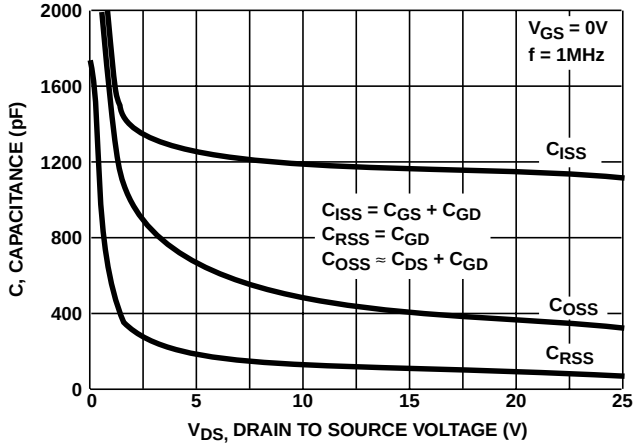



FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

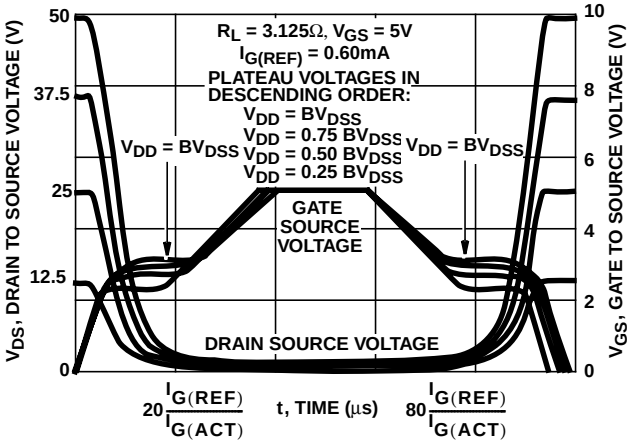



FIGURE 12. NORMALIZED SWITCHING WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuits and Waveforms

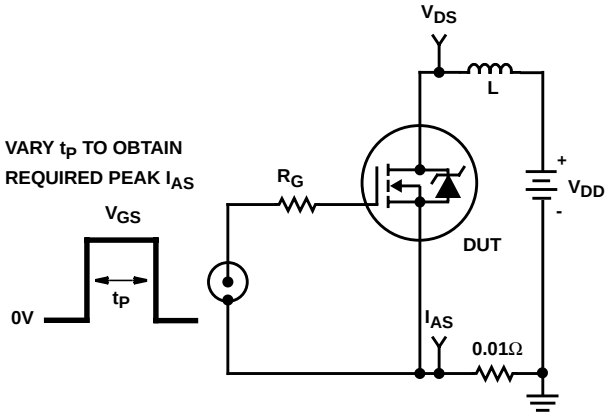



FIGURE 13. UNCLAMPED ENERGY TEST CIRCUIT

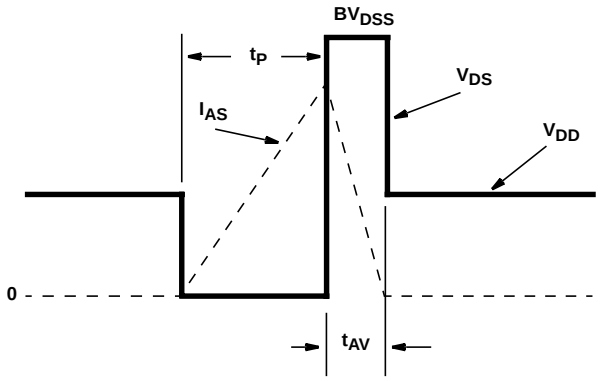



FIGURE 14. UNCLAMPED ENERGY WAVEFORMS

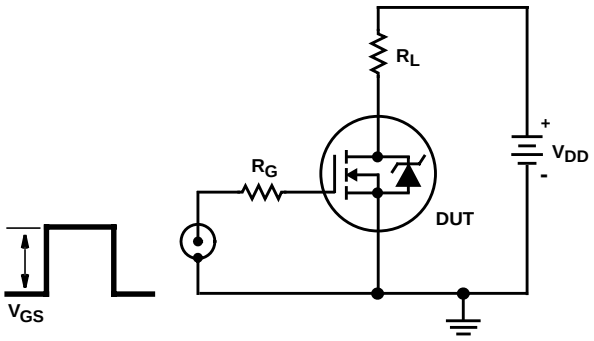



FIGURE 15. SWITCHING TIME TEST CIRCUIT

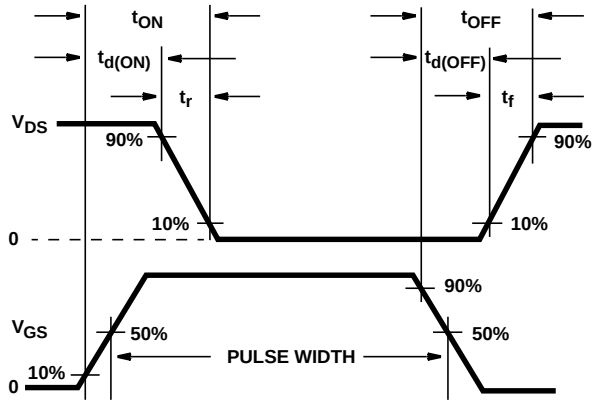



FIGURE 16. RESISTIVE SWITCHING WAVEFORMS

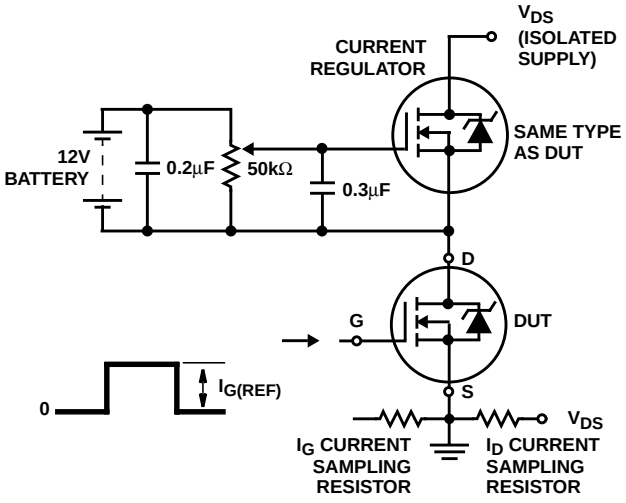



FIGURE 17. GATE CHARGE TEST CIRCUIT

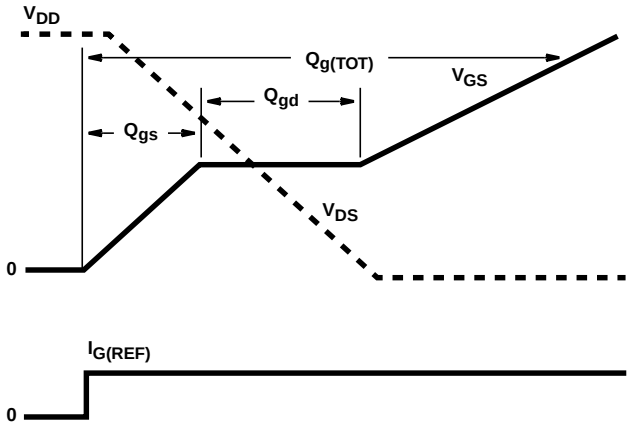



FIGURE 18. GATE CHARGE WAVEFORMS

## Spice Model (RFD16N05L)

```
.SUBCKT RFD16N05L  2  1  3;  rev 04/08/92
*Nominal Temperature = 25OC
.MODEL MOSMOD NMOS (VTO=2.054  KP=24.73  IS=1e-30  N=10  TOX=1  L=1u  W=1u)
Vto  21  6  0.448
Rsource  8  7  RDSMOD  0.614E-3
Rdrain  5  16  RDSMOD  27.38E-3
.MODEL RDSMOD RES (TC1=3.66E-3  TC2=1.46E-5)
.MODEL RVTOMOD RES (TC1=-1.81E3  TC2=1.41E-6)
Ebreak 11  7  17  18  70.9
.MODEL RBKMOD RES (TC1=1.01E-3  TC2=5.21E-8)
.MODEL DBKMOD D (RS=8.82E-2  TRS1=-2.01E-3  TRS2=7.32E-10)
.MODEL DBDMOD D (IS=1.34E-13  RS=1.21E-2  TRS1=1.64E-3  TRS2=2.59E-6  +CJO=1.13E-9  TT=4.14E-8)
Cin  6  8  1.21E-9
Ca  12  8  3.33E-9
.MODEL S1AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-4.25  VOFF=-2.25)
.MODEL S1BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-2.25  VOFF=-4.25)
.MODEL DPLCAPMOD D (CJO=5.22E-10  IS=1e-30  N=10)
Cb  15  14  3.11E-9
.MODEL S2AMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=-0.65  VOFF=4.35)
.MODEL S2BMOD VSWITCH (RON=1e-5  ROFF=0.1  VON=4.35  VOFF=-0.65)
Rgate  9  20  2.98
Lgate  1  9  1.38E-9
Ldrain  2  5  1.0E-12
Lsource  3  7  1.0E-9
Dbody  7  5  DBDMOD
Dbreak  5  11  DBKMOD
Dplcap  10  5  DPLCAPMOD
Eds  14  8  5  8  1
Egs  13  8  6  8  1
Esg  6  10  6  8  1
Evto  20  6  18  8  1
It  8  17  1
MOS1  16  6  8  8  MOSMOD  M=0.99
MOS2  16  21  8  8  MOSMOD  M=0.01
Rbreak  17  18  RBKMOD  1
Rin  6  8  1e9
Rvto  18  19  RVTOMOD  1
S1a  6  12  13  8  S1AMOD
S1b  13  12  13  8  S1BMOD
S2a  6  15  14  13  S2AMOD
S2b  13  15  14  13  S2BMOD
Vbat  8  19  DC  1
.ENDS

x
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