

AD5547-EP

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REVISION HISTORY

9/11—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

$V_{DD} = 2.7 \text{ V to } 5.5 \text{ V}$, $I_{OUT} = \text{virtual GND}$, $\text{GND} = 0 \text{ V}$, $V_{REF} = -10 \text{ V to } +10 \text{ V}$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE ¹						
Resolution	N	1 LSB = $V_{REF}/2^{16} = 153 \mu\text{V}$ at $V_{REF} = 10 \text{ V}$		16		Bits
Relative Accuracy	INL				±2	LSB
Differential Nonlinearity	DNL	Monotonic			±1	LSB
Output Leakage Current	I_{OUT}	Data = zero scale, $T_A = 25^\circ\text{C}$			10	nA
		Data = zero scale, $T_A = T_A \text{ maximum}$			20	nA
Full-Scale Gain Error	G_{FSE}	Data = full scale	±1		±5	mV
Bipolar Mode Gain Error	G_E	Data = full scale	±1		±5	mV
Bipolar Mode Zero-Scale Error	G_{ZSE}	Data = full scale	±1		±4	mV
Full-Scale Temperature Coefficient ²	TCV_{FS}		1			ppm/°C
REFERENCE INPUT						
V_{REF} Range	V_{REF}		−18		+18	V
REF Input Resistance	REF		4	5	6	kΩ
R1 and R2 Resistance	R1 and R2		4	5	6	kΩ
R1-to-R2 Mismatch	$\Delta(R1 \text{ to } R2)$			±0.5	±1.5	Ω
Feedback and Offset Resistance	R_{FB}, R_{OFS}		8	10	12	kΩ
Input Capacitance ²	C_{REF}			5		pF
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = full scale		2		mA
Output Capacitance ²	C_{OUT}	Code dependent		200		pF
LOGIC INPUT AND OUTPUT						
Logic Input Low Voltage	V_{IL}	$V_{DD} = 5 \text{ V}$			0.8	V
		$V_{DD} = 3 \text{ V}$			0.4	V
Logic Input High Voltage	V_{IH}	$V_{DD} = 5 \text{ V}$	2.4			V
		$V_{DD} = 3 \text{ V}$	2.1			V
Input Leakage Current	I_{IL}				10	μA
Input Capacitance ²	C_{IL}				10	pF
INTERFACE TIMING ^{2, 3}						
Data to $\overline{WR}$ Setup Time	t_{DS}	See Figure 3				
		$V_{DD} = 5 \text{ V}$	20			ns
		$V_{DD} = 3 \text{ V}$	35			ns
Data to $\overline{WR}$ Hold Time	t_{DH}	$V_{DD} = 5 \text{ V}$	0			ns
		$V_{DD} = 3 \text{ V}$	0			ns
$\overline{WR}$ Pulse Width	$t_{\overline{WR}}$	$V_{DD} = 5 \text{ V}$	20			ns
		$V_{DD} = 3 \text{ V}$	35			ns
LDAC Pulse Width	t_{LDAC}	$V_{DD} = 5 \text{ V}$	20			ns
		$V_{DD} = 3 \text{ V}$	35			ns
$\overline{RS}$ Pulse Width	t_{RS}	$V_{DD} = 5 \text{ V}$	20			ns
		$V_{DD} = 3 \text{ V}$	35			ns
$\overline{WR}$ to LDAC Delay Time	t_{LWD}	$V_{DD} = 5 \text{ V}$	0			ns
		$V_{DD} = 3 \text{ V}$	0			ns
SUPPLY CHARACTERISTICS						
Power Supply Range	$V_{DD \text{ RANGE}}$		2.7		5.5	V
Positive Supply Current	I_{DD}	Logic inputs = 0 V			10	μA
Power Dissipation	P_{DISS}	Logic inputs = 0 V			0.055	mW
Power Supply Sensitivity	P_{SS}	$\Delta V_{DD} = \pm 5\%$			0.003	%/%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
AC CHARACTERISTICS ⁴						
Output Voltage Settling Time	t_s	To $\pm 0.1\%$ of full scale, data cycles from zero scale to full scale to zero scale		0.5		μs
Reference Multiplying Bandwidth	BW	$V_{REF} = 100 \text{ mV rms}$, data = full scale		6.8		MHz
DAC Glitch Impulse	Q	$V_{REF} = 0 \text{ V}$, midscale – 1 to midscale		–3.5		nV-s
Multiplying Feedthrough Error	V_{OUT}/V_{REF}	$V_{REF} = 100 \text{ mV rms}$, $f = 10 \text{ kHz}$		–78		dB
Digital Feedthrough	Q_D	$\overline{WR} = 1$, LDAC toggles at 1 MHz		7		nV-s
Total Harmonic Distortion	THD	$V_{REF} = 5 \text{ V p-p}$, data = full scale, $f = 1 \text{ kHz}$		–104		dB
Output Noise Density	e_N	$f = 1 \text{ kHz}$, BW = 1 Hz		12		$\text{nV}/\sqrt{\text{Hz}}$
Analog Crosstalk	C_{AT}	Signal input at Channel A and measures the output at Channel B, $f = 1 \text{ kHz}$		–95		dB

¹ All static performance tests (except I_{OUT}) are performed in a closed-loop system using an external precision [OP97](#) I-to-V converter amplifier. The device R_{FB} terminal is tied to the amplifier output. The +IN pin of the [OP97](#) is grounded, and the I_{OUT} of the DAC is tied to the [OP97](#)'s –IN pin. Typical values represent average readings measured at 25°C .

² Guaranteed by design; not subject to production testing.

³ All input control signals are specified with $t_R = t_F = 2.5 \text{ ns}$ (10% to 90% of 3 V) and are timed from a voltage level of 1.5 V.

⁴ All ac characteristic tests are performed in a closed-loop system using an [AD8038](#) I-to-V converter amplifier except for THD where the [AD8065](#) was used.

Timing Diagram

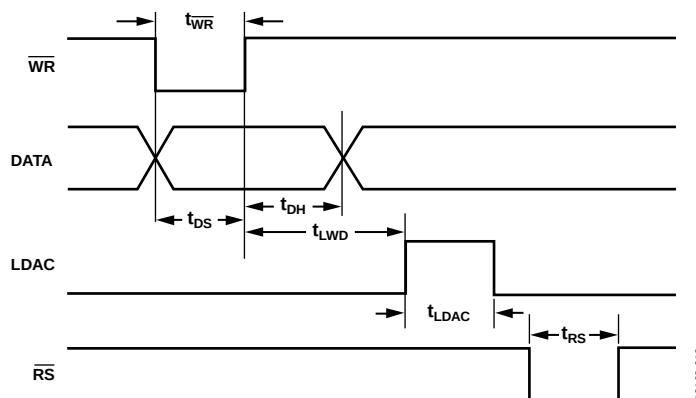


Figure 3. [AD5547-EP](#) Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V _{DD} to GND	–0.3 V to +8 V
R _{FB} , R _{OF} , R ₁ , R _{COM} , and V _{REF} to GND	–18 V to +18 V
Logic Inputs to GND	–0.3 V to +8 V
V(I _{OUT}) to GND	–0.3 V to V _{DD} + 0.3 V
Input Current to Any Pin except Supplies	±50 mA
Thermal Resistance (θ _{JA}) ¹	
Maximum Junction Temperature (T _{J MAX})	150°C
Operating Temperature Range	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature	
Vapor Phase, 60 sec	215°C
Infrared, 15 sec	220°C

¹ Package power dissipation = (T_{J MAX} – T_A)/θ_{JA}.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

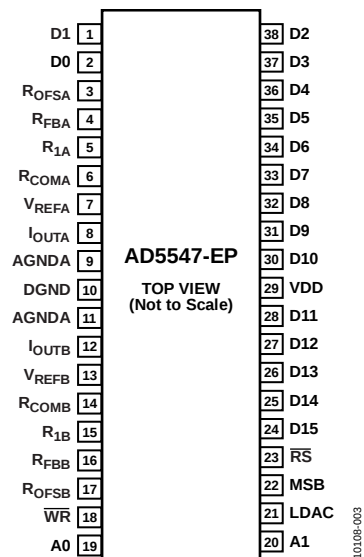


Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 24 to 28, 30 to 38	D0 to D15	Digital Input Data Bits D0 to D15. Signal level must be $\leq V_{DD} + 0.3$ V.
3	ROFSA	Bipolar Offset Resistor A. Accepts up to ± 18 V. In 2-quadrant mode, ROFSA ties to RFBA. In 4-quadrant mode, ROFSA ties to R1A and the external reference.
4	RFBA	Internal Matching Feedback Resistor A. Connects to the external op amp for I-to-V conversion.
5	R1A	4-Quadrant Resistor. In 2-quadrant mode, R1A shorts to the VREFA pin. In 4-quadrant mode, R1A ties to ROFSA. Do not connect when operating in unipolar mode.
6	RCOMA	Center Tap Point of the Two 4-Quadrant Resistors, R1A and R2A. In 4-quadrant mode, RCOMA ties to the inverting node of the reference amplifier. In 2-quadrant mode, RCOMA shorts to the associated VREFA pin. Do not connect if operating in unipolar mode.
7	VREFA	DAC A Reference Input in 2-Quadrant Mode, R2 Terminal in 4-Quadrant Mode. In 2-quadrant mode, VREFA is the reference input with constant input resistance vs. code. In 4-quadrant mode, VREFA is driven by the external reference amplifier.
8	IOUTA	DAC A Current Output. Connects to the inverting terminal of external precision I-to-V op amp for voltage output.
9	AGNDA	DAC A Analog Ground.
10	DGND	Digital Ground.
11	AGNDB	DAC B Analog Ground.
12	IOUTB	DAC B Current Output. Connects to inverting terminal of external precision I-to-V op amp for voltage output.
13	VREFB	DAC B Reference Input Pin. Establishes DAC full-scale voltage. Constant input resistance vs. code. If configured with an external op amp for 4-quadrant multiplying, VREFB becomes $-V_{REF}$.
14	RCOMB	Center Tap Point of the Two 4-Quadrant Resistors, R1B and R2B. In 4-quadrant mode, RCOMB ties to the inverting node of the reference amplifier. In 2-quadrant mode, RCOMB shorts to the VREFB pin. Do not connect if operating in unipolar mode.
15	R1B	4-Quadrant Resistor. In 2-quadrant mode, R1B shorts to the VREFB pin. In 4-quadrant mode, R1B ties to ROFSB. Do not connect if operating in unipolar mode.
16	RFBB	Internal Matching Feedback Resistor B. Connects to external op amp for I-to-V conversion.
17	ROFSB	Bipolar Offset Resistor B. Accepts up to ± 18 V. In 2-quadrant mode, ROFSB ties to RFBB. In 4-quadrant mode, ROFSB ties to R1B and an external reference.
18	WR	Write Control Digital Input In, Active Low. WR transfers shift register data to the DAC register on the rising edge. Signal level must be $\leq V_{DD} + 0.3$ V.

Pin No.	Mnemonic	Description
19	A0	Address Pin 0. Signal level must be $\leq V_{DD} + 0.3 \text{ V}$.
20	A1	Address Pin 1. Signal level must be $\leq V_{DD} + 0.3 \text{ V}$.
21	LDAC	Digital Input Load DAC Control. Signal level must be $\leq V_{DD} + 0.3 \text{ V}$.
22	MSB	Power-On Reset State. MSB = 0 corresponds to zero-scale reset; MSB = 1 corresponds to midscale reset. The signal level must be $\leq V_{DD} + 0.3 \text{ V}$.
23	$\overline{\text{RS}}$	Active low resets both input and DAC registers. Resets to zero-scale if MSB = 0 and resets to midscale if MSB = 1. Signal level must be $\leq V_{DD} + 0.3 \text{ V}$.
29	VDD	Positive Power Supply Input. The specified range of operation is 2.7 V to 5.5 V.

Table 4. Address Decoder Pins

A1	A0	Output Update
0	0	DAC A
0	1	None
1	0	DAC A and DAC B
1	1	DAC B

Table 5. Control Inputs

$\overline{\text{RS}}$	$\overline{\text{WR}}$	LDAC	Register Operation
0	X	X	Reset the output to 0 with MSB = 0; reset the output to midscale with MSB = 1.
1	0	0	Load the input register with data bits.
1	1	1	Load the DAC register with the contents of the input register.
1	0	1	The input and DAC registers are transparent.
1			When LDAC and $\overline{\text{WR}}$ are tied together and programmed as a pulse, the data bits are loaded into the input register on the falling edge of the pulse and are then loaded into the DAC register on the rising edge of the pulse.
1	1	0	No register operation.

TYPICAL PERFORMANCE CHARACTERISTICS

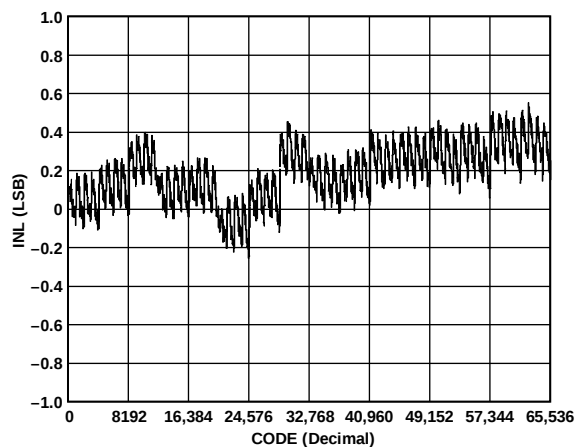


Figure 5. AD5547-EP Integral Nonlinearity Error

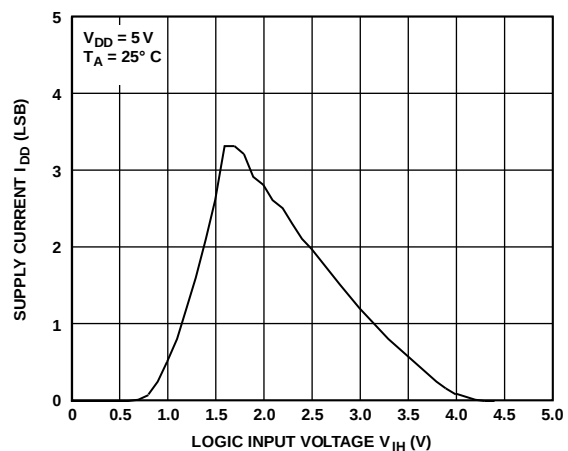


Figure 8. Supply Current vs. Logic Input Voltage

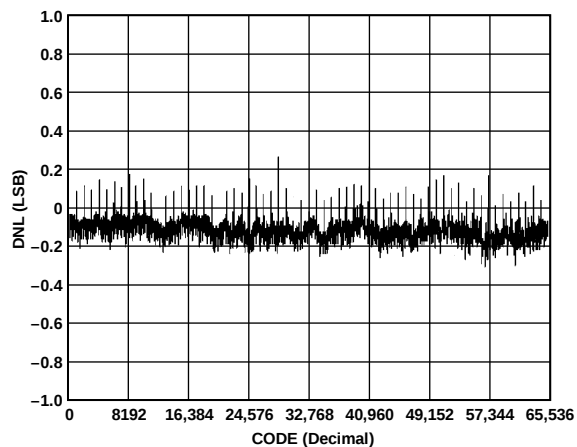


Figure 6. AD5547-EP Differential Nonlinearity Error

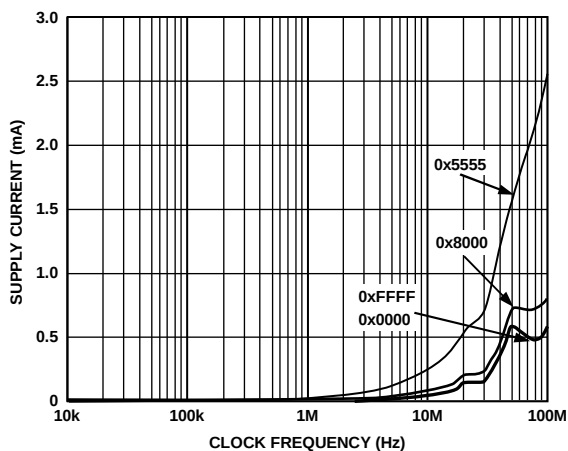


Figure 9. AD5547-EP Supply Current vs. Clock Frequency

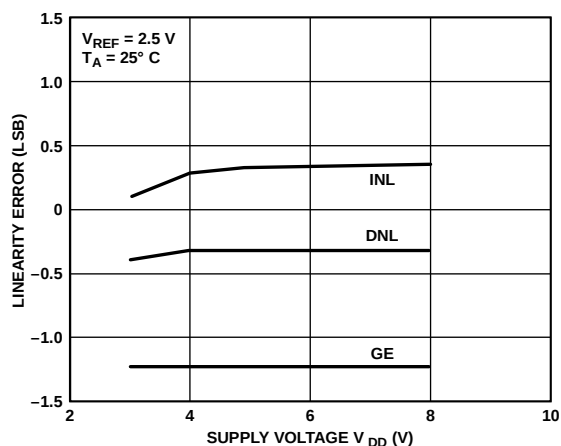
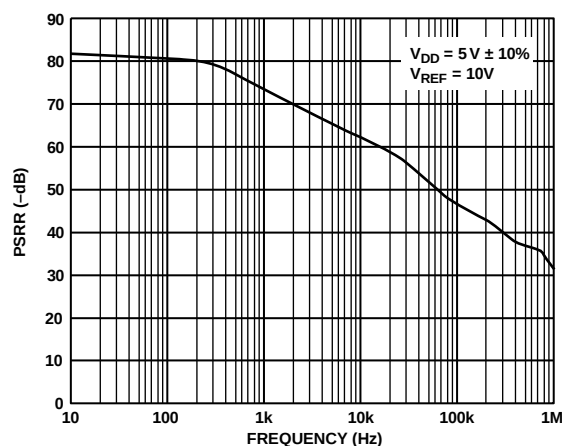
Figure 7. Linearity Error vs. Supply Voltage, V_{DD} 

Figure 10. Power Supply Rejection Ratio (PSRR) vs. Frequency

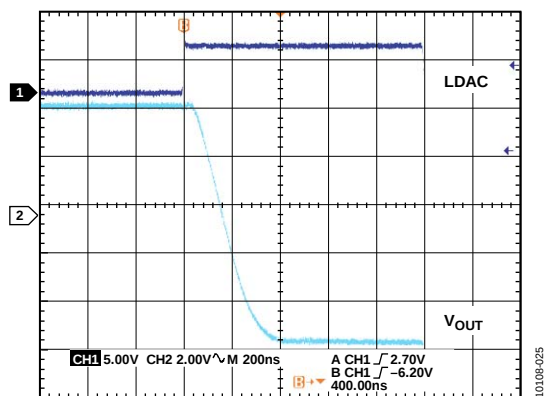


Figure 11. Settling Time from Full Scale to Zero Scale

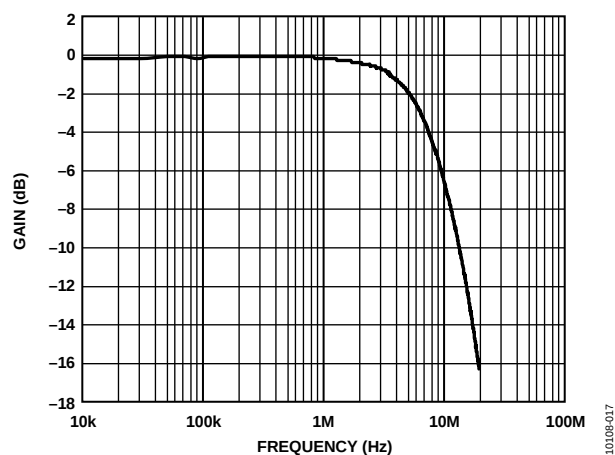


Figure 13. AD5547-EP Unipolar Reference Multiplying Bandwidth

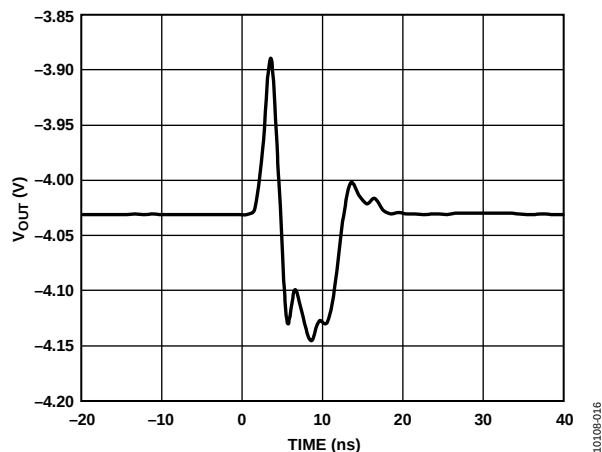


Figure 12. AD5547-EP Midscale Transition and Digital Feedthrough

OUTLINE DIMENSIONS

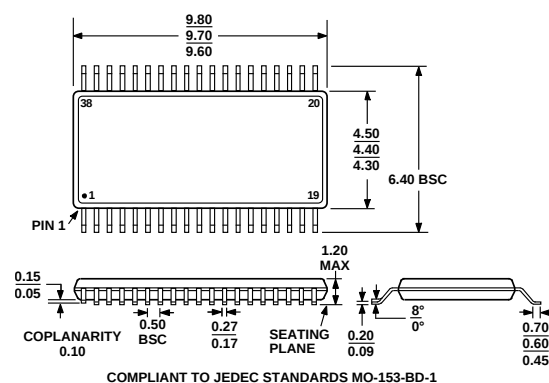


Figure 14. 38-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-38)

Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Resolution (Bits)	DNL (LSB)	INL (LSB)	Temperature Range	Package Description	Package Option
AD5547SRU-EP	16	±1	±2	−55°C to +125°C	38-Lead TSSOP	RU-38

¹ Z = RoHS Compliant Part.

NOTES

NOTES