GENERAL DESCRIPTION

FUNCTIONAL DESCRIPTION

XRK32308 is a 3.3V Zero Delay Buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom, and other high-performance applications.

The part has an on-chip PLL which locks to an input clock presented on the REF pin. The PLL feedback is required to be driven into the FB pin, and can be obtained from one of the outputs. The input-to-output skew is guaranteed to be less than 350 ps, and output-to-output skew is guaranteed to be less than 200 ps.

XRK32308 has two banks of four outputs each. These can be controlled by the Select inputs as shown in Table 2, “Select Input Decoding,” on page 2. If all output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the output for chip and system testing purposes.

Multiple XRK32308 devices can accept the same input clock and distribute it in a system. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

XRK32308 devices are available in five different configurations, as shown in Table 3, “Available XRK32308 Configurations,” on page 3.

The XRK32308–1 is the base part, where the output frequencies equal the reference if there is no counter in the feedback path.

The XRK32308–1H is the high-drive version of the –1. Rise and fall times on this device are faster.

The XRK32308–2 allows the user to obtain 1X, and 2X or X/2 depending on which Bank sources the FB signal.

The XRK32308–3 allows the user to obtain 4X and 2X frequencies or 1X and 2X.

The XRK32308–4 enables the user to obtain 2X clocks on all outputs.

The XRK32308–5H is a high-drive version with REF/2 on both banks.

FEATURES

- Zero input-output propagation delay, adjustable by capacitive load on FB input
- Multiple configurations, see “Available XRK32308 Configurations” table
- Multiple low-skew outputs
- Two banks of four outputs, three-stateable by two select inputs
- 10-MHz to 120-MHz operating range
- 75ps typical cycle-to-cycle jitter (15pF, 66MHz)
- Space-saving 16-pin 150-mil SOIC package or 16-pin TSSOP
- 3.3V operation
- Industrial and commercial temperature available

FIGURE 1. BLOCK DIAGRAM AND PIN CONFIGURATION OF THE XRK32308

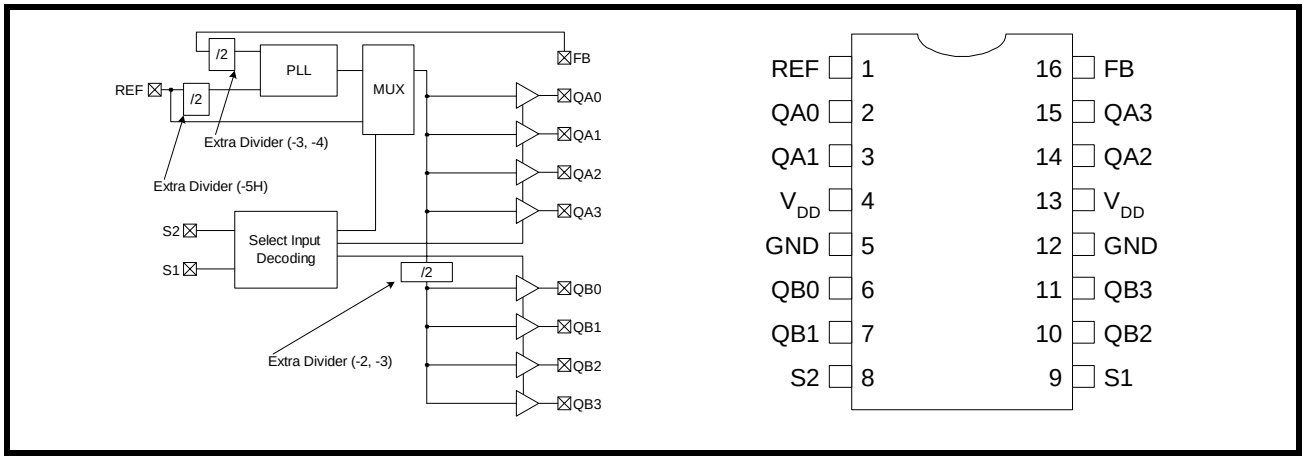


TABLE 1: PIN DESCRIPTION

PIN	SIGNAL	DESCRIPTION
1	REF[1]	Input reference frequency
2	QA0[2]	Clock output, Bank A
3	QA1[2]	Clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	QB0[2]	Clock output, Bank B
7	QB1[2]	Clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	QB2[2]	Clock output, Bank B
11	QB3[2]	Clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V supply
14	QA2[2]	Clock output, Bank A
15	QA3[2]	Clock output, Bank A
16	FB	PLL feedback input

TABLE 2: SELECT INPUT DECODING

S2	S1	QA0-QA3	QB0-QB3	OUTPUT SOURCE
0	0	Three-State	Three-State	PLL
0	1	Driven	Three-State	PLL
1	0	Driven[4]	Driven[4]	Reference
1	1	Driven	Driven	PLL

NOTES:

1. *Weak pull-down.*
2. *Weak pull-down on all outputs.*
3. *Weak pull-ups on these inputs.*
4. *Outputs inverted on XRK32308–2 and XRK32308–3 in bypass mode, S2 = 1 and S1 = 0.*

TABLE 3: AVAILABLE XRK32308 CONFIGURATIONS

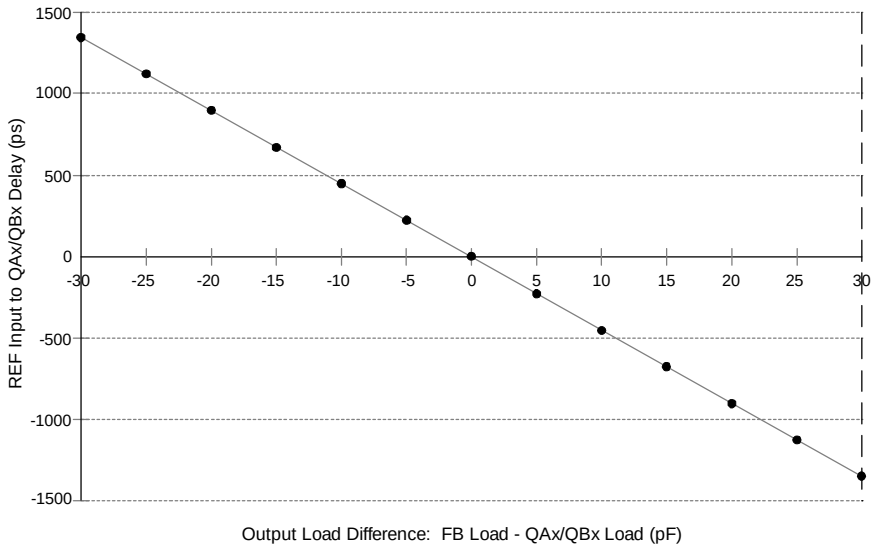
DEVICE	FEEDBACK FROM	BANK A FREQUENCY	BANK B FREQUENCY
XRK32308-1	Bank A or Bank B	Reference	Reference
XRK32308-1H	Bank A or Bank B	Reference	Reference
XRK32308-2	Bank A	Reference	Reference/2
XRK32308-2	Bank B	2 X Reference	Reference
XRK32308-3	Bank A	2 X Reference	Reference or $\overline{\text{Reference}}$[5]
XRK32308-3	Bank B	4 X Reference	2 X Reference
XRK32308-4	Bank A or Bank B	2 X Reference	2 X Reference
XRK32308-5H	Bank A or Bank B	Reference/2	Reference/2

NOTES:

5. Output phase is indeterminant (0° or 180° from input clock). If phase integrity is required, use the XRK32308–2.

ZERO DELAY AND SKEW CONTROL

FIGURE 2. REF INPUT TO QAX/QBX DELAY VS DIFFERENCE IN LOADING BETWEEN FB AND QAX/QBX PINS



Note: Target only, actual characterization curve may be slightly different.

To close the feedback loop of the XRK32308, the FB pin can be driven from any of the eight available output pins. The output driving the FB pin will be driving a total load of 7 pF plus any additional load that it drives. The relative loading of this output (with respect to the remaining outputs) can adjust the input-output delay. This is shown in the graph above.

For applications requiring zero input-output delay, all outputs including the one providing feedback should be equally loaded. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs.

For zero output-output skew, be sure to load outputs equally.

TABLE 4: ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage (Except Ref)	-0.5V to V_{DD} +0.5V
DC Input Voltage REF	-0.5 to 7V
Storage Temperature	-65°C to +150°C
Junction Temperature	150°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000V

TABLE 5: OPERATING CONDITIONS FOR XRK32308 COMMERCIAL TEMPERATURE DEVICES

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	0	70	°C
C_L	Load Capacitance, below 100MHz	-	30	pF
	Load Capacitance, from 100MHz to 120MHz	-	15	pF
C_{IN}	Input Capacitance[6]	-	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

NOTES:

6. Applies to both Ref Clock and FB.

TABLE 6: ELECTRICAL CHARACTERISTICS FOR XRK32308 COMMERCIAL TEMPERATURE DEVICES

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IL}	Input Low Voltage		-	0.8	V
V_{IH}	Input High Voltage		2.0	-	V
I_{IL}	Input Low Current	V_{IN}=0V	-	50.0	µA
I_{IH}	Input High Current	V_{IN}=V_{DD}	-	100.0	µA
V_{OL}	Output Low Voltage[7]	I_{OL}= 8mA (-1, -2, -3, -4) I_{OL}= 12mA (-1H, -5H)	-	0.4	V
V_{OH}	Output High Voltage[7]	I_{OH}= -8mA (-1, -2, -3, -4) I_{OH}= -12mA (-1H, -5H)	2.4	-	V

TABLE 6: ELECTRICAL CHARACTERISTICS FOR XRK32308 COMMERCIAL TEMPERATURE DEVICES

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
I_{DD}	Supply Current	Unloaded outputs, 100-MHz REF, Select inputs at V_{DD} or GND	-	45.0	mA
			-	70 (-1H, -5H)	mA
		Unloaded outputs, 66-MHz REF (-1, -2, -3, -4)	-	32.0	mA
		Unloaded outputs, 33-MHz REF (-1, -2, -3, -4)	-	18.0	mA

NOTES:

7. Parameter is guaranteed by design and characterization. Not 100% tested in production.

TABLE 7: SWITCHING CHARACTERISTICS FOR XRK32308 COMMERCIAL TEMPERATURE DEVICES[8]

PARAMETER	NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Output Frequency	30-pF load, All devices	10	-	100	MHz
		20-pF load, -1H, -5H devices[9]	10	-	120	MHz
		15-pF load, -1, -2, -3, -4 devices	10	-	120	MHz
DC	Duty Cycle[7] = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -5H)	Measured at 1.4V, F_{OUT}=66.66MHz 30-pF load	40.0	50.0	60.0	%
		Measured at 1.4V, F_{OUT}<50.0MHz 15-pF load	45.0	50.0	55.0	%
t_3	Rise Time[7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V, 30-pF load	-	-	2.20	ns
		Measured between 0.8V and 2.0V, 15-pF load	-	-	1.50	ns
	Rise Time[7] (-1H, -5H)	Measured between 0.8V and 2.0V, 30-pF load	-	-	1.50	ns
t_4	Fall Time[7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V, 30-pF load	-	-	2.20	ns
		Measured between 0.8V and 2.0V, 15-pF load	-	-	1.50	ns
	Fall Time[7] (-1H, -5H)	Measured between 0.8V and 2.0V, 30-pF load	-	-	1.25	ns

TABLE 7: SWITCHING CHARACTERISTICS FOR XRK32308 COMMERCIAL TEMPERATURE DEVICES[8]

PARAMETER	NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_5	Output to Output Skew on same Bank (-1, -2, -3, -4)[7]	All outputs equally loaded	-	-	200	ps
	Output to Output Skew (-1H, -5H)[7]	All outputs equally loaded	-	-	200	ps
	Output Bank A to Output Bank B Skew (-1, -4, -5H)	All outputs equally loaded	-	-	200	ps
	Output Bank A to Output Bank B Skew (-2, -3)	All outputs equally loaded	-	-	400	ps
t_6	Delay, REF Rising Edge to FB Rising Edge[7]	Measured at $V_{DD}/2$	-	0	±250	ps
t_7	Device to Device Skew[7]	Measured at $V_{DD}/2$ on the FB pins of devices	-	0	700	ps
t_8	Output Slew Rate[7]	Measured between 0.8V and 2.0V on -1H, -5H device using Test Circuit #2	1	-		V/ns
t_J	Cycle to Cycle Jitter[7] (-1, -1H, -4, -5H)	Measured at 66.67MHz, loaded outputs, 15-pF load	-	75	200	ps
		Measured at 66.67MHz, loaded outputs, 30-pF load	-	-	200	ps
		Measured at 120MHz, loaded outputs, 15-pF load	-	-	100	ps
	Cycle to Cycle Jitter[7] (-2, -3)	Measured at 66.67MHz, loaded outputs, 30-pF load	-	-	400	ps
		Measured at 66.67MHz, loaded outputs, 15-pF load	-	-	400	ps
t_{LOCK}	PLL Lock Time[7]	Stable power suppy, valid clock presented on REF and FB pins	-	-	1.0	ms

NOTES:

8. All parameters are specified with loaded outputs.

9. XRK32308 has maximum input frequency of 120MHz and maximum output of 66.67MHz.

TABLE 8: OPERATING CONDITIONS FOR XRK32308 INDUSTRIAL TEMPERATURE DEVICES

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	-40	85	°C
C_L	Load Capacitance, below 100MHz	-	30	pF
	Load Capacitance, from 100MHz to 120MHz	-	15	pF
C_{IN}	Input Capacitance[6]	-	7	pF
t_{PU}	Power-up time for all V_{DD}s to reach minimum specified voltage (power ramps must be monotonic)	0.05	50	ms

TABLE 9: ELECTRICAL CHARACTERISTICS FOR XRK32308 INDUSTRIAL TEMPERATURE DEVICES

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
V_{IL}	Input Low Voltage		-	0.8	V
V_{IH}	Input High Voltage		2.0	-	V
I_{IL}	Input Low Current	V_{IN}=0V	-	50.0	µA
I_{IH}	Input High Current	V_{IN}=V_{DD}	-	100.0	µA
V_{OL}	Output Low Voltage[7]	I_{OL}= 8mA (-1, -2, -3, -4) I_{OL}= 12mA (-1H, -5H)	-	0.4	V
V_{OH}	Output High Voltage[7]	I_{OH}= -8mA (-1, -2, -3, -4) I_{OH}= -12mA (-1H, -5H)	2.4	-	V
I_{DD}	Supply Current	Unloaded outputs, 100 MHz REF, Select inputs at V_{DD} or GND	-	45.0	mA
			-	70 (-1H, -5H)	mA
		Unloaded outputs, 66-MHz REF (-1, -2, -3, -4)	-	35.0	mA
		Unloaded outputs, 33-MHz REF (-1, -2, -3, -4)	-	20.0	mA

TABLE 10: SWITCHING CHARACTERISTICS FOR XRK32308 INDUSTRIAL TEMPERATURE DEVICES[8]

PARAMETER	NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Output Frequency	30-pF load, All devices	10	-	100	MHz
		20-pF load, -1H, -5H devices[9]	10	-	120	MHz
		15-pF load, 01, 02, 03, 04 devices	10	-	120	MHz
DC	Duty Cycle[7] = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -5H)	Measured at 1.4V, F_{OUT}=66.66MHz 30-pF load	40.0	50.0	60.0	%
		Measured at 1.4V, F_{OUT}<50.0MHz 15-pF load	45.0	50.0	55.0	%
t_3	Rise Time[7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V, 30-pF load	-	-	2.5	ns
		Measured between 0.8V and 2.0V, 15-pF load	-	-	1.50	ns
	Rise Time[7] (-1H, -5H)	Measured between 0.8V and 2.0V, 30-pF load	-	-	1.50	ns
t_4	Fall Time[7] (-1, -2, -3, -4)	Measured between 0.8V and 2.0V, 30-pF load	-	-	2.50	ns
		Measured between 0.8V and 2.0V, 15-pF load	-	-	1.50	ns
	Fall Time[7] (-1H, -5H)	Measured between 0.8V and 2.0V, 30-pF load	-	-	1.25	ns
t_5	Output to Output Skew on same Bank (-1, -2, -3, -4)[7]	All outputs equally loaded	-	-	200	ps
	Output to Output Skew (-1H, -5H)	All outputs equally loaded	-	-	200	ps
	Output Bank A to Output Bank B Skew (-1, -4, -5H)	All outputs equally loaded	-	-	200	ps
	Output Bank A to Output Bank B Skew (-2, -3)	All outputs equally loaded	-	-	400	ps
t_6	Delay, REF Rising Edge to FB Rising Edge[7]	Measured at $V_{DD}/2$	-	0	±250	ps
t_7	Device to Device Skew[7]	Measured at $V_{DD}/2$ on the FB pins of devices	-	0	700	ps
t_8	Output Slew Rate[7]	Measured between 0.8V and 2.0V on -1H, -5H device using Test Circuit #2	1	-		V/ns

TABLE 10: SWITCHING CHARACTERISTICS FOR XRK32308 INDUSTRIAL TEMPERATURE DEVICES[8]

PARAMETER	NAME	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_J	Cycle to Cycle Jitter[7] (-1, -1H, -4, -5H)	Measured at 66.67MHz, loaded outputs, 15-pF load	-	75	200	ps
		Measured at 66.67MHz, loaded outputs, 30-pF load	-	-	200	ps
		Measured at 120MHz, loaded outputs, 15-pF load	-	-	100	ps
	Cycle to Cycle Jitter[7] (-2, -3)	Measured at 66.67MHz, loaded outputs, 30-pF load	-	-	400	ps
		Measured at 66.67MHz, loaded outputs, 15 pF load	-	-	400	ps
t_{LOCK}	PLL Lock Time[7]	Stable power suppy, valid clocks presented on REF and FB pins	-	-	1.0	ms

FIGURE 3. SWITCHING WAVEFORMS

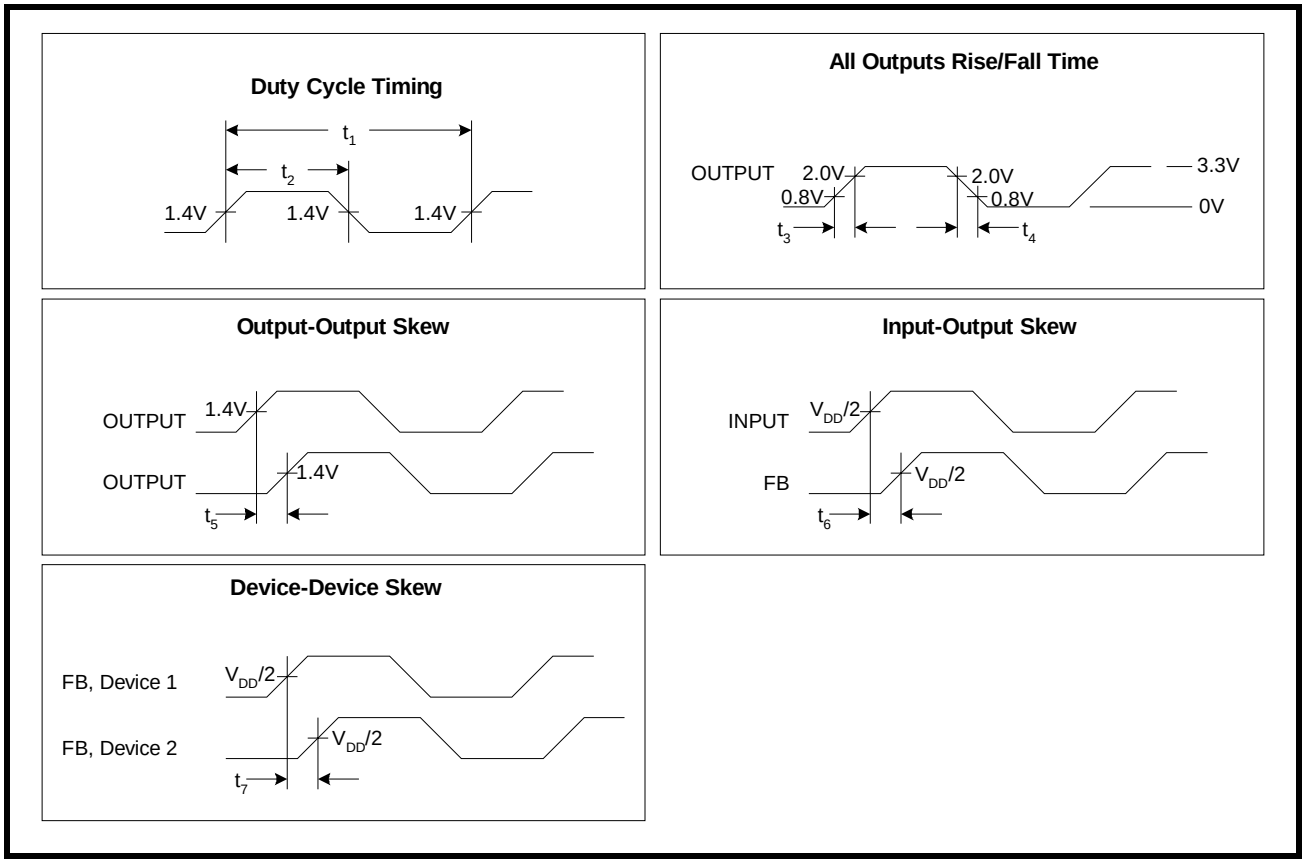
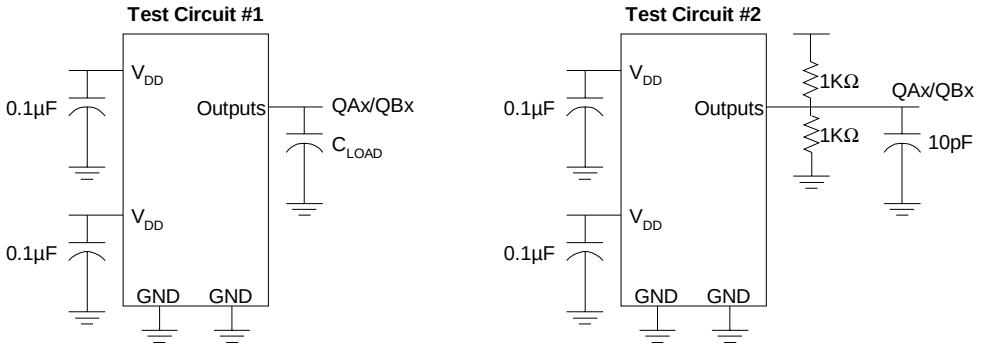


FIGURE 4. TEST CIRCUIT



Test Circuit for all parameters except t_8.

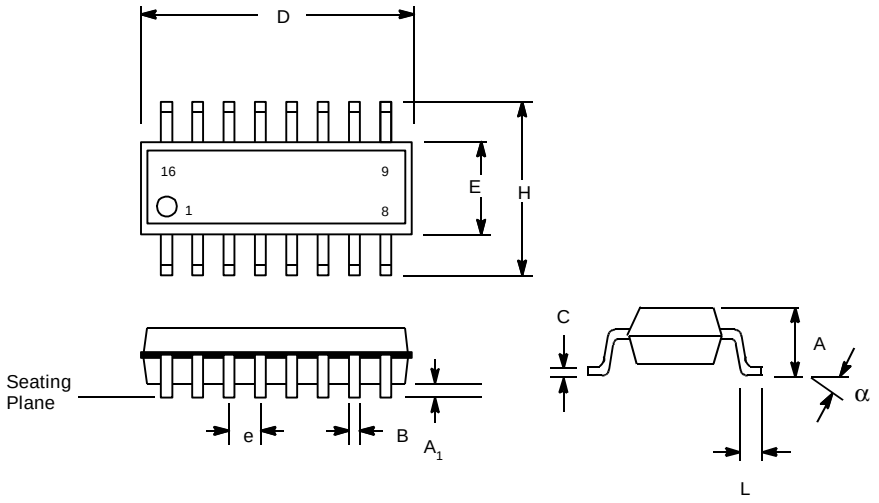
Test Circuit for t_8. Output slew rate on -1H, -5 device.

TABLE 11: ORDERING INFORMATION

PART ORDERING NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRK32308CD-1	16 Pin SOIC	0° to +70°
XRK32308CDTR-1	16 Pin SOIC	0° to +70°
XRK32308ID-1	16 Pin SOIC	-40° to +85°
XRK32308IDTR-1	16 Pin SOIC	-40° to +85°
XRK32308CD-1H	16 Pin SOIC	0° to +70°
XRK32308CDTR-1H	16 Pin SOIC	0° to +70°
XRK32308ID-1H	16 Pin SOIC	-40° to +85°
XRK32308IDTR-1H	16 Pin SOIC	-40° to +85°
XRK32308CG-1H	16 Pin TSSOP	0° to +70°
XRK32308CGTR-1H	16 Pin TSSOP	0° to +70°
XRK32308IG-1H	16 Pin TSSOP	-40° to +85°
XRK32308IGTR-1H	16 Pin TSSOP	-40° to +85°
XRK32308CD-2	16 Pin SOIC	0° to +70°
XRK32308CDTR-2	16 Pin SOIC	0° to +70°
XRK32308ID-2	16 Pin SOIC	-40° to +85°
XRK32308IDTR-2	16 Pin SOIC	-40° to +85°
XRK32308CD-3	16 Pin SOIC	0° to +70°
XRK32308CDTR-3	16 Pin SOIC	0° to +70°
XRK32308ID-3	16 Pin SOIC	-40° to +85°
XRK32308IDTR-3	16 Pin SOIC	-40° to +85°
XRK32308CD-4	16 Pin SOIC	0° to +70°
XRK32308CDTR-4	16 Pin SOIC	0° to +70°
XRK32308ID-4	16 Pin SOIC	-40° to +85°
XRK32308IDTR-4	16 Pin SOIC	-40° to +85°
XRK32308CD-5H	16 Pin SOIC	0° to +70°
XRK32308CDTR-5H	16 Pin SOIC	0° to +70°

PACKAGE DRAWINGS AND DIMENSIONS

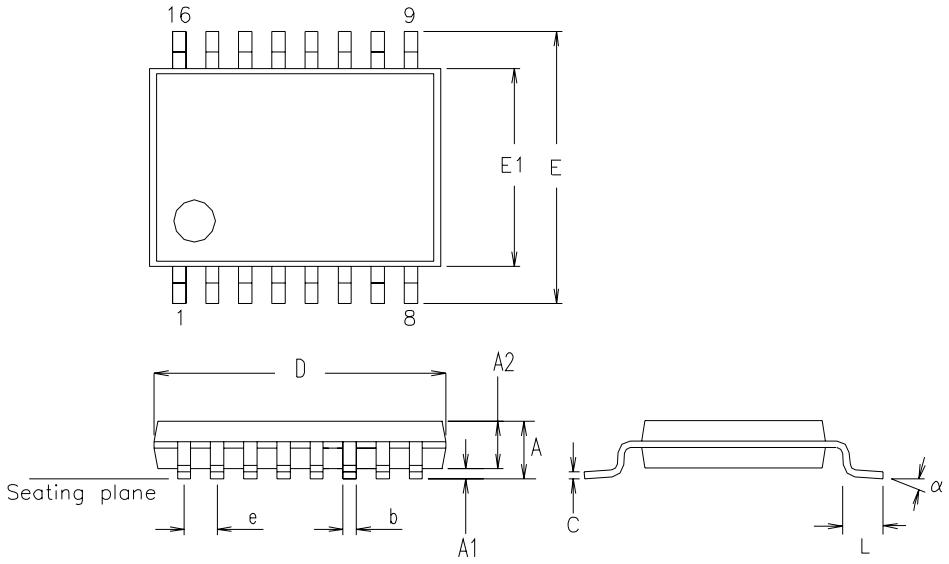
16 LEAD SMALL OUTLINE
(150 MIL JEDEC SOIC)
rev. 1.00



Note: The control dimension is the millimeter column

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A_1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.386	0.394	9.80	10.00
E	0.150	0.157	3.80	4.00
e	0.050 BSC		1.27 BSC	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
α	0°	8°	0°	8°

16 LEAD TSSOP THIN SHRINK SMALL OUTLINE
(4.4mm TSSOP)
Rev. 1.0



	INCHES		MILLIMETERS	
SYMBOL	**MIN**	**MAX**	**MIN**	**MAX**
A	0.031	0.043	0.80	1.10
A1	0.002	0.006	0.05	0.15
A2	0.031	0.037	0.80	0.95
B	0.007	0.012	0.19	0.30
C	0.004	0.008	0.09	0.20
D	0.193	0.201	4.90	5.10
E	0.248	0.260	6.30	6.60
E1	0.169	0.177	4.30	4.50
e	0.0256 BSC		0.65 BSC	
L	0.018	0.030	0.45	0.75
α	0°	8°	0°	8°

REVISIONS

REV. #	DATE	DESCRIPTION OF CHANGES
P1.0.0	04/05/06	Initial release.
P1.0.1	04/21/06	Ordering information edit: Added "H" to last two product numbers.
P1.0.2	05/12/06	Operating range changed to 10MHz to 120MHz - edit all references of this.

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Datasheet May 2006.