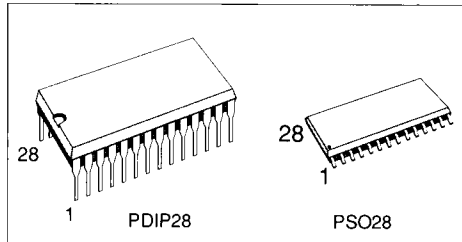
SGS-THOMSON MICROELECTRONICS

MK48256
MK48256L

32K x 8 CMOS STATIC RAM

PRELIMINARY DATA

- BYTEWYDE™ 32K X 8 CMOS SRAM
- EQUAL CYCLE/ACCESS TIMES, 100, 120NS MAX.
- LOW V_{CC} DATA RETENTION, 2 VOLTS
- THREE-STATE OUTPUT



(Ordering information at the end of the data-sheet)

DESCRIPTION

The MK48256 is a 256K (262,144-bit) CMOS SRAM, organized as 32,768 words x 8 bits. It is fabricated using SGS-THOMSON's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single +5V ± 10% supply, and all inputs and outputs are TTL compatible.

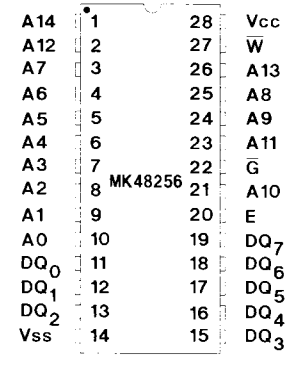
OPERATIONAL MODES

The MK48256 has a Chip Enable power down feature wich sustains an automatic standby mode whenever Chip Enable ($\overline{E}$) goes inactive high. An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$ and $\overline{E}$, as summarized in the truth table.

PIN NAMES

A0-A14	Address Inputs
DQ0-DQ7	Data I/O_{0-7}
$\overline{E}$	Chip Enable
$\overline{G}$	($\overline{OE}$) Output Enable
$\overline{W}$	Write/Read Enable
Vcc	+ 5V
Vss	GROUND

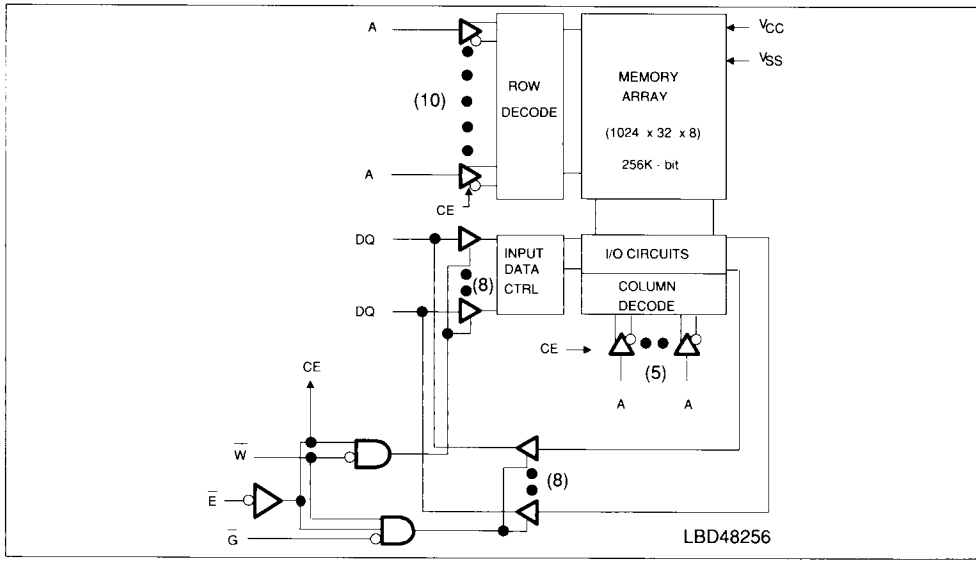
Pin Connection



MK48256 TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	MODE	DQ	POWER
H	X	X	Deselect	Hi-Z	Standby
L	H	H	Read	Hi-Z	Active
L	H	L	Read	D_{OUT}	Active
L	L	X	write	D_{IN}	Active

Figure 1 : MK48256 Block Diagram



READ MODE

The MK48256 is in the Read mode whenever Write Enable ($\overline{W}$) is high with Output Enable ($\overline{G}$) low, and Chip Enable ($\overline{E}$) is active low. This provides access to data from eight of 262,144 locations in the static memory array, specified by the 15 address inputs. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is low, and $\overline{E}$ is low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

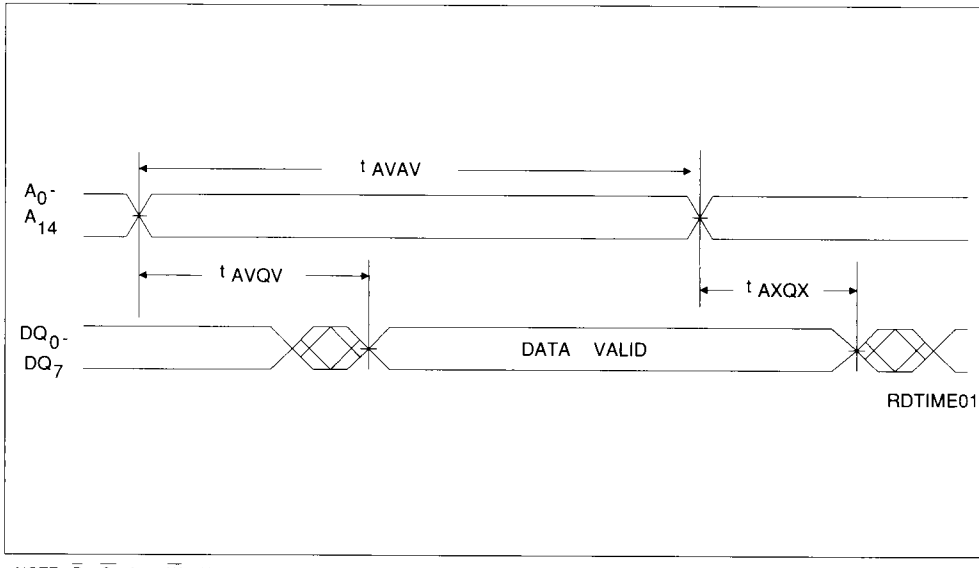
AC ELECTRICAL CHARACTERISTICS (READ CYCLE)

($0°C \leq T_A \leq +70°C$, $V_{CC} = 5.V \pm 10\%$)

SYMBOL	PARAMETER	MK48256-100		MK48256-120		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{AVAV}	Read Cycle Time	100		120		ns	
t_{AVQV}	Address Access Time		100		120		4
t_{ELQV}	Chip Enable Access Time		100		120		4
t_{GLQV}	Output Enable Access Time		50		60		4
t_{ELQX}	Chip Enable to Q Low-Z	10		10			5
t_{GLQX}	Output Enable to Q Low-Z	5		5			5
t_{EHQZ}	Chip Disable ($\overline{E}$) High to Q High-Z	0	35	0	35		5
t_{GHQX}	Output Disable ($\overline{G}$) High to Q High-Z	0	35	0	35		5
t_{AXQX}	Output Hold from Address Change	10		10			4

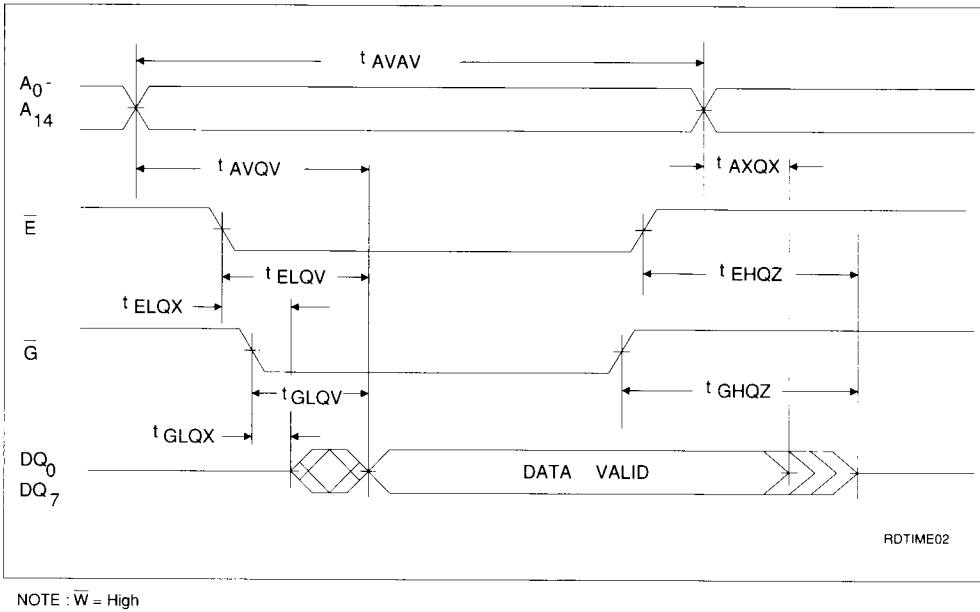
NOTES : 4. Measured with load as shown in Figure 8A.
5. Measured with load as shown in Figure 8B.

Figure 2 : Read Timing N°.1 (Address Access)



NOTE : $\overline{E}$ = $\overline{G}$ = Low, $\overline{W}$ = High

Figure 3 : Read Timing N°.2



NOTE : $\overline{W}$ = High

WRITE MODE

The MK48256 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are low. Either Chip Enable or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Enable being low with $\overline{W}$ low. Therefore, address setup times are referenced to Write Enable and Chip Enable as t_{AVWL}, and t_{AVEL} respectively, and is determined by whichever edge occurs latter. The Write cycle can be terminated by the earliest rising edge of $\overline{W}$ or Chip Enable ($\overline{E}$).

If the Output is enabled ($\overline{E}$ = low, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E}$, whichever occurs first, and remain valid t_{WHDX}.

AC ELECTRICAL CHARACTERISTICS (WRITE CYCLE)

(0°C ≤ T_A ≤ 70°C, V_{CC}= 5.0 ±10%)

SYMBOL	PARAMETER	MK48256-100		MM48256-120		UNIT	NOTE
		MIN	MAX	MIN	MAX		
t_{AVAV}	Write Cycle Time	100		120		ns	
t_{AVWL}	Address Set-up Time to $\overline{W}$ Low	0		0			
t_{AVEL}	Address Set-up Time to $\overline{E}$ Low	0		0			
t_{AVWH}	address valid to $\overline{W}$ HiGh	80		85			
t_{WLWH}	Write Pulse Width	60		65			
t_{WHAX}	Address Hold After End Of Write	5		5			
t_{ELEH}	Chip Enable Active To End Of Write	80		85			
t_{EHAX}	Address Hold Time From Chip Enable	5		5			
t_{DVWH}	Data Valid To End Of Write	40		45			
t_{WHDX}	Data Hold Time	0		0			
t_{WHQX}	$\overline{W}$ High to Q Active	5		5			5
t_{WLQZ}	$\overline{W}$ Low to Q High-Z	0	35	0	40		5

NOTE : 5. Measured with load as shown in Figure 8B.

Figure 4 : Write Control Cycle Timing

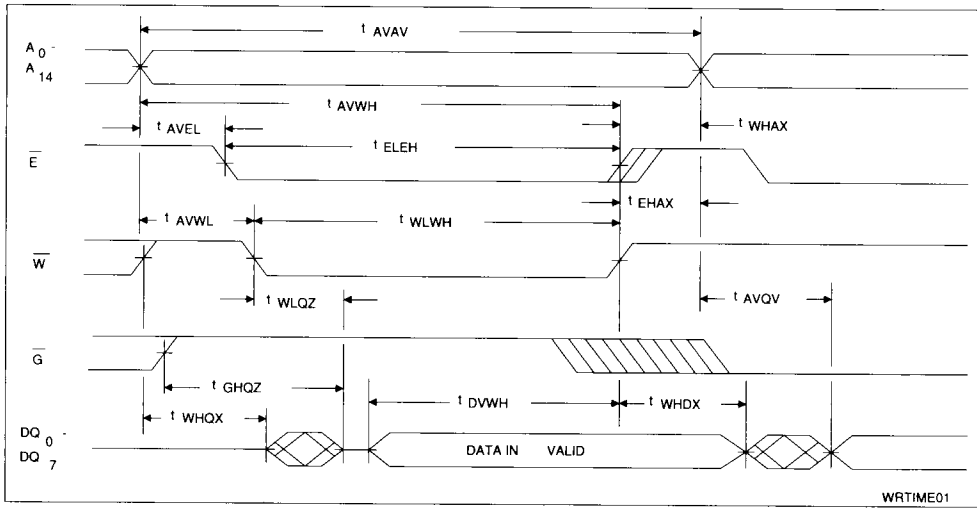
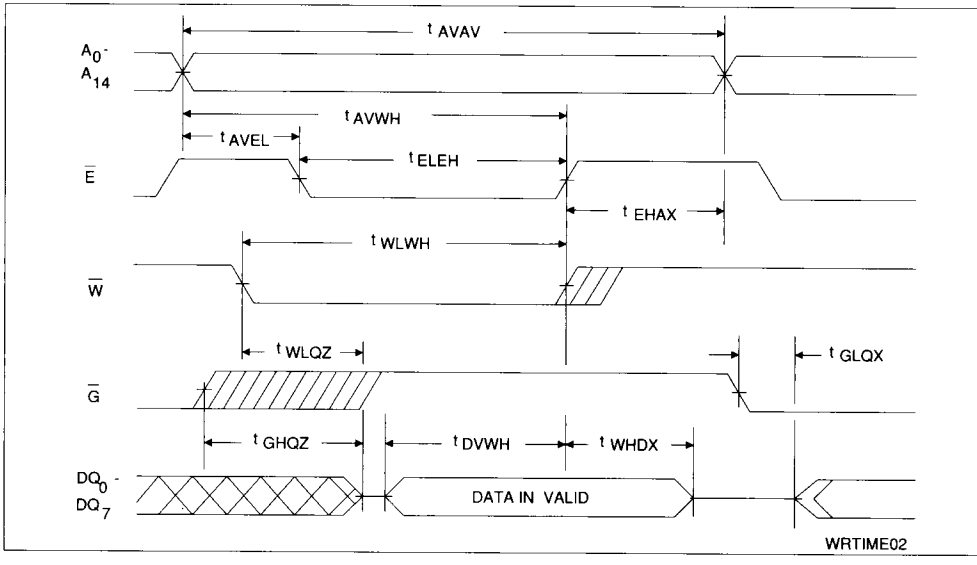


Figure 5 : Chip Enable Control Write Cycle Timing



STANDBY MODE CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C, Vcc = 5.0V ± 10%)

SYMBOL	PARAMETER	MK48256-100		MK48256-120		UNIT
		MAX	MIN	MAX	MIN	
t_{PU} †	Chip Enable to Power-Up	0		0		ns
t_{PD} †	Chip Enable to Power-Down		100		120	ns

† Parameters are guaranteed but not tested.

Figure 6 : Standby Mode Timing

LOW V_{CC} DATA RETENTION CHARACTERISTICS

(0°C ≤ T_A ≤ +70°C, Vcc = 5.0 ± 10%)

SYMBOL	PARAMETER		MAX	MAX	UNIT	NOTE
V_{DR}	V_{CC} Data Retention Mode		2.0		V	9
$I_{CC}DR^{(1)}$	Data Retention Pwr.supply Current Test Condition : Vcc = 3.0	MK48256		500	µA	9
		MK48256L		50	µA	9
t_{CDR} †	Chip Deselect to Data Retention Mode		0		nS	9
t_R †	Operation Recovery Time		t_{AVAV} (2)		nS	9

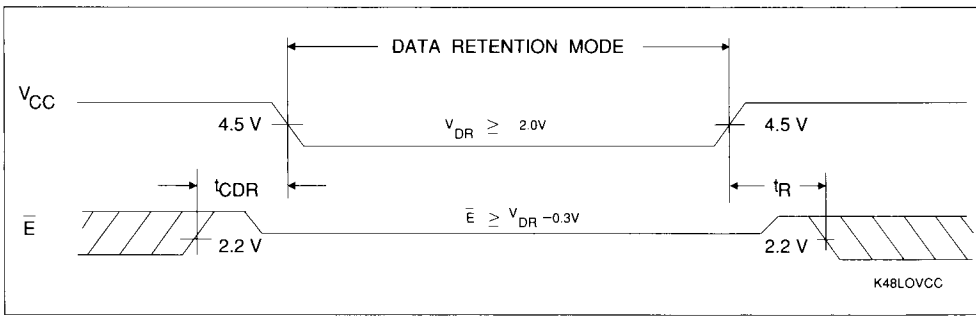
NOTE : 9. $\overline{E}$ ≥ Vcc - 0.3v, all other Inputs = don't care ; f = 0

† Parameters are guaranteed but not tested.

(1) For $I_{CC}DR$ between Vcc (MIN.) and Vcc (MAX.) refer to I_{SB1}.

(2) t_{AVAV} = Read Cycle Time.

Figure 7 : Low Vcc Data Retention



ABSOLUTE MAXIMUM RATINGS *

SYMBOL	PARAMETER	VALUE	UNIT
V_I	Voltage On Any Pin Relative to Ground	-0.5 to +7.0	V
T_A	Ambient Operating Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-65 to 150	°C
P_D	Power Dissipation	1	W
I_O	Output Current †	50	mA

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

† Output current absolute maximum rating is specified for one output at a time, not to exceed a duration of 1 second.

RECOMMENDED DC OPERATING CONDITIONS

($0°C \leq T_A \leq +70°C$)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	NOTE
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	1
V_{SS}	Ground	0	0	0	V	1
V_{IH}	Logic "1" Voltage All Inputs	2.2		Vcc + 0.3V	V	1
V_{IL}	Logic "0" Voltage All Inputs	-0.3		0.8	V	1

DC ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq +70°C$)

SYMBOL	PARAMETER		MIN	MAX	UNIT	NOTE
I_{CC1}	Average Vcc Power Supply Current			70	mA	6
I_{SB}	TTL Standby Current ($\overline{E}$= V_{IH})			3	mA	7
I_{SB1}	CMOS Standby Current ($\overline{E}$= Vcc -0.2v)	MK48256		1	mA	8
		MK48256L		100	µA	8
I_{LI}	Input Leakage Current (Any Input)		-1	+1	µA	2
I_{LO}	Ouput Leakage Current		-2	+2	µA	2
V_{OH}	Output Logic "1" Voltage (I_{OUT} =-4.0 mA)		2.4		V	1
V_{OL}	Output Logic "0" Voltage (I_{OUT} = +8.0 mA)			0.4	V	1

NOTES : 1. All voltages references to Ground.

2. Measured with $Vss \leq V \leq Vcc$ and outputs deselected.

6. Icc1 measured with outputs open, Vcc max ; f = min.duty cycle100%.

7. $\overline{E}$ = V_{IH}, all other inputs = don't care ; f = O

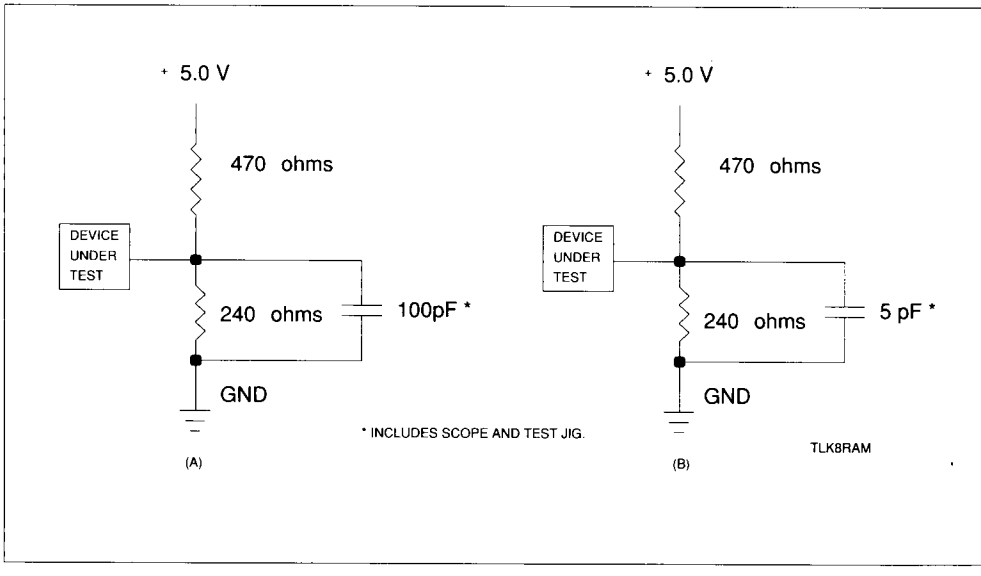
8. Vcc (max) $\geq \overline{E} \geq$ Vcc - 0.3v, all other inputs = don't care ; f = 0.

AC TEST CONDITIONS

Input Levels	GND to 3.0 V
Transition Time	1.5 ns
Input and Output Signal Timing Reference Level	1.5 Volts
Ambient Temperature	0°C to 70°C
V_{CC}	5.0V ± 10%

Note : ± 5% V-bump test is employed for t_{AVQV} only.

Figure 8 : Output Load Diagram



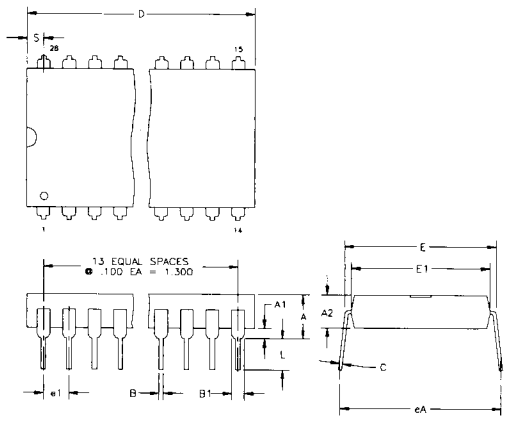
CAPACITANCE (TA = 25°C, f = 1.0 MHz)

Symbol	Parameter	Max	Unit	Note
C_I	Capacitance on all pins (except DQ)	8.0	pF	10
C_{DQ}	Capacitance on DQ pins	10.0	pF	3,10

NOTES : 3. Output buffer is deselected.
10. Capacitances are sampled and not 100 % tested.

MECHANICAL INFORMATION

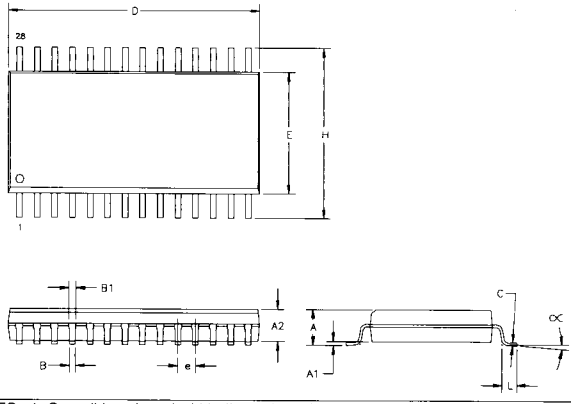
Figure 9 : Plastic PDIP28



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A (2)	3.94		5.08	.155		.200
a1 (2)	.38		1.78	.015		.070
A2	3.56		4.06	.140		.160
B (3)	.38		.53	.015		.021
B1	1.14		1.78	.045		.070
C (3)	.20		.30	.008		.012
D (1)	36.32		37.34	1.430		1.470
E	14.99		16.26	.590		.640
E1	13.46		13.97	.530		.550
e 1	2.54 NOM.			.100		
e A	15.24		17.78	.600		.700
L	3.05		3.81	.120		.150

NOTES : 1. Overall length includes .010 IN. Flash on either end of the package.
2. Package stand off to be measured per jedec requirements.
3. The maximum limit shall be increased by .003 IN. When solder lead finish is specified.

Figure 10 : Plastic PSO28



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			4.72			.120
a1	.078		.551	.002		.014
A2	3.62		4.17	.092		.106
B	.551		.787	.014		.020
B1 (3)	.551		.944	.014		.024
C	.236		.492	.006		.0125
D (1)	27.44		28.66	.697		.728
E (1)	12.75		13.77	.324		.350
e	1.27 NOM.			.050 NOM.		
H	17.83		19.68	.453		.500
L	.629		1.96	.016		.050

NOTES : 1. Overall length and width dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .006 per side.
2. Formed leads shall be planar with respect to one another within .004 at seating plane.
3. B1 is to allow for positive dambar protrusion.

ORDERING INFORMATION

PART NUMBER	ACCESS TIME	PACKAGE TYPE	TEMPERATURE RANGE
MK48256N-100	100ns	28 PIN 600 Mil. Plastic DIP	0°C to 70°C
MK48256N-120	120ns	28 PIN 600 Mil. Plastic DIP	0°C to 70°C
MK48256LN-100	100ns	28 PIN 600 Mil. Plastic DIP	0°C to 70°C
MK48256LN-120	120ns	28 PIN 600 Mil. Plastic DIP	0°C to 70°C
MK48256S-100	100ns	28 PIN 330 mil. PSO	0°C to 70°C
MK48256S-120	120ns	28 PIN 330 mil. PSO	0°C to 70°C
MK48256LS-100	100ns	28 PIN 330 mil. PSO	0°C to 70°C
MK48256LS-100	120 ns	28 PIN 330 mil. PSO	0°C to 70°C