CMOS DECODER FOR COMPACT DISC SYSTEMS

GENERAL DESCRIPTION

The SAA7310 (CD3A) incorporates the functions of demodulator, subcoding processor, motor speed control, error corrector and concealment in one CMOS chip. The device accepts data from the disc and outputs serial data via the Inter IC signal bus (I^2S) directly to a digital-to-analogue converter (such as the stereo CMOS dual DAC; SAA7320). The I^2S output can also be fed via the stereo interpolating digital filter SAA7220 which provides additional concealment plus over-sampling digital filtering. The SAA7310 is available in both 40-pin DIL and 44-pin QFP packages.

Features

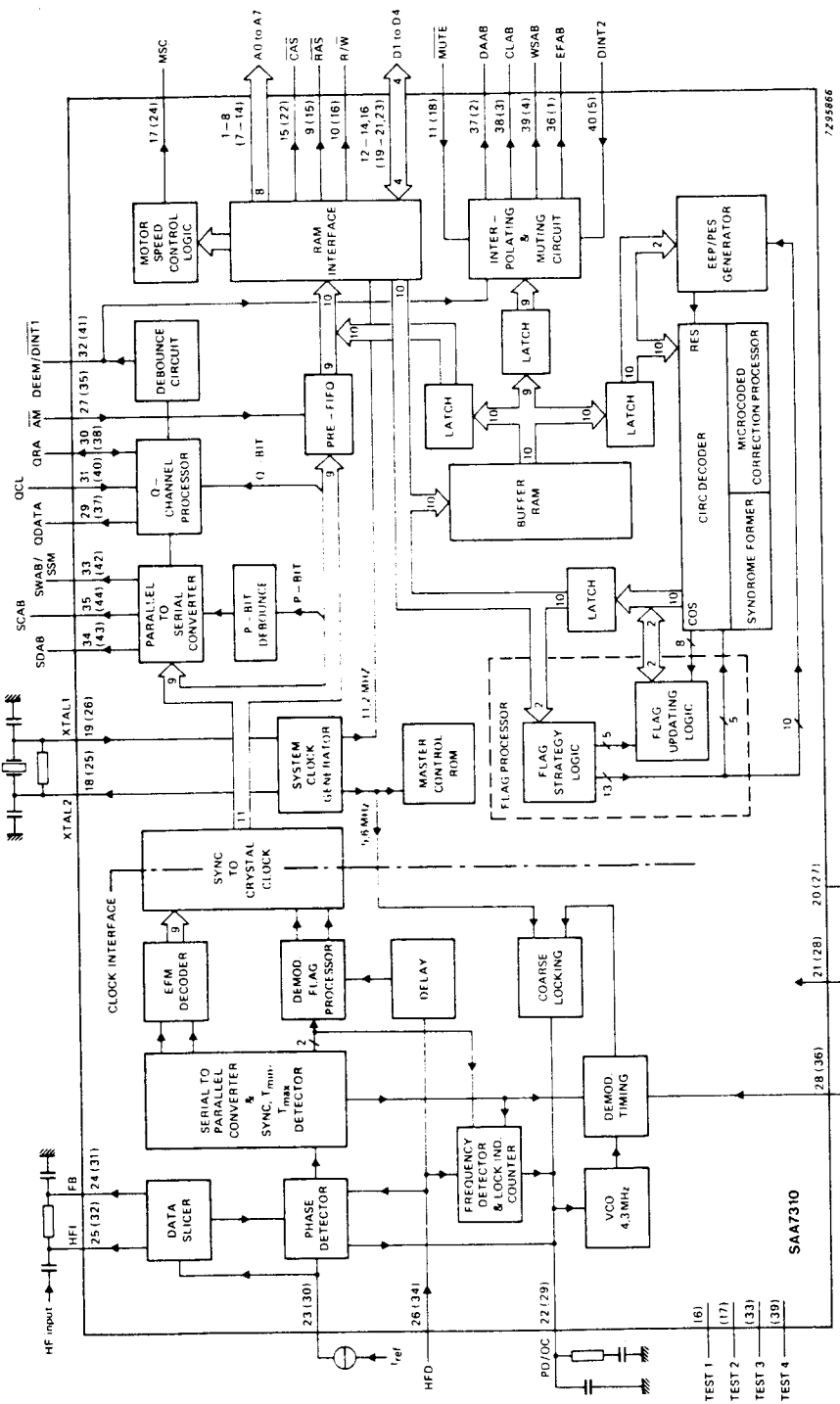
- Adaptive slicer with high-frequency level detector for input data
- Built-in drop-out detector to prevent error propagation in adaptive slicer
- Fully protected timing synchronization to incoming data
- Eight-to-Fourteen Modulation (EFM) decoding
- Adaptive CIRC error correction enabling 4 erroneous symbols per frame (32 symbols) to be corrected
- Subcoding microprocessor handshaking protocol
- Motor speed control logic which stabilizes the input data rate
- Error flag processing to identify unreliable data
- Concealment to replace uncorrectable data
- I^2S bus for data exchange
- Bidirectional data bus to external RAM (16 K x 4 bits) with 64-frame FIFO capacity
- Demodulator PLL requiring virtually no peripheral components
- Replacement for the CD2A
- Low power consumption (typ. 175 mW)
- Track loss correction by additional muting
- Non-digital audio interface application (such as CD-ROM or CD-I)
- 2-package option
- −40 to +85 °C operating temperature range

QUICK REFERENCE DATA

parameter	symbol	min.	typ.	max.	unit
Supply voltage	V_{DD}	4,5	5,0	5,5	V
Supply current	I_{DD}	–	35	50	mA
Data slicer input voltage (peak-to-peak value)	$V_{I(p-p)}$	0,5	–	2,5	V
Oscillator operating frequency					
XTAL	f_{XTAL}	10,16	11,2896	12,42	MHz
VCO (PLL locked on to data)	f_{VCO1}	2,54	4,3218	6,21	MHz
Output current (each output)	I_O	−10	–	+ 10	mA
Operating ambient temperature	T_{amb}	−40	–	+ 85	°C

PACKAGE OUTLINES

SAA7310P : 40-lead DIL; plastic (SOT-129).
SAA7310GP : 44-lead QFP; plastic (SOT-205A).



Pins in parenthesis relate to 44-pin QFP package.

Fig. 1 Block diagram.

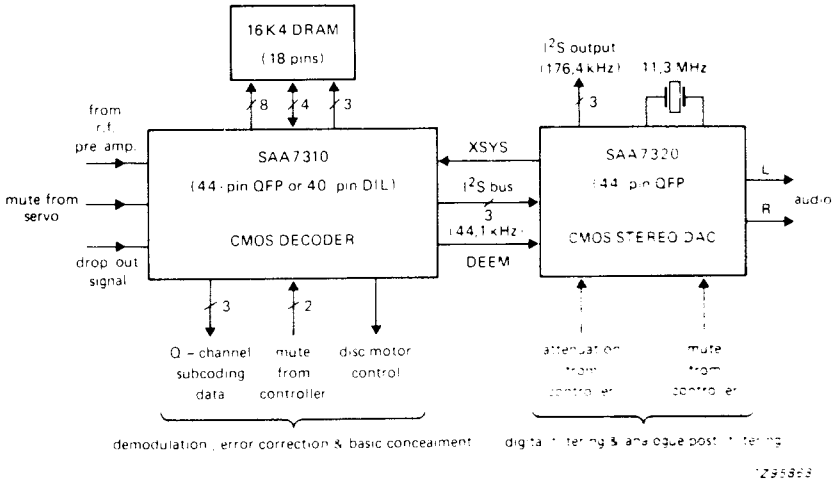


Fig. 2 (a) Block diagram of SAA7310 as used with SAA7320.

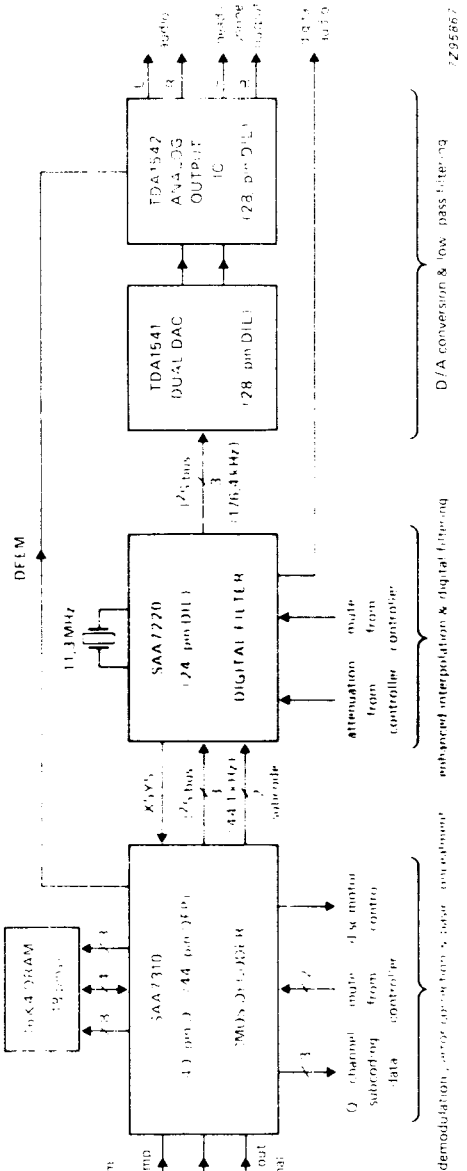


Fig. 2 (b) Block diagram of SAA7310 as used with SAA7220.

PINNING

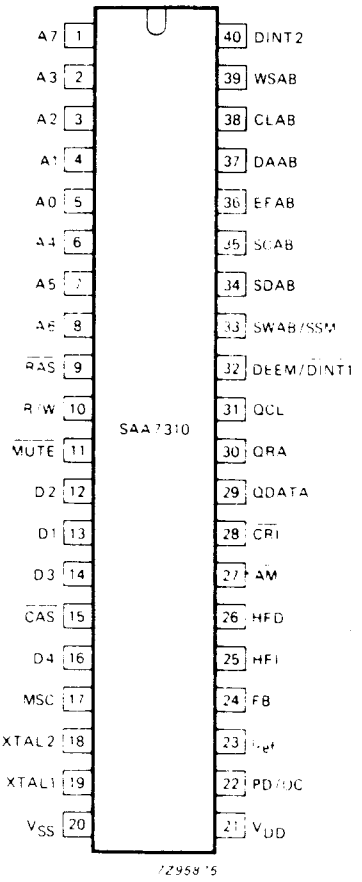


Fig. 3 Pinning diagram, for 40 lead DIL package.

PINNING (continued)

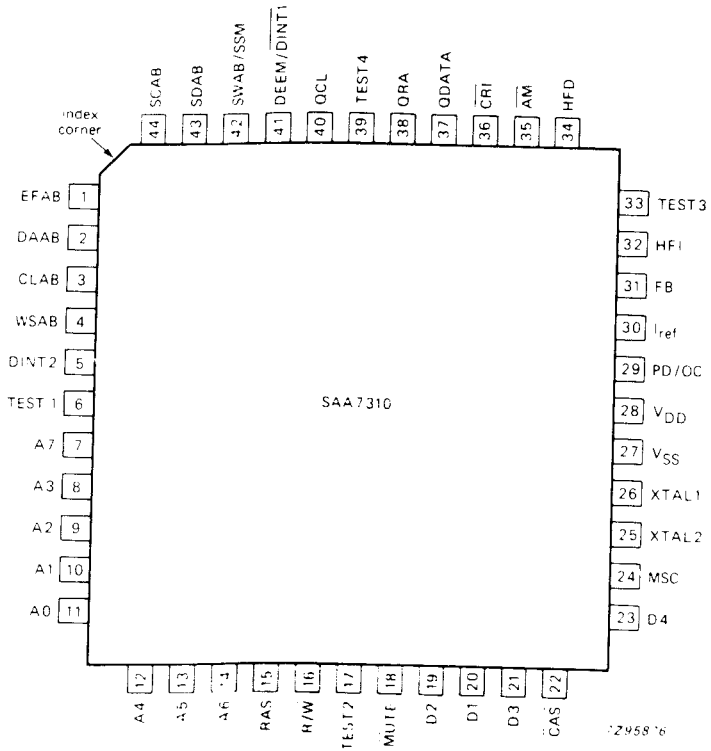


Fig. 4 Pinning diagram; for 44-lead QFP package.

DEVELOPMENT DATA

Pin functions

pin no. DIL	pin no. QFP	mneumonic	description
1 - 8	7 - 14	A0 - A7	**Address:** address outputs to external RAM.
9	15	$\overline{RAS}$	**Row Address Select:** output to external RAM (4416) which uses multiplexed address inputs.
10	16	R/$\overline{W}$	**Read/Write:** output signal to external RAM.
11	18	$\overline{MUTE}$	**Mute:** input from the microprocessor. When mute is LOW the data output DAAB, pin 37 (2), is attenuated to zero in 15 successive divide-by-2 steps. On the rising edge of mute the data output is incremented to the first 'good' value in 2 steps. This input has an internal pull-up of 50 kΩ (typ.).
12 - 14	19 - 21	D1 - D3	**Data:** data inputs/outputs to external RAM.
15	22	$\overline{CAS}$	**Column Address Select:** output signal to external RAM.
16	23	D4	**Data:** data input/output to external RAM.
17	24	MSC	**Motor Speed Control:** open drain output which provides a pulse width modulated signal with a pulse rate of 88 kHz to control the rate of data entry. The duty factor varies from 1,6% to 98,4% in 62 steps. When a motor-start signal is detected via pin 33 (42) (SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds, followed by a continuous 50% duty factor.
18	25	XTAL2	**Crystal oscillator output:** drive output to clock crystal (11,2896 MHz typ.).
19	26	XTAL1	**Crystal oscillator input:** input from crystal oscillator or slave clock.
20	27	V_{SS}	**Ground:** circuit earth potential.
21	28	V_{DD}	**Power Supply:** positive supply voltage (+ 5 V).
22	29	PD/OC	**Phase Detector output/ Oscillator Control input:** outputs of the frequency detector and phase detector are summed internally, then filtered at this pin to provide the frequency control signal for the VCO.
23	30	I_{ref}	**Current reference:** external reference input to the phase detector and data slicer. This input is required to minimize the spread in the charge pump output of the phase detector and data slicer.
24	31	FB	**Feedback:** output from the input data slicer. This output is a current source of 100 μA (typ.) which changes polarity when the level detector input HFI at pin 25 (32) rises above the threshold voltage of 2 V (typ.). When a data run length violation is detected (e.g. during drop-out), or when HFD at pin 26 (34) is LOW, this output goes to a high impedance state.

FUNCTIONAL DESCRIPTION

All references to pin numbers show the 40-lead DIL pin first followed by the 40-lead QFP pin in parenthesis.

Demodulation

Data read from the disc is amplified and filtered externally and then converted into a clean digital signal by the data slicer. The data slicer is an adaptive level detector which relies on the nature of the eight-to-fourteen modulation system (EFM) to determine the optimum slicing level. When a signal drop-out is detected (via the HFD input, or internally when a data run length violation is detected) the feedback (FB) to the data slicer is disabled to stop drift of the slicing level.

Two frequency detectors, a phase detector and a voltage-controlled oscillator (VCO) form an internal phase-lock loop (PLL) system. The voltage-controlled oscillator (VCO) runs at the input data rate (typically at 4,3218 MHz), its frequency being dependent on the voltage at pin 22 (29) (PD/OC). One of the frequency detectors compares the VCO frequency with that of the crystal clock to provide coarse frequency-control signals which pull the VCO to within the capture range of fine frequency control. Signals for fine frequency control are provided by the second frequency detector which uses data run length violations to pull the VCO within the capture range of the PLL. When the system is phase-locked the frequency detector output stage is disabled via a lock indication signal. The VCO output provides the main demodulator clock signal which is compared with the incoming data in the phase detector. The output of the phase detector, which is combined internally with the frequency detector outputs at pin 22 (29), is a positive and negative current pulse with a net charge that is dependent on the phase error. The current amplitude is determined by the current source I_{ref} connected to pin 23 (30).

The demodulator uses a double timing system to protect the EFM decoder from erroneous sync patterns in the data. The protected divide-by-588 master counter is reset only if a sync pattern occurs exactly one frame after a previous sync pattern (sync coincidence) or if the new sync pattern occurs within a safe window determined by the divide-by-588 master counter. If track jumping occurs the divide-by-588 master counter is allowed to free-run to minimize interference to the motor speed controller; this is achieved by taking the CRI input at pin 28 (36) LOW to inhibit the reset signal.

The sync coincidence pulse is also used to reset the lock indication counter and disable the output from the fine frequency detector. If the system goes out of lock, the sync pulses cease and the lock indication counter counts frame periods. After 63 frame periods with no sync coincidence pulse, the lock indication counter enables the frequency detector output.

The EFM decoder converts each symbol (14 bits of disc data + 3 merging bits) into one of 256 8-bit digital words which are then passed across the clock interface to the subcoding section. An additional output from the decoder senses one of two extra symbol patterns which indicate a subcoding frame sync. This signal together with a data strobe and two error flags are also passed across the clock interface. The error flags are derived from the HFD input and from detected run length violations.

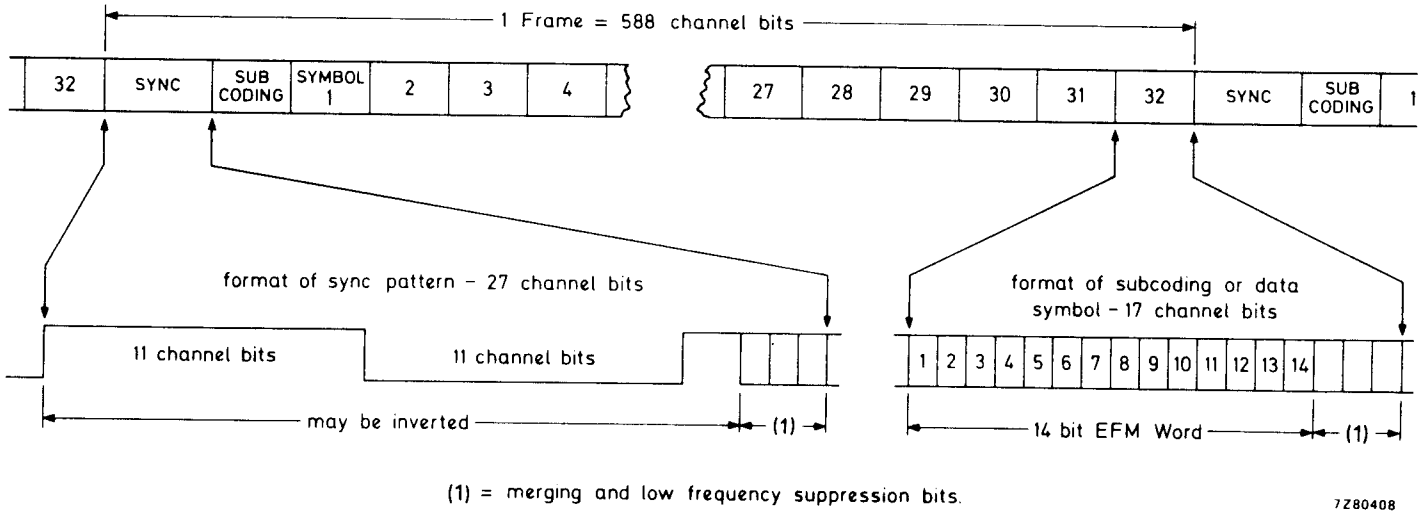


Fig. 5 Data input signal.

FUNCTIONAL DESCRIPTION (continued)

Subcoding

The subcoding section has four main functions

- Q-channel processor
- De-emphasis output
- Pause (P-bit) output
- Serial subcoding output

The Q-channel processor accumulates a subcoding word of 96 bits from the Q-bit of successive subcoding symbols, performs a cyclic redundancy check (CRC) using 16 bits and then outputs the remaining 80 bits to a microprocessor on an external clock. The de-emphasis signal (DEEM) is derived from one bit of the CRC checked Q channel. The DEEM output pin 32 (41) is additionally protected by a debounce circuit.

The P-bit from the subcoding symbol, also protected by a debounce circuit, is output via the serial subcoding signal (SDAB) at pin 34 (43). The protected timing used for the EFM decoder makes this output unreliable during track jumping.

The serial output consists of a burst of 10 bits of data clocked by a burst clock (SCAB). The 10 bits are made up from subcoding signal bits Q to W, the Q channel parity check flag, a demodulator error flag and the subcoding sync signal. At the end of the clock burst this output delivers the debounced P-bit signal which can be read externally in the rising edge of SWAB at pin 33 (42); see Fig. 6.

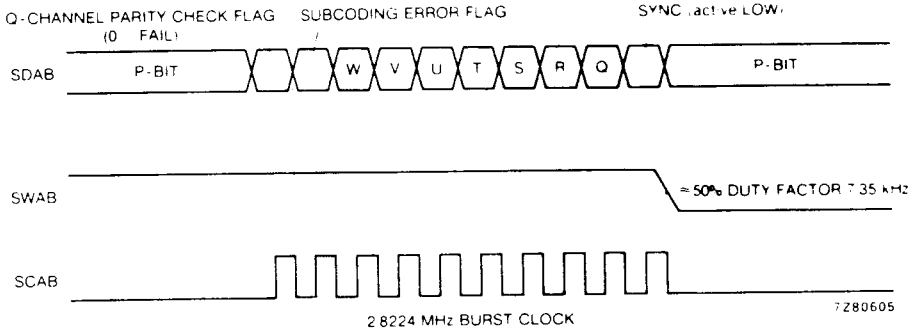


Fig. 6 Typical subcoding waveform outputs.

Pre-FIFO

The 10 bits (8 bits of symbol data + 2 error flag bits) which are passed from the demodulator across the clock interface to the subcoding section are also fed to the pre-FIFO with the addition of two timing signals. These two timing signals indicate:

(1) That a new data symbol is valid
(2) Whether the new data symbol is the first symbol of a frame

The pre-FIFO stores up to 4-symbols (including flags) and acts as a time buffer between data input and data output. Data passes into the pre-FIFO at the rate of 32 symbols per demodulator frame and the symbols are called from the pre-FIFO into RAM storage at the rate of 32 symbols per error-correction frame. The timing, organized by the master controller, allows up to 40 attempts to write 32 symbols into the RAM per error-correction frame. The 8 extra attempts allow for transient changes in clock frequency.

Data control

This section controls the flow of data between the external RAM and the error corrector. Each symbol of data passes through the error corrector two times (correction processes C1 and C2) before entering the concealment section.

The RAM interface uses the full crystal frequency of 11,2 MHz to determine the RAM access waveforms (the main clock for the system is 5,6 MHz). One RAM access (READ or WRITE) uses 12 crystal clock cycles which is approximately 1 μs. The timing (see Fig. 8) is based upon the specification for the dynamic 16 K x 4-bit RAM (4416). This RAM requires multiplexed address signals and therefore, in each access cycle, a row address $\overline{RAS}$ pin 9 (15) is set up first and then three 4-bit nibbles are accessed using sequential column addresses $\overline{CAS}$ pin 15 (22). As only 10 bits are used for each symbol (including flags), the fourth nibble is not accessible.

There are 4 different modes of RAM access:

- WRITE 1
- READ 1
- WRITE 2
- READ 2

During WRITE 1, data is taken from pre-FIFO at regular intervals and written into one half of the RAM. This half of the RAM acts as the main FIFO and has a capacity of up to 64 frames. During READ 1, the 32 symbols of the next frame due out are read from the FIFO. The numerical difference between the WRITE 1 and READ 1 addresses is used to control the speed of the disc drive motor.

When a frame of data has been read from the FIFO it is stored in a buffer RAM until it can be accepted by the CIRC error correction system. At this time the error correcting strategy of the CIRC decoder for the frame is determined by the flag processor. The frame for correction is then loaded into the decoder one symbol at a time and the 32 symbols from the previous correction are returned to the buffer RAM.

After the first correction (C1), only 28 of the symbols are required per frame. The symbols are stored in the buffer RAM together with new flags generated after the correction cycle by the flag updating logic. This partially-corrected frame is then passed to the external RAM by a WRITE 2 instruction. The de-interleaving process is carried out during this second passage through the external RAM. The WRITE 2 and READ 2 addresses for each symbol provide the correct delay of 108 frames for the first symbol and zero delay for the last symbol.

After execution of the READ 2 instruction, the frame of 28 symbols is again stored in the buffer RAM pending readiness of the CIRC decoder and calculation of decoding strategy. Following the second correction (C2), 24 symbols including unreliable data flags (URD) are stored in the buffer RAM and then output to the concealment section at regular intervals.

Flag processing

Flag processing is carried out in two parts as follows:

- Flag strategy logic
- Flag updating logic.

While a frame of data from the external memory is being written into the buffer RAM, the error flags associated with that frame are counted. Two bits are used for the flags, thus 'good' data (flags = 00) and three levels of error can be indicated.
The optimum strategy to be used by the CIRC error corrector is determined by the 2-bit flag information used by the flag strategy logic ROM in conjunction with its associated arithmetic unit (ALU). The flags for the C1 correction are generated in the demodulator and are based on detected signal drop-outs and data run length violations. Updating of the flags after C1 is dependent on the CIRC decoder correction of that frame. The updated flags are used to determine the C2 strategy. After C2 correction a single flag (URD) is generated to accompany the data into the concealment section.

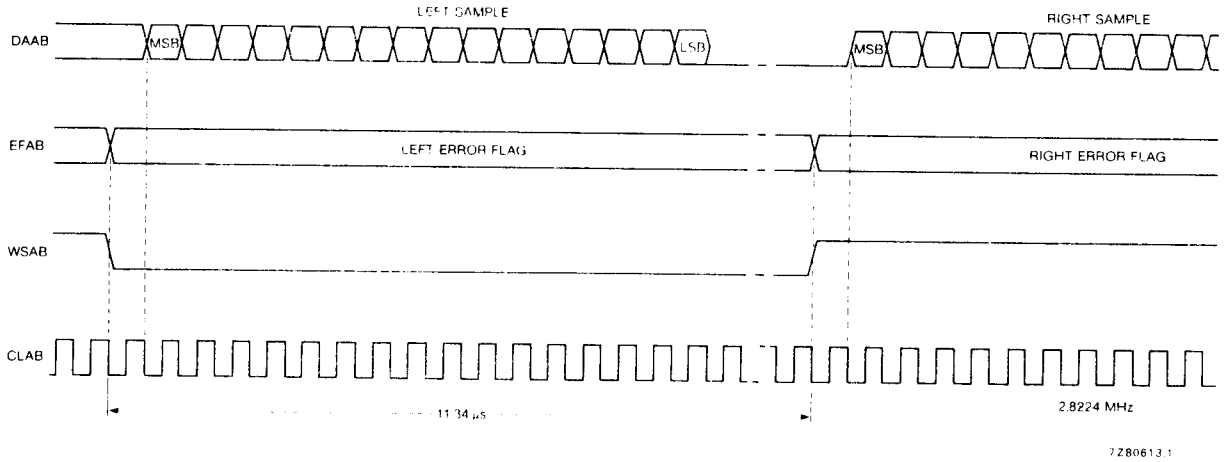


Fig. 7 Typical I²S waveform outputs to SAA7220 or SAA7320.

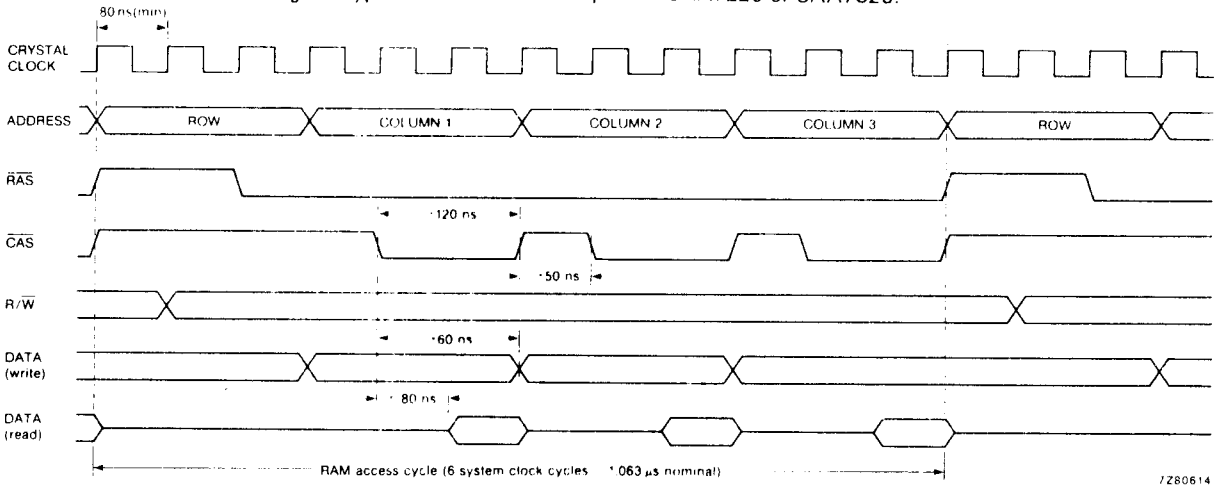


Fig. 8 RAM timing waveforms: timings based on RAM TMS4416; $\bar{G}$ input to RAM held LOW.

CIRC Decoding

Data on the compact disc is encoded according to a cross-interleaved Reed-Solomon code (CIRC) and this decoder exploits fully the error-correction capabilities of the code.

Decoding is performed in two cycles and in each cycle the CIRC decoder corrects data in accordance with the following formula:

$$2t + e = 4$$

Where:

e = the number of erasures (erroneous symbols whose position is known).
t = allowed number of additional failures which the decoder program has to find.

The flag processor points to the erasure symbols and tells the CIRC decoder how many additional failures are allowed. If the error corrector is presented with more than the maximum it will stop and flag all symbols as unreliable.

The CIRC decoder is comprised of two sections:

Syndrome formation

Four correction syndromes are calculated while the frame of data is being written into a symbol memory. From these syndromes errors can be detected and corrected.

Microcoded correction processing

The processor uses an Arithmetic Logic Unit (ALU) which includes a multiplier based on logarithms. The correction algorithm follows the microcode program stored in a ROM.

Concealment

This section combines 8-bit data symbols into left and right stereo channels. Each channel has a 16-bit capacity and holds two symbols (a stereo sample). The channels operate independently. A concealment operation is performed when a URD flag accompanies either symbol in a stereo sample. If a single erroneous sample is flagged between two 'good' samples then linear interpolation is used to replace the erroneous value. If two or more successive samples are flagged, a sample and hold is applied and the last of the erroneous samples is interpolated to a value between that of the hold and that of the following 'good' sample.

When using the CD3A in a non-digital audio application, pins DINT2 and DEEM/$\overline{\text{DINT1}}$ should be set to logic 0 and logic 1 respectively. The URD flag will then be disabled to prevent data being interpolated.

If MUTE is requested, the data in each channel is attenuated to zero in 15 successive divide-by-two steps. At the end of a mute period the output is incremented to the first 'good' value in two steps using the interpolator.

All erroneous data supplied to the concealment section continues to be flagged when it is output to the SAA7220 where it receives additional and more efficient concealment (see Fig. 9).

FUNCTIONAL DESCRIPTION (continued)

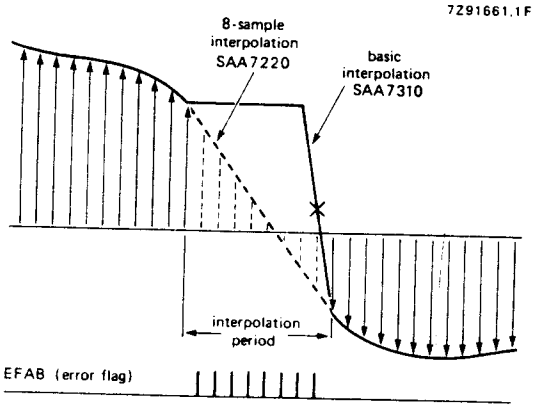


Fig. 9 The SAA7220 can make an 8-sample linear interpolation, the SAA7310 a hold and single-sample interpolation. When interpolating more than 8 samples, a hold function operates in the SAA7220 before the interpolation.

Non-digital audio applications

The CD3A contains a special mode for non-digital applications such as CD-ROM and CD-I. In this mode the concealment section is not allowed to operate. The flagged output words of the error correction circuit are passed to the output DAAB without being affected by the interpolation circuit. The EFAB output signal indicates unreliable output words on a sample basis when one or both bytes in a sample are unreliable. This is necessary as the CD-ROM/CD-I player performs its own error correction strategy on the data. The level of data integrity has to be much higher to ensure no errors occur in text or numerical information.

Specifications of CD-ROM and CD-I modes are available on request.

Motor speed control (see Fig. 10)

The motor speed control (MSC) output from pin 17 (24) is a pulse-width modulated signal. The duty factor of the pulse-width modulation is calculated from the difference in numerical value between the WRITE 1 and READ 1 addresses, the difference being nominally half of the FIFO space. The calculation is performed at a rate of 88,2 kHz.

The duty factor of MSC varies in 62 steps from 1,6% (FIFO full) to 98,4% (FIFO empty). When a motor-start signal is detected (via SWAB/SSM) the duty factor is forced to 98,4% for 0,2 seconds followed by a normal, calculated signal. After a motor-stop signal is detected the duty factor is forced to 1,6% for 0,2 seconds followed by a continuous 50% duty factor. A change in motor start/stop status occurring within the 0,2 second periods overrides the previous condition and resets the data control timer.

Track loss correction

The CD3A also incorporates a function to provide extra correction during track loss. Should track loss occur, the additional mute pin ($\overline{AM}$) should be taken LOW, which forces the data LOW at the pre-FIFO stage. This muted data is then corrected after de-interleaving. This function is particularly useful for applications where mechanical shock is likely to occur.

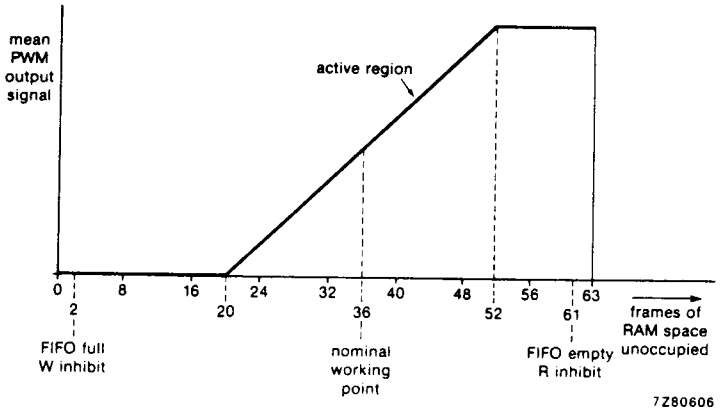


Fig. 10 Motor speed control.

CD2A replacement

The CD3A can become a direct replacement for the CD2A by externally connecting pin 21 to V_{DD} and modifying the PLL peripheral components (see Fig. 12).

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

parameter	symbol	min.	max.	unit
Supply voltage, pin 21 (28)	V_{DD}	−0,5	+ 6,5	V
Maximum input voltage	V_I	−0,5	V_{DD} + 0,5	V
Input current, pin 23 (30)	I_I	−	5	mA
Maximum output voltage MSC, QRA, SWAB/SSM	V_O	−0,5	+ 6,5	V
Output current (each output)	I_O	−	± 10	mA
DC V_{SS} or V_{DD} current	I_{DD} or I_{SS}	−	± 100	mA
DC input diode current	I_{IK}	−	± 20	mA
DC output diode current	I_{OK}	−	± 20	mA
Storage temperature range	T_{stg}	−55	+ 150	°C
Operating ambient temperature range	T_{amb}	−40	+ 85	°C
Electrostatic handling*	V_{es}	−1000	+ 1000	V

INTER·IC I²S SOUND

Purchase of Philips' I²S components conveys a license under the Philips' I²S patent to use the components in the I²S-system provided the system conforms to the I²S specification defined by Philips.

Detailed information on the I²S bus specification is available on request.

Supply of this Compact Disc IC does not convey an implied licence under any patent right to use this IC in any Compact Disc application.

* Equivalent to discharging a 100 pF capacitor through a 1,5 kΩ series resistor with a rise time of 15 ns.

CHARACTERISTICS

V_{DD} = 4,5 to 5,5 V; V_{SS} = 0 V; T_{amb} = −40 to + 85 °C unless otherwise specified

parameter	conditions	symbol	min.	typ.	max.	unit
Supply						
Supply voltage, pin 21 (28)		V_{DD}	4,5	5,0	5,5	V
Supply current, pin 21 (28)		I_{DD}	–	35	50	mA
Inputs						
D1 – D4, QCL, $\overline{AM}$, DEEM/$\overline{DINT1}$, DINT2						
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input leakage current	note 2	I_{LI}	−10	–	+ 10	μA
Input capacitance		C_I	–	–	10	pF
$\overline{MUTE}$, $\overline{CRI}$						
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Internal pull-up impedance	V_I = 0 V	$\lvert Z_I \rvert$	18	50	110	kΩ
Input capacitance		C_I	–	–	10	pF
QRA, SWAB/SSM						
Input voltage LOW	note 1	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	note 1	V_{IH}	2,0	–	V_{DD} + 0,5	V
Input capacitance		C_I	–	–	10	pF
Internal pull-up impedance	V_I = 0 V	$\lvert Z_I \rvert$	3,9	10	18	kΩ
HFD						
Input voltage LOW		V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH		V_{IH}	2,0	–	clamped	V
Input clamping voltage	I_I = 100 μA	V_{CL}	2,0	3,0	4,5	V
Input source current		I_S	−100	–	100	μA
Input capacitance		C_I	–	–	10	pF
Internall pull-up impedance	V_I = 0 V	$\lvert Z_I \rvert$	18	50	110	kΩ

DEVELOPMENT DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Outputs						
A0–A7, R/$\overline{W}$, D1–D4, $\overline{CAS}$, $\overline{RAS}$, QDATA, DEEM/$\overline{DINT1}$, SDAB, SCAB, EFAB, DAAB, CLAB, WSAB, TEST1, TEST2, TEST3, TEST4						
Output voltage LOW	$-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH	I_{OH} = 0,2 mA	V_{OH}	3,0	–	V_{DD}	V
Load capacitance		C_L	–	–	50	pF
Leakage current	note 2	I_{LO}	−10	–	+ 10	μA
MSC (open drain)						
Output voltage LOW	$-I_{OL}$ = 1 mA	V_{OL}	0	–	0,35	V
Load capacitance		C_L	–	–	50	pF
Leakage current	note 2	I_{LO}	−10	–	+ 10	μA
SWAB/SSM, QRA (open drain)						
Output voltage LOW	$-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Load capacitance		C_L	–	–	50	pF
Internal load resistance		R_L	3,9	10	18	kΩ
ANALOGUE CIRCUITS						
Data slicer (see Fig. 11)						
Input HFI						
AC input voltage range (peak-to-peak value)		$V_{I(p-p)}$	0,5	–	2,5	V
Input impedance						
normal (HFD HIGH)		$\|Z_I\|$	500	–	–	kΩ
disabled (HFD LOW)		$\|Z_I\|$	50	100	200	kΩ
Input capacitance		C_I	–	–	10	pF
Output FB						
Output current	V_{FB} = 2 V	I_O	$I_{ref}/5$ −20%	$I_{ref}/5$	$I_{ref}/5$ +20%	μA

parameter	conditions	symbol	min.	typ.	max.	unit
Phase detector						
Output PD/OC	see Fig. 12					
Output current	PD/OC = 1 to 3 V	I_O	$\pm I_{ref}-20\%$	$\pm I_{ref}$	$\pm I_{ref}+20\%$	μA
Control range	note 3	α	±2,1	–	--	rad
Input I_{ref}	see Fig. 13					
Input reference current		I_{ref}	–	500	*	μA
Fine frequency detector						
Output PD/OC						
Output impedance		$\|Z_O\|$	2	4,1	5,6	kΩ
Output voltage LOW	I_{OL} = 1 μA	V_{OL}	0	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 1 μA	V_{OL}	4	–	V_{DD}	V
Coarse frequency detector						
Output PD/OC	note 4					
Output impedance		$\|Z_O\|$	1	2,3	3,2	kΩ
Output voltage LOW	I_{OL} = 1 μA	V_{OL}	0	–	0,4	V
Output voltage HIGH	$-I_{OH}$ = 1 μA	V_{OL}	4	–	V_{DD}	V
Voltage controlled oscillator						
Input PD/OC						
Oscillator constant		K_{osc}	–	3,5	–	MHz/V
Crystal oscillator	see Fig. 14					
Input XTAL1						
Output XTAL2						
Mutual conductance	100 kHz	G_m	1,5	–	–	ms
Small signal voltage gain	$G_v = G_m \times R_o$	G_v	3,5	–	–	V/V
Input capacitance		C_I	–	–	10	pF
Feedback capacitance		C_{FB}	–	–	5	pF
Output capacitance		C_O	–	–	10	pF
Input leakage current	note 2	I_{LI}	−10	–	+ 10	μA

DEVELOPMENT DATA

* Value to be fixed.

parameter	conditions	symbol	min.	typ.	max.	unit
Slave clock mode	see Fig. 15					
Input voltage (peak-to-peak value)		$V_{I(p-p)}$	3,0	–	$V_{DD}+0,5$	V
Input voltage LOW	note 1	V_{IL}	−0,3	–	0,8	V
Input voltage HIGH	note 1	V_{IH}	2,4	–	$V_{DD}+0,5$	V
Input rise time	note 5	t_r	–	–	20	ns
Input fall time	note 5	t_f	–	–	20	ns
Input HIGH time (relative to clock period)	at 1,5 V	t_{HIGH}	45	–	55	%
TIMING						
Operating frequency (XTAL)		f_{XTAL}	10,16	11,2896	12,42	MHz
Operating frequency (VCO)	PLL locked on to data	f_{VCO1}	2,54	4,3218	6,21	MHz
Operating frequency (VCO)	VCO absolute limits; PLL not locked on to data	f_{VCO2}	2	–	7,5	MHz
Outputs	Figs. 16 and 17					
CEFM	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
Output HIGH time		t_{HIGH}	50	–	–	ns
DAAB, CLAB, WSAB, EFAB (I^2S format)	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
DAAB, WSAB, EFAB to CLAB						
Data set-up time		$t_{SU;DAT}$	100	–	–	ns
CLAB to DAAB, WSAB, EFAB						
Data hold time		$t_{HD;DAT}$	100	–	–	ns
SDAB, SCAB, DEEM (subcoding outputs)	note 6					
Output rise time		t_r	–	–	20	ns
Output fall time		t_f	–	–	20	ns
SDAB to SCAB						
Subcoding data set-up time		$t_{SU;SDAT}$	100	–	–	ns

parameter	conditions	symbol	min.	typ.	max.	unit
SCAB to SDAB						
Subcoding data hold time		$t_{HD;SDAT}$	100	–	–	ns
SWAB/SSM	note 6					
Output rise time		t_r	–	–	1	ns
Output fall time		t_f	–	–	100	ns
Output duty factor			–	50	–	%
Q-channel I/O	Figs 18 and 19					
QRA, QCL, QDATA						
Access time	note 7					
normal mode		$t_{ACC;N}$	0	–	13,3 + n x 13,3	ms
refresh mode		$t_{ACC;F}$	13,3	–	n x 13,3	ms
QCL to QRA						
acknowledge delay		t_{DACK}	–	–	500	ns
request hold time		$t_{HD;R}$	750	–	–	ns
QCL clock input LOW time		$t_{CK;LOW}$	750	–	–	ns
QCL clock input HIGH time		$t_{CK;HIGH}$	750	–	–	ns
QCL to QDATA delay time		t_{DD}	–	–	750	ns
Data hold time before new frame is accessed		$t_{HD;ACC}$	2,3	–	–	ms
Acknowledge time		t_{ACK}	–	–	10,8	ms

DEVELOPMENT DATA

Notes to the characteristics

1. Minimum V_{IL}, maximum V_{IH} are peak values to allow for transients.
2. $I_{LI(min)}$ and $I_{LO(min)}$ measured at $V_I = 0$ V; $I_{LI(max)}$ and $I_{LO(max)}$ measured at $V_I = V_{DD}$.
3. 1 rad = $\frac{180^o}{(3,14)}$.
4. Coarse frequency detector output PD/OC active for VCO frequencies $> \frac{f_{XTAL}}{2}$ and $< \frac{f_{XTAL}}{4}$.
5. Reference levels = 0,5 V and 2,5 V.
6. Output rise and fall times measured with load capacitance (C_L) = 50 pF.
7. Q-channel access times dependent on cyclic redundancy check (CRC);
   n = number of cycles until CRC is 'good'.

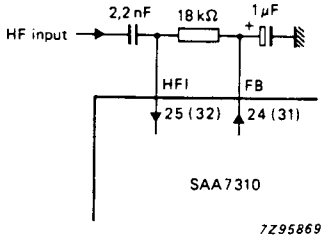


Fig. 11 Data slicer HFI input.

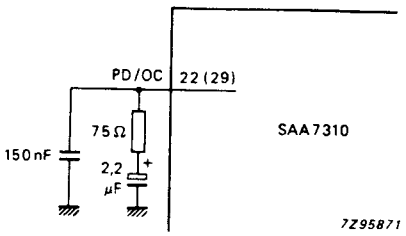


Fig. 12 PLL circuit.

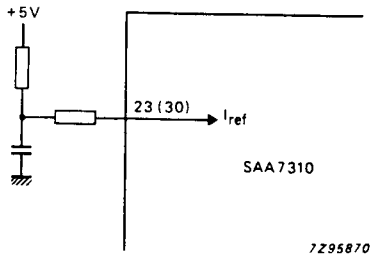


Fig. 13 I_{ref} circuit.

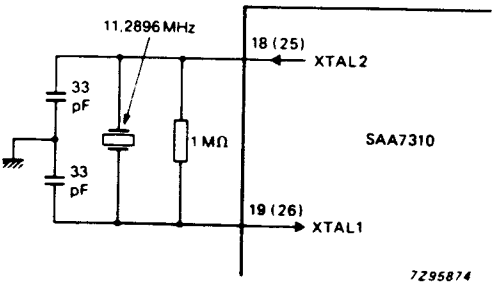


Fig. 14 Crystal oscillator circuit; using crystal type: 4322 143 05031.

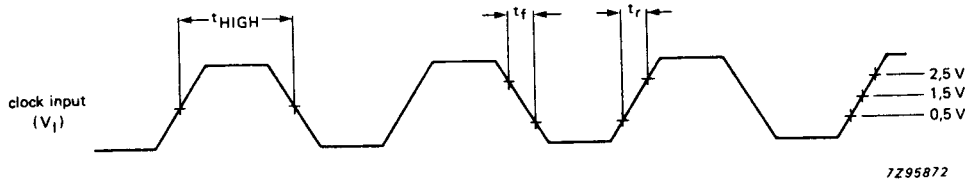


Fig. 15 Input clock timing diagram; reference levels 0,5 V, 1,5 V and 2,5 V.

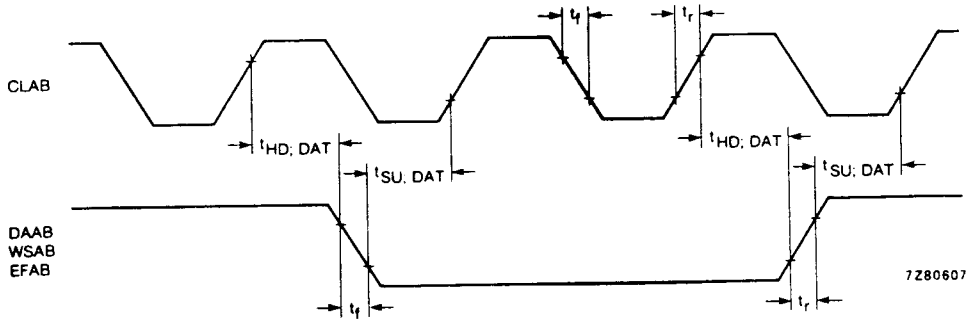


Fig. 16 Typical I²S data output waveforms; reference levels = 0,8 V and 2,0 V.

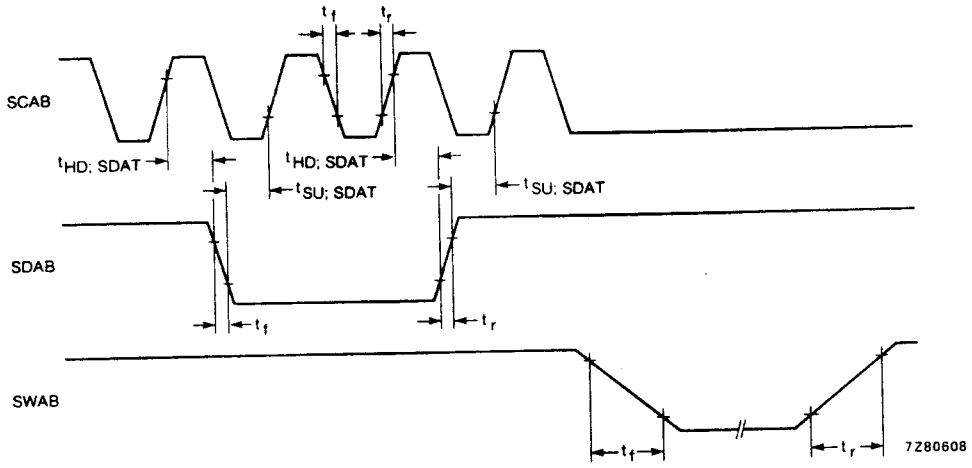


Fig. 17 Typical subcoding data output waveforms; reference levels for SCAB and SDAB = 0,8 V and 2,0 V; reference levels for SWAB = 0,8 V and 4,0 V.

DEVELOPMENT DATA

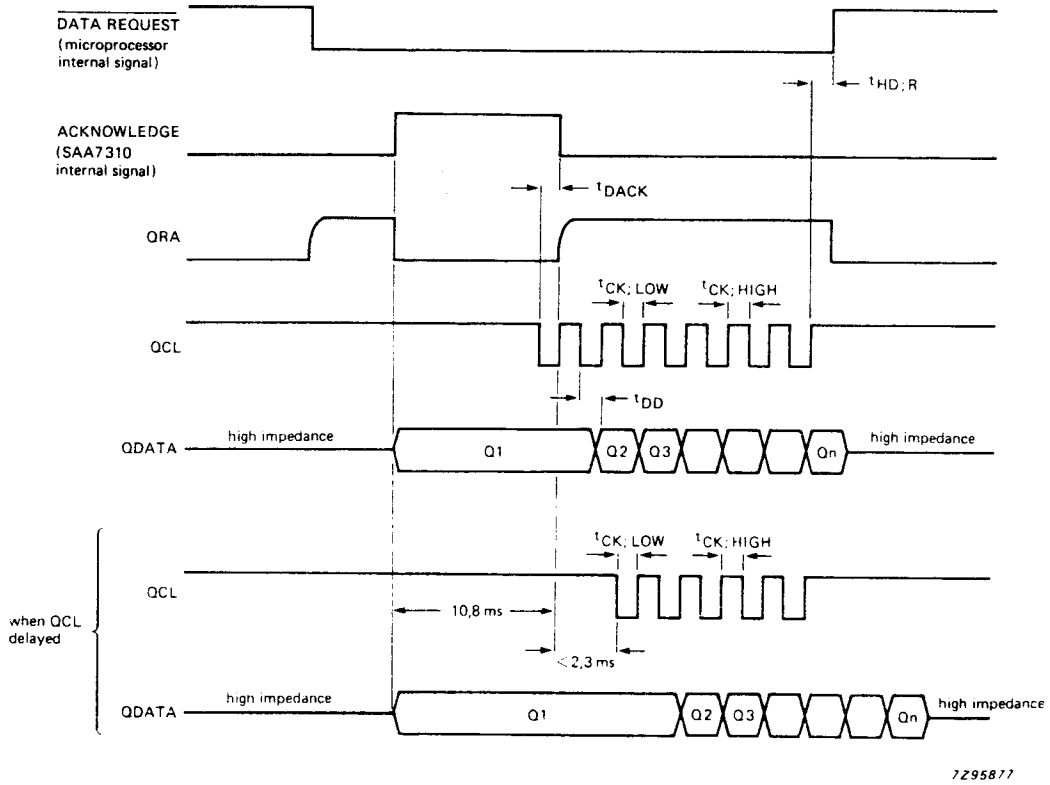


Fig. 18 Q-channel timing waveforms (normal mode).

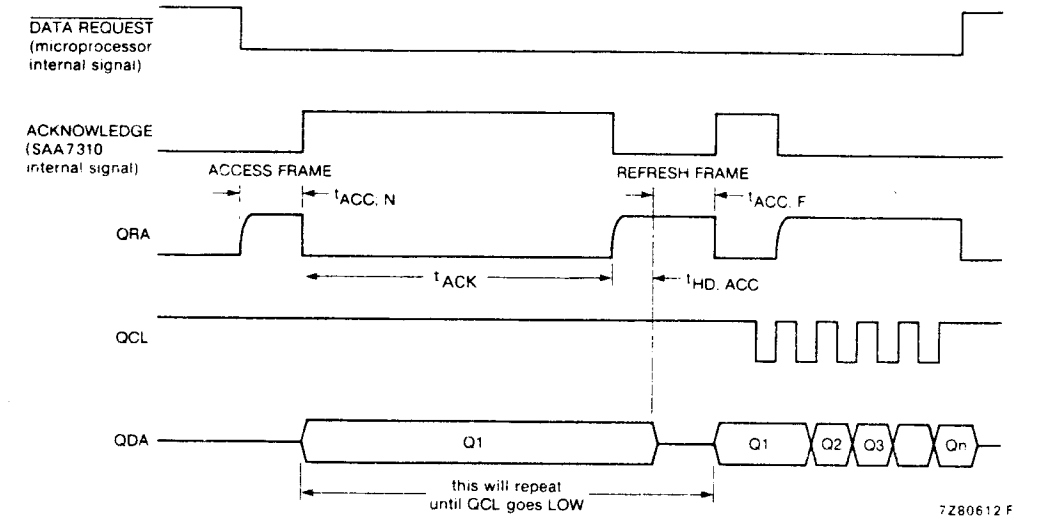


Fig. 19 Q-channel timing waveforms (refresh mode).

APPLICATION INFORMATION

EFM Encoding system

The Eight-to-Fourteen Modulation (EFM) code used in the Compact Disc Digital Audio system is designed to restrict the bandwidth of the data on the disc and to present a DC free signal to the demodulator. In this modulation system the data run length between transitions is $\geqslant 3$ clock periods and $\leqslant 11$ clock periods. The number of bits per symbol is 17, including three merging and low frequency suppression bits which also assist in the removal of the DC content.

The conversion from 8-bit, non-return-to-zero (NRZ) symbols to equivalent 14-bit code words is shown in Table 2. C1 is the first bit of a 14-bit code word read from the disc and D1 is the Most Significant Bit (MSB) of the data sent to the error corrector. The 14-bit code words are given in NRZ-I representation in which a logic 1 means a transition at the beginning of that bit from HIGH-to-LOW or LOW-to-HIGH (see Fig. 20).

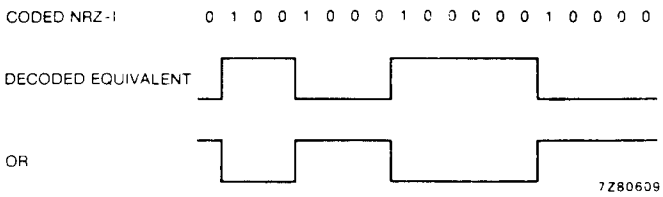


Fig. 20 Non Return to Zero (NRZ) representation.

The codes shown in Table 2 cover the normal 256 possibilities for an 8-bit data symbol. There are other combinations of 14-bit codes which, although they obey the EFM rules for maximum and minimum run length (T_{max}, T_{min}), produce unspecified data output symbols. Two of these extra codes are used in the subcoding data to define a subcoding frame sync and are as shown in Table 1.

Table 1 Codes used to define subcoding frame sync

8-bit NRZ data symbol								14-bit equivalent code word													
D1	D2	D3	D4	D5	D6	D7	D8	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	C11	C12	C13	C14
x	0	0	1	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	1
x	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	1	0
P	Q	R	S	T	U	V	W														

Where: X = don't care state.

When a subcoding frame sync is detected the P-bit (Pause-bit) of the data is ignored by the debounce circuitry. The remaining bits (Q to W) are not specified in the system but always appear at the serial output as shown in Table 1.

APPLICATION INFORMATION (continued)

Table 2 EFM code conversion

No.	DNZ data symbol D1 D8	equivalent code word C1 C14	No.	DNZ data symbol D1 D8	equivalent code word C1 C14
0	0 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 0	128	1 0 0 0 0 0 0 0	0 1 0 0 1 0 0 0 1 0 0 0 0 1
1	0 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 0 0 0 0 0 0	129	1 0 0 0 0 0 0 1	1 0 0 0 0 1 0 0 1 0 0 0 0 1
2	0 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 0	130	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 0 1 0 0 0 0 1
3	0 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 0	131	1 0 0 0 0 0 1 1	1 0 0 0 1 0 0 0 1 0 0 0 0 1
4	0 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 0 0 0 0 0 0	132	1 0 0 0 0 1 0 0	0 1 0 0 0 1 0 0 1 0 0 0 0 1
5	0 0 0 0 0 1 0 1	0 0 0 0 0 1 0 0 0 1 0 0 0 0	133	1 0 0 0 0 1 0 1	0 0 0 0 0 0 0 0 1 0 0 0 0 1
6	0 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 0	134	1 0 0 0 0 1 1 0	0 0 0 1 0 0 0 0 1 0 0 0 0 1
7	0 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 0 0 0 0 0 0	135	1 0 0 0 0 1 1 1	0 0 1 0 0 1 0 0 1 0 0 0 0 1
8	0 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 0	136	1 0 0 0 1 0 0 0	0 1 0 0 1 0 0 1 0 0 0 0 0 1
9	0 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 0	137	1 0 0 0 1 0 0 1	1 0 0 0 0 0 0 1 0 0 0 0 0 1
10	0 0 0 0 1 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 0	138	1 0 0 0 0 0 1 0	1 0 0 1 0 0 0 1 0 0 0 0 0 1
11			139		
to			to		
119			247		
120	0 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 0 0 0 1 0	248	1 1 1 1 1 0 0 0	0 1 0 0 1 0 0 0 0 1 0 0 1 0
121	0 1 1 1 1 0 0 1	0 0 0 0 1 0 0 1 0 0 1 0 0 0	249	1 1 1 1 1 0 0 1	1 0 0 0 0 0 0 0 1 0 0 1 0
122	0 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 0 0 0 1 0 0	250	1 1 1 1 1 0 1 0	1 0 0 1 0 0 0 0 1 0 0 1 0
123	0 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 0 0 0 1 0 0	251	1 1 1 1 1 0 1 1	1 0 0 0 1 0 0 0 1 0 0 1 0
124	0 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 0 0 0 1 0 0	252	1 1 1 1 1 1 0 0	0 1 0 0 0 0 0 0 1 0 0 1 0
125	0 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 0 0 1 0 0	253	1 1 1 1 1 1 0 1	0 0 0 0 1 0 0 0 0 1 0 0 1 0
126	0 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 0 0 1 0 0	254	1 1 1 1 1 1 1 0	0 0 0 1 0 0 0 0 0 1 0 0 1 0
127	0 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 0 0 1 0 0	255	1 1 1 1 1 1 1 1	0 0 1 0 0 0 0 0 0 1 0 0 1 0

Subcoding microprocessor handshaking protocol (see Figs. 18, 19 and 21)

The QRA line is normally held LOW by the microprocessor.

When the microprocessor needs data (Request) it releases the QRA line and allows it to be pulled HIGH by the pull-up resistor in the SAA7310.

The SAA7310 is continuously collecting Q-channel data and when it detects that QRA is HIGH it holds the first frame of Q-channel data for which the Cyclic Redundancy Check (CRC) is 'good'. Then the SAA7310 pulls QRA LOW to tell the microprocessor that the data is ready (Acknowledge) and enables the QDATA output.

When the microprocessor detects a QRA LOW signal it generates a clock signal (QCL) to shift the data out from the SAA7310 to the microprocessor via the QDATA output. The first negative edge of QCL also resets the acknowlegde signal and thus releases the QRA line.

As soon as the microprocessor has received sufficient data (not necessarily 80 bits) it pulls the QRA line LOW again. The SAA7310 now disabled the QDATA output and resumes collecting new Q-channel data.

If the microprocessor does not generate a QCL signal within 10,8 ms from the start of the acknowledge (QRA LOW), the SAA7310 resets the acknowledge signal and allows the QRA line to go HIGH again. The microprocessor still has 2,3 ms to accept the data, which allows for a long propagation delay in the microprocessor. After a further 13,33 ms the SAA7310 will have received a new frame of Q-channel data and, provided the CRC is 'good', will give a fresh acknowledge signal. This refreshing process is repeated until the microprocessor accepts the data or stops the request.

When the microprocessor has a requirement to hold the data for a long period before acceptance, it prevents the refreshing process by setting QCL LOW after any acknowledge signal.

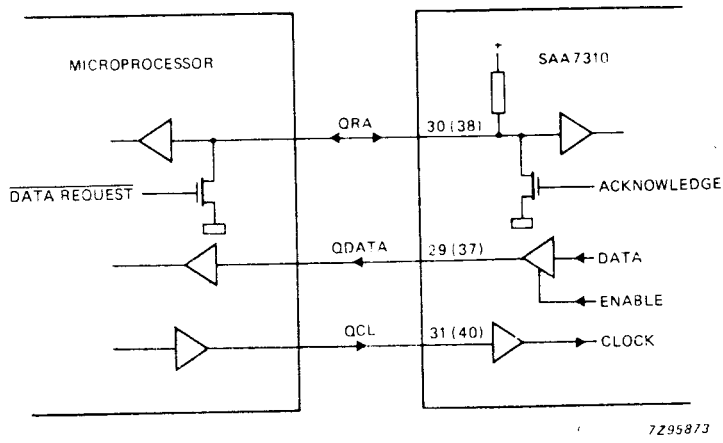


Fig. 21 Microprocessor handshaking protocol.