S72WS-P based MCP/PoP Products

1.8 Volt-only x16 Flash Memory and SDRAM on Split Bus Simultaneous Read/Write, Burst Mode NOR Flash NAND Flash or NAND Interface ORNAND™ Flash on Bus 1 Mobile SDRAM on Bus 2

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S72WS-P_00 **Revision** A **Amendment** 4 **Issue Date** May 29, 2006

Notice On Data Sheet Designations

Spansion LLC issues data sheets with Advance Information or Preliminary designations to advise readers of product information or intended specifications throughout the product life cycle, including development, qualification, initial production, and full production. In all cases, however, readers are encouraged to verify that they have the latest information before finalizing their design. The following descriptions of Spansion data sheet designations are presented here to highlight their presence and definitions.

Advance Information

The Advance Information designation indicates that Spansion LLC is developing one or more specific products, but has not committed any design to production. Information presented in a document with this designation is likely to change, and in some cases, development on the product may discontinue. Spansion LLC therefore places the following conditions upon Advance Information content:

> "This document contains information on one or more products under development at Spansion LLC. The information is intended to help you evaluate this product. Do not design in this product without contacting the factory. Spansion LLC reserves the right to change or discontinue work on this proposed product without notice."

Preliminary

The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. The Preliminary status of this document indicates that product qualification has been completed, and that initial production has begun. Due to the phases of the manufacturing process that require maintaining efficiency and quality, this document may be revised by subsequent versions or modifications due to changes in technical specifications."

Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

> "This document states the current technical specifications regarding the Spansion product(s) described herein. Spansion LLC deems the products to have been in sufficient production volume such that subsequent versions of this document are not expected to change. However, typographical or specification corrections, or modifications to the valid combinations offered may occur."

Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

S72WS-P based MCP/PoP Products

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Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 1.7 to 1.95V**
- **Flash access time: 80 ns for NOR Flash, 25 ns for ORNAND Flash**
- **Flash burst frequencies: 66 MHz, 80 MHz, 108 MHz**
- **Mobile SDRAM burst frequency: 104 MHz (SDR), 133 MHz (DDR)**
- **Package:**
- **9.0 x 12.0 mm MCP**
- **11.0 x 13.0 mm MCP**
- **15.0 x 15.0 mm Package-on-Package (PoP)**
- **Operating Temperature**
- **–25°C to +85°C (wireless)**

The S72WS series is a product line of stacked packages and consists of:

- **One or two NOR flash memory die**
- **One NAND Interface ORNAND die**
- **Separate bus for one or more Mobile SDRAM die**

The products covered by this document are listed in the table below.

Device	NOR Flash Density			ORNAND™ Flash Density		NAND Flash Density	DRAM Density		
	512Mb	256Mb	128Mb	1024Mb	512Mb	512Mb	512Mb	256Mb	128Mb
S72WS256PD0 (MCP)		X							X (DDR)
S72WS256PD0 (POP)		X							X (DDR)
S72WS512PE0 (MCP)	X							X (SDR)	
S72WS512PEF (POP)	X					X		X (SDR)	
S72WS512PEF (POP)	X				X			X (SDR)	
S72WS512PFF (MCP)	X					X	X (DDR)		
S72WS512PFF (POP)	X					X	X (DDR)		
S72WS512PFF (MCP)	X				X		X (DDR)		
S72WS512PFF (POP)	X				X		X (DDR)		
S72WS512PFG (MCP)	X			X			X (DDR)		
S72WS512PFG (POP)	X			X			X (DDR)		

Note:
For a full list of OPNs, please contact the local sales representative or refer to the Ordering Information valid combinations tables.

For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29WS-P	S29WS-P_00
S30MS-P	S30MS-P_00
128 Mb Mobile DDR-DRAM Type 5	SDRAM_07
256 Mb Mobile SDR-DRAM Type 2	SDRAM_05
512 Mb Mobile DDR-DRAM Type 1	SDRAM_09
512 Mb Mobile SDR-DRAM Type 4	SDRAM_06
512 Mb NAND Type 1	NAND_01
512 Mb Mobile DDR-DRAM Type 5	DRAM_04

Publication Number S72WS-P_00 **Revision** A **Amendment** 4 **Issue Date** May 29, 2006

1. Product Selector Guide

1.1 NOR Flash + DRAM Products

Device	NOR Flash Density	NOR Flash Speed	DRAM Density	DRAM Speed	DRAM Supplier	Package
S72WS256PD0KFKLG	256 Mb	66 MHz	128 Mb	133 MHz (DDR)	Type 5	PoP 15 x 15 mm
S72WS256PD0HF6LG						MCP 9 x 12 mm
S72WS512PE0HF61R	512 Mb	80 MHz	256 Mb	104 MHz (SDR)	Type 2	MCP 9 x 12 mm

1.2 NOR Flash + ORNAND Flash + DRAM Products

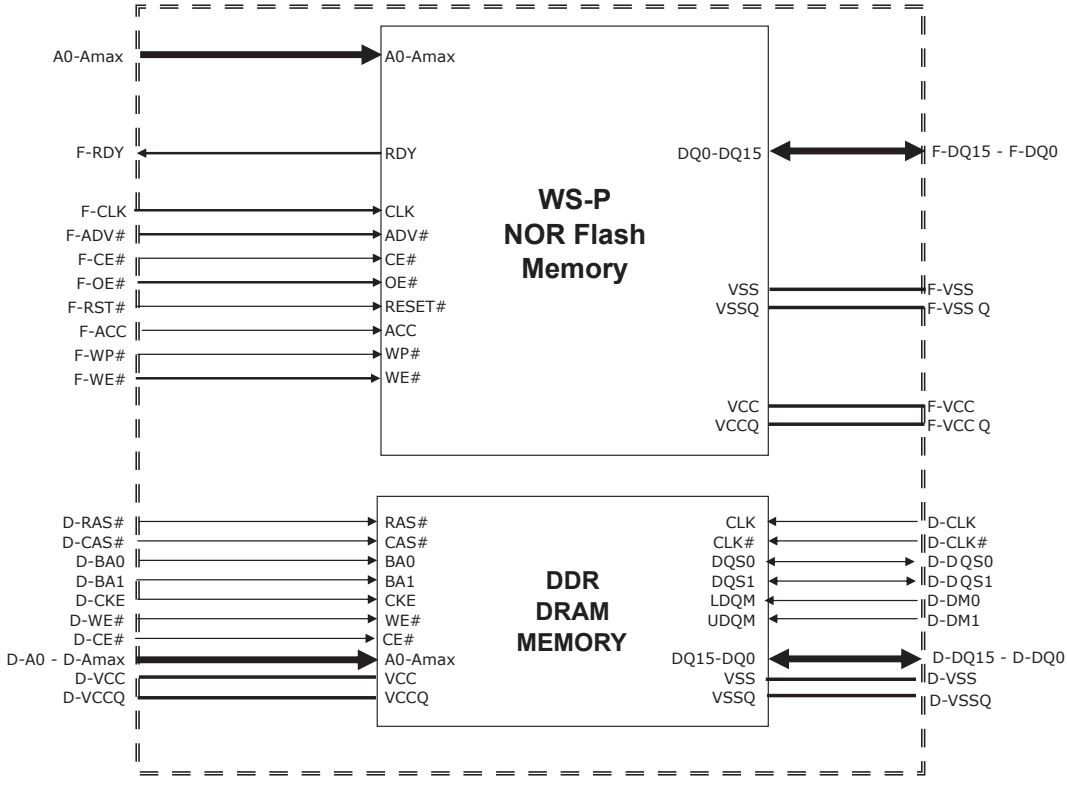
Device-Model#	NOR Flash Density	NOR Flash Speed	ORNAND Flash Density	ORNAND Bus Width	ECC Required	DRAM Density	DRAM Speed	DRAM Supplier	Package
S72WS512PEFKFKHH	512 Mb	66 MHz	512Mb	x16	Yes	256 Mb	133 MHz (DDR)	Type 2	PoP 15 x 15 mm 160-ball
S72WS512PFFKFKGH						512 Mb		Type 1	PoP 15 x 15 mm 160-ball
S72WS512PFFJF9GH									MCP 11 x 13 mm 137-ball
S72WS512PFGJF9GH			1024 Mb						MCP 11 x 13 mm 137-ball
S72WS512PFGKFKGH									PoP 15 x 15 mm 160-ball
S72WS512PFFJF9LD		80 MHz	512 Mb	x16	Yes			Type 5	MCP 11 x 13 mm 137-ball
S72WS512PFFKFKLD									PoP 15 x 15 mm 160-ball

1.3 NOR Flash + NAND Flash + DRAM Products

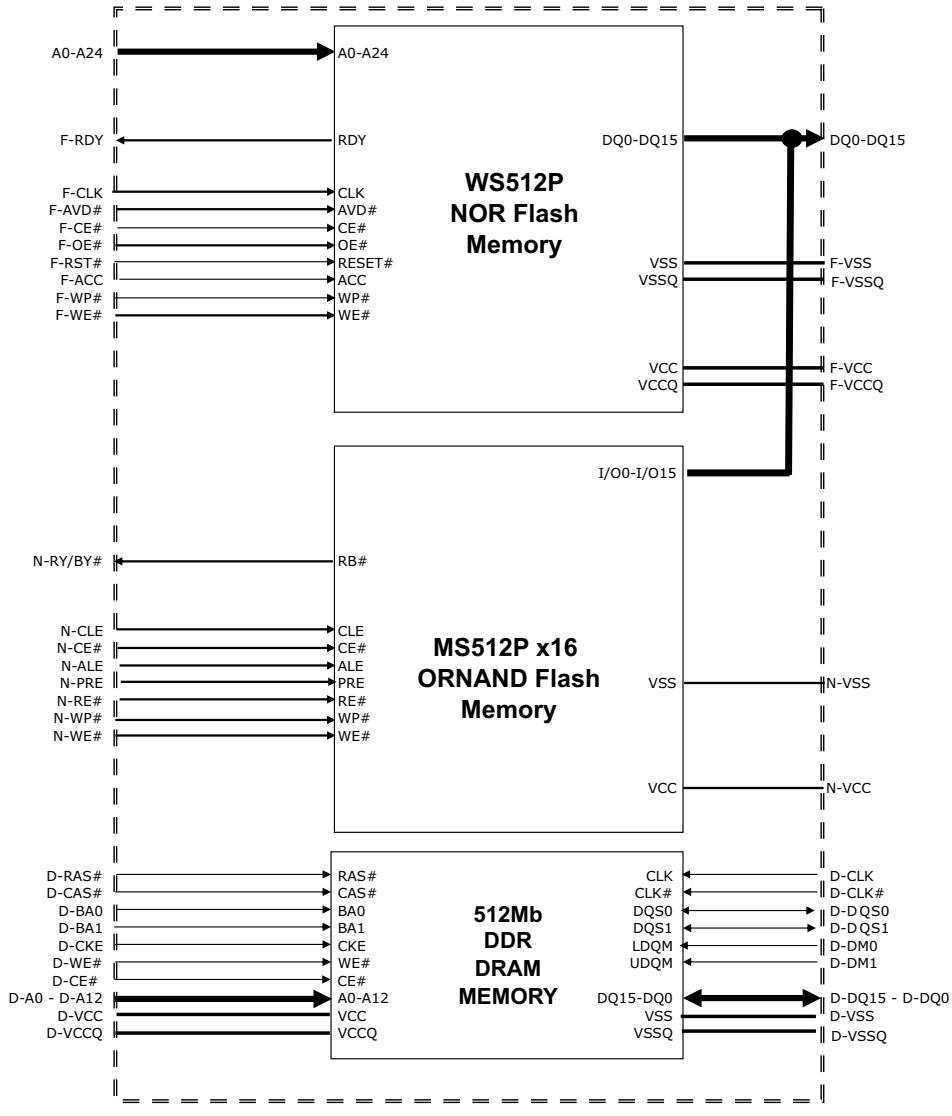
Device-Model#	NOR Flash Density	NOR Flash Speed	NAND Flash Density	NAND Bus Width	ECC Required	DRAM Density	DRAM Speed	DRAM Supplier	Package
S72WS512PEFKFKHJ	512Mb	66 MHz	512Mb	x16	Yes	256 Mb	133 MHz (DDR)	Type 2	PoP 15 x 15 mm 160-ball
S72WS512PFFKFKGJ						512 Mb		Type 1	PoP 15 x 15 mm 160-ball
S72WS512PFFJF9GJ									MCP 11 x 13 mm 137-ball
S72WS512PFFKFKLE		80 MHz						Type 5	PoP 15 x 15 mm 160-ball
S72WS512PFFJF9LE									MCP 11 x 13 mm 137-ball

2. MCP Block Diagram

2.1 NOR Flash + DRAM Products



2.2 NOR Flash + (OR)NAND Flash + DRAM Products



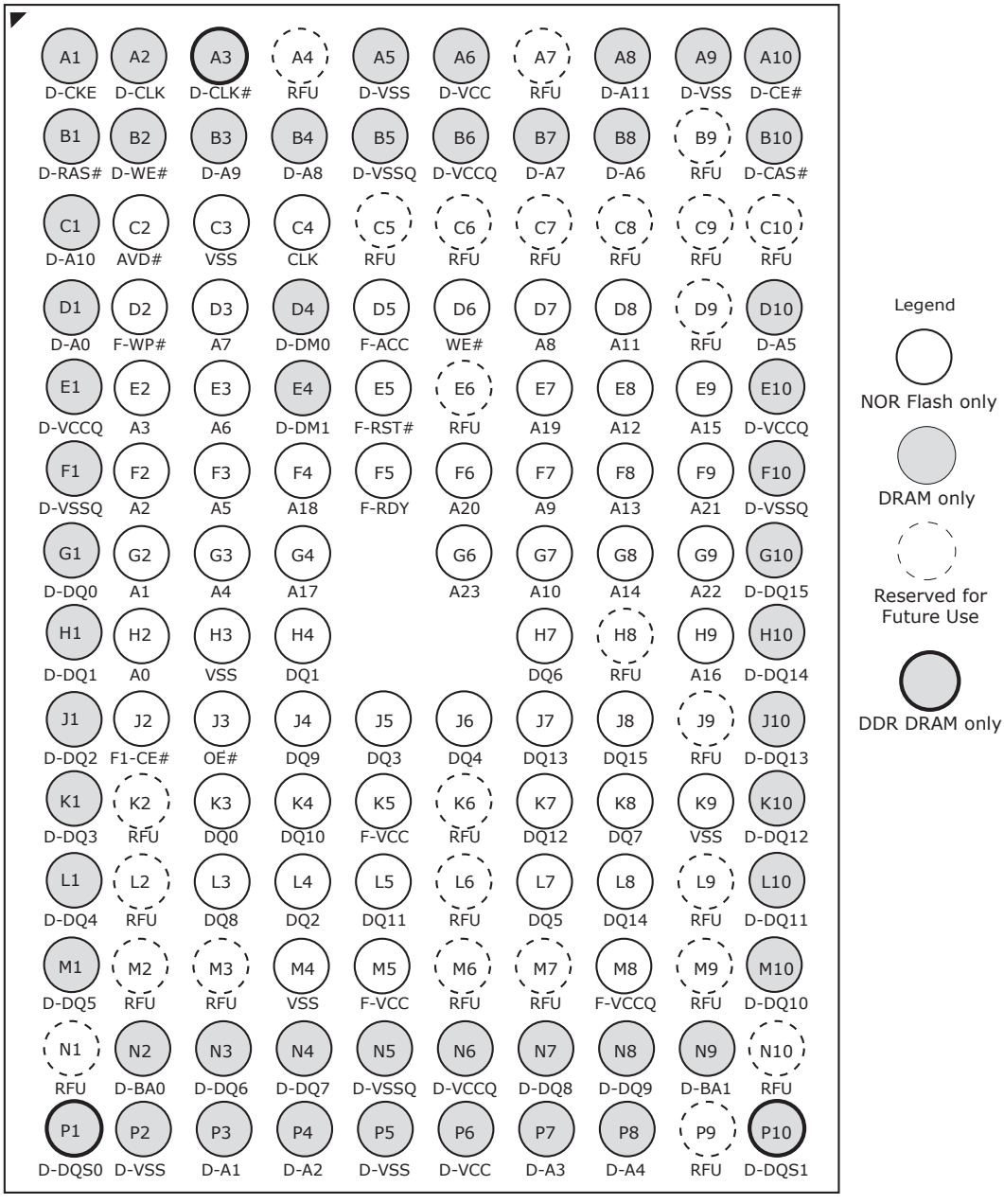
Note

1. *For MCPs, V_{SS} is shared between all Flash (NOR and ORNAND). Also, V_{SSQ} is tied to V_{SS} internally within the MCP.*

3. Connection Diagrams

3.1 256Mb NOR Flash with 128Mb SDR/DDR-DRAM

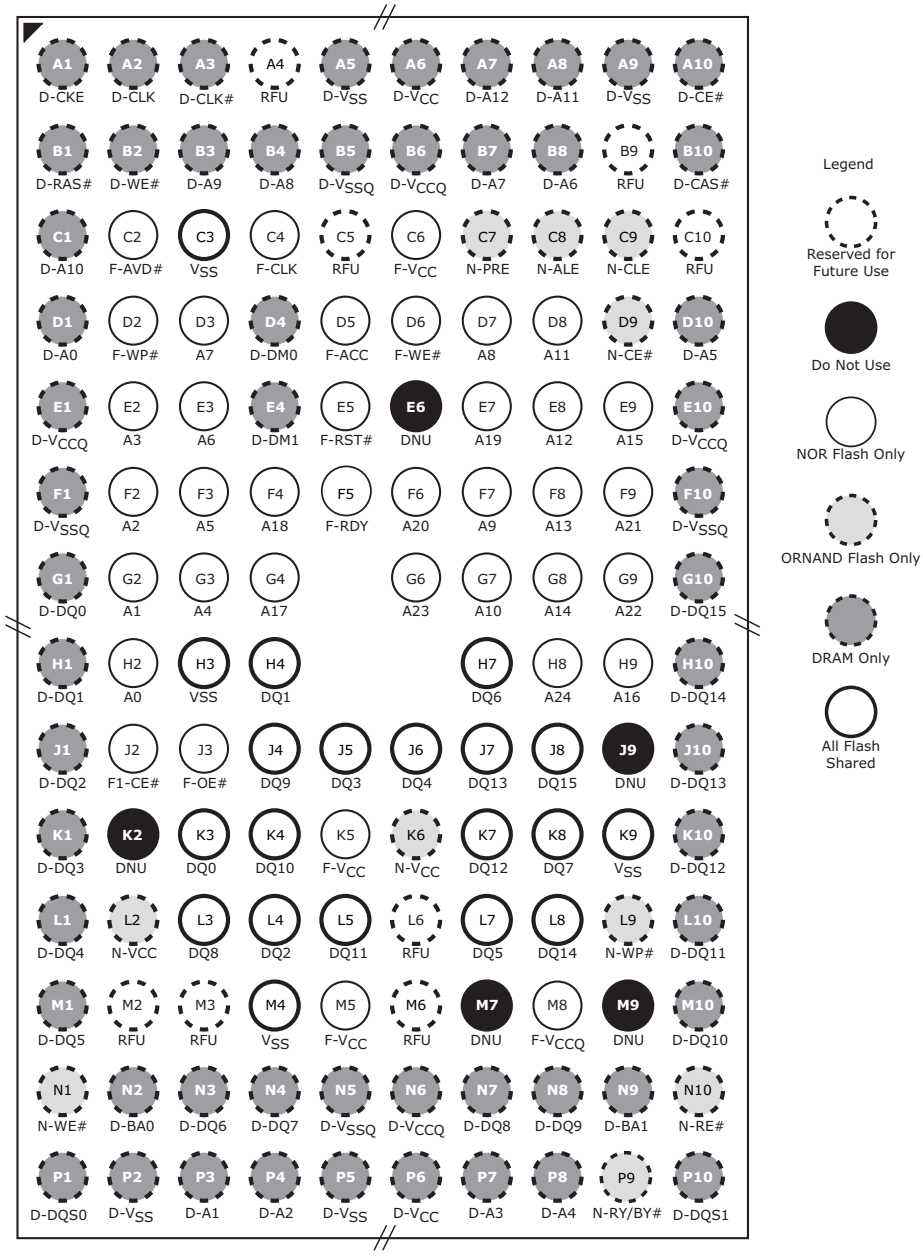
137-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



Note: DDR-only signals are RFUs in the case of the SDR DRAM-based solutions.

3.2 512Mb NOR Flash with 512-Mb (OR)NAND on Bus 1 and 512-Mb DRAM on Bus 2

137-ball Fine-Pitch Ball Grid Array
(Top View, Balls Facing Down)



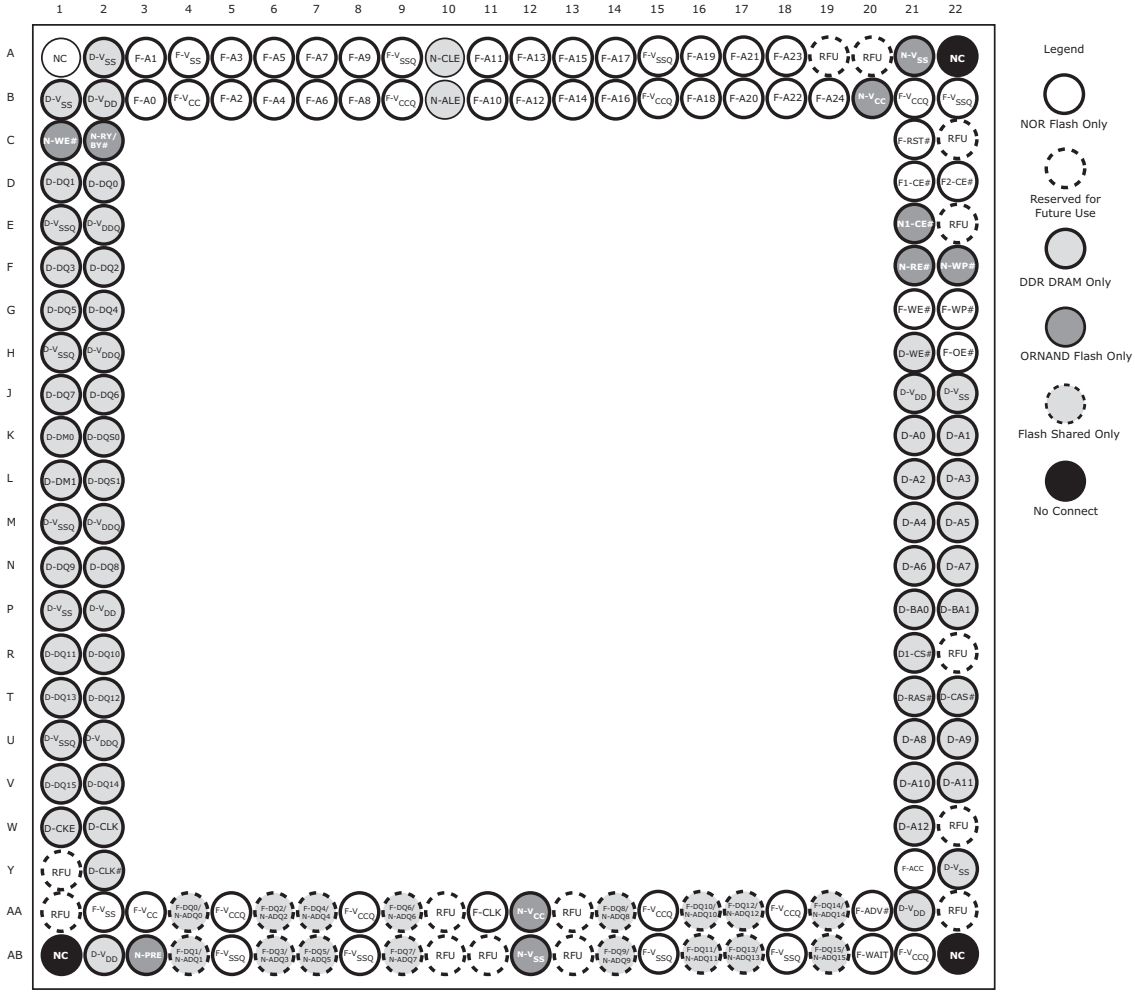
3.2.0.1 Special Handling Instructions For FBGA Package

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150×C for prolonged periods of time.

3.2.1 Package-on-Package Connection Diagram

160-ball Fine Pitch Ball Grid Array
(Top View, Balls Facing Down)



3.2.2 Look-ahead Ballout for Future Designs

Please refer to the Design-in Scalable Wireless Solutions with Spansion Products application note (publication number: Design_Scalable_Wireless_A0_E). Contact your local Spansion sales representative for more details.

3.3 NOR Flash and DRAM Input/Output Descriptions

Amax-A0	=	NOR Flash Address inputs
DQ15-DQ0	=	Flash Data input/output, shared between NOR and ORNAND Flash. DQ0-DQ7 shared for x8 ORNAND
F-CE#	=	NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.
F-OE#	=	NOR Flash Output Enable input. Asynchronous relative to CLK for Burst mode.
F-WE#	=	NOR Flash Write Enable input.
F-V_{CC}	=	NOR Flash device power supply (1.7 V - 1.95V).
F-V_{CCQ}	=	Input/Output Buffer power supply.
V_{SS}	=	Ground
RFU	=	Reserved for Future Use
F-RDY	=	Flash ready output. Indicates the status of the Burst read. VOL = data valid.
F-CLK	=	NOR Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
F-AVD#	=	NOR Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. VIL = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. VIH= device ignores address inputs
F-RST#	=	NOR Flash hardware reset input. VIL= device resets and returns to reading array data
F-WP#	=	NOR Flash hardware write protect input. VIL = disables program and erase functions in the four outermost sectors.
F-ACC	=	NOR Flash accelerated input. At VHH, accelerates programming; automatically places device in unlock bypass mode. At VIL, disables all program and erase functions. Should be at VIH for all other conditions.
D-Amax-D-A0	=	SDRAM Address inputs
D-DQ15-D-DQ0	=	SDRAM Data input/output
D-CLK	=	SDRAM System Clock
D-CE#	=	SDRAM Chip Select
D-CKE	=	SDRAM Clock Enable
D-BA1-BA0	=	SDRAM Bank Select
D-RAS#	=	SDRAM Row Address Strobe
D-CAS#	=	SDRAM Column Address Strobe
D-DM1-D-DM0	=	SDRAM Data Input/Output Mask
D-WE#	=	SDRAM Write Enable input
D-V_{SS}	=	SDRAM Ground
D-CLK#	=	DDR SDRAM Clock - in addition to D-CLK, this signal is available for DDRAMs that need CLK# for normal operations
D-V_{SSQ}	=	SDRAM Input/Output Buffer ground
D-V_{CCQ}	=	SDRAM Input/Output Buffer power supply
D-V_{CC}	=	SDRAM device power supply
D-DQS0 - D-DQS1	=	DDR SDRAM Data Strobe pins. DQS provides the read data strobes (as output) and the write data strobes (as input). Each DQS pin corresponds to eight DQ pins, respectively.

3.3.1 ORNAND Signal Descriptions

N-PRE	=	ORNAND Power-On Read Enable. Tie to V_{SS} on customer board if not used
N-ALE	=	ORNAND Address Latch Enable
N-CLE	=	ORNAND Command Latch Enable
N-CE#	=	ORNAND Chip-enablE
N-WP#	=	ORNAND Write-protect
N-WE#	=	ORNAND Write-enable
N-RE#	=	ORNAND Read-enable
N-RY/BY#	=	ORNAND Ready-Busy
N-I/O0-N-I/O15	=	ORNAND I/O Signals (I/O0-I/O7 for x8 bus width)
N-V_{CC}	=	ORNAND Power Supply

4. Ordering Information

The order number is formed by a valid combinations of the following:

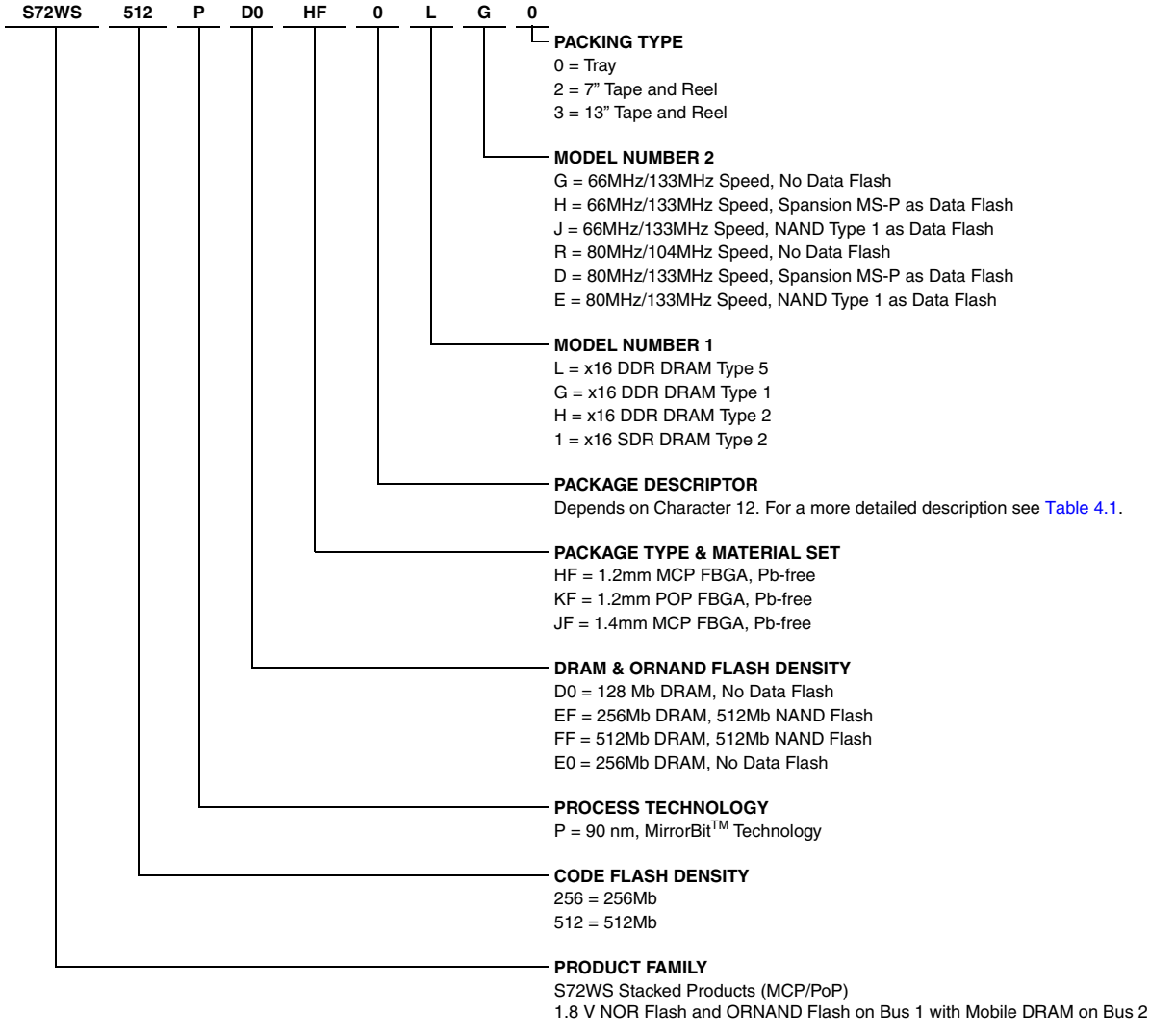


Table 4.1 Character Position Descriptions (Sheet 1 of 2)

Character 12	Character 13	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
H, J, or G	0	7x9 mm	56	0.35 mm
	1	7x9 mm	80	
	2	8x11.6 mm	64	
	3	8x11.6 mm	84	
	4	9x12 mm	84	
	5	9x12 mm	115	
	6	9x12 mm	137	
	7	11x13 mm	84	
	8	11x13 mm	115	
	9	11x13 mm	137	

Table 4.1 Character Position Descriptions (Sheet 2 of 2)

Character 12	Character 13	Character 14 Description		
		Package Area	Package Ball Count	Raw Ball Size
K	A	11x11 mm	112	0.45 mm
	B	11x11 mm	112	0.50 mm
	D	12x12 mm	128	0.45 mm
	F	12x12 mm	128	0.50 mm
	G	14x14 mm	152	0.45 mm
	H	14x14 mm	152	0.50 mm
	J	15x15 mm	160	0.45 mm
	K	15x15 mm	160	0.50 mm
	L	17x17 mm	192	0.45 mm
	M	17x17 mm	192	0.50 mm

4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

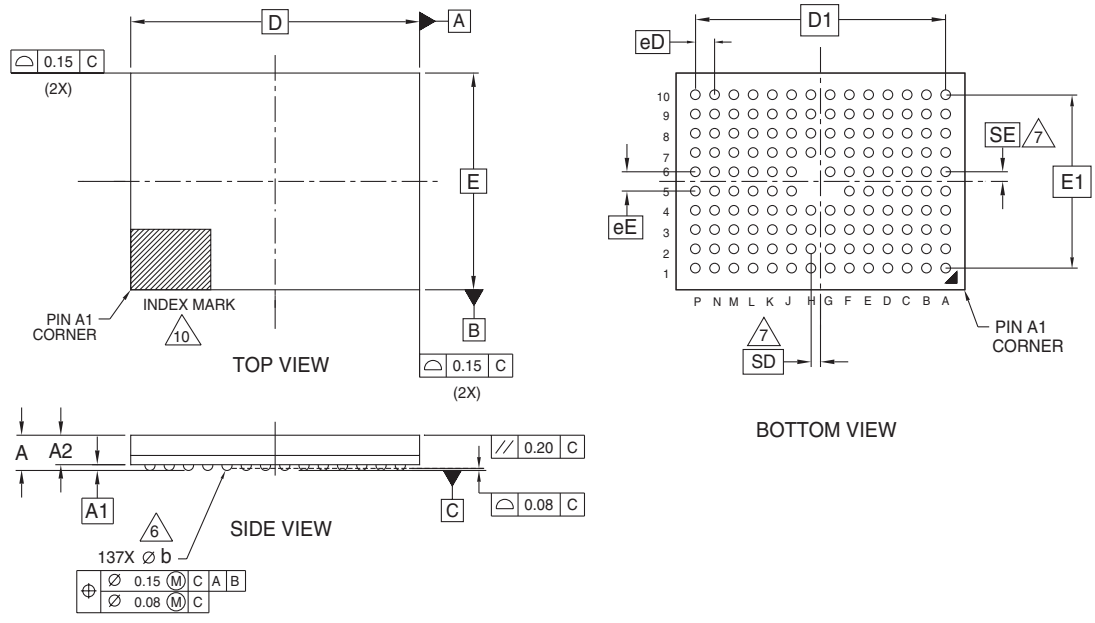
S72WS-P Valid Combinations				NOR Flash Speed	DRAM Supplier	DRAM Speed	Package Type	Package Markings
Base Ordering Number	Package & Material Set	Package Descriptor	Packing Type					
S72WS256PD0	KF	K	0, 2, 3 (Note 1)	66 MHz	Type 5	133 MHz	15x15 mm (PoP)	(Note 2)
	HF	6					9x12 mm (MCP)	
S72WS512PE0	HF	6		80 MHz	Type 2	104 MHz	9x12 mm (MCP)	
S72WS512PEF	KF	K		66 MHz	Type 2	133 MHz	15x15 mm (PoP)	
S72WS512PFF	HF	6		66 MHz	Type 1	133 MHz	15x15 mm (PoP)	
	JF	9		66 MHz	Type 1		11x13 mm (MCP)	
				80 MHz	Type 5			
	KF	K		66 MHz	Type 1		15x15 mm (PoP)	
				80 MHz	Type 5			
S72WS512PFG	JF	9		66 MHz	Type 1	133 MHz	11x13 mm (MCP)	
	KF	K					15x15 mm (PoP)	

Notes:

1. *Packing Type 0 is standard. Specify other options as required.*
2. *BGA package marking omits leading* S *and packing type designator from ordering part number.*

5. Physical Dimensions

5.1 TLD137—137-ball Fine-Pitch Ball Grid Array (FBGA) 12 x 9 mm Package



PACKAGE	TLD 137			
JEDEC	N/A			
D x E	12.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D		12.00 BSC.		BODY SIZE
E		9.00 BSC.		BODY SIZE
D1		10.40 BSC.		MATRIX FOOTPRINT
E1		7.20 BSC.		MATRIX FOOTPRINT
MD		14		MATRIX SIZE D DIRECTION
ME		10		MATRIX SIZE E DIRECTION
n		137		BALL COUNT
ϕb	0.35	0.40	0.45	BALL DIAMETER
eE		0.80 BSC.		BALL PITCH
eD		0.80 BSC		BALL PITCH
SD / SE		0.40 BSC.		SOLDER BALL PLACEMENT
		G5,H5,H6		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. N/A
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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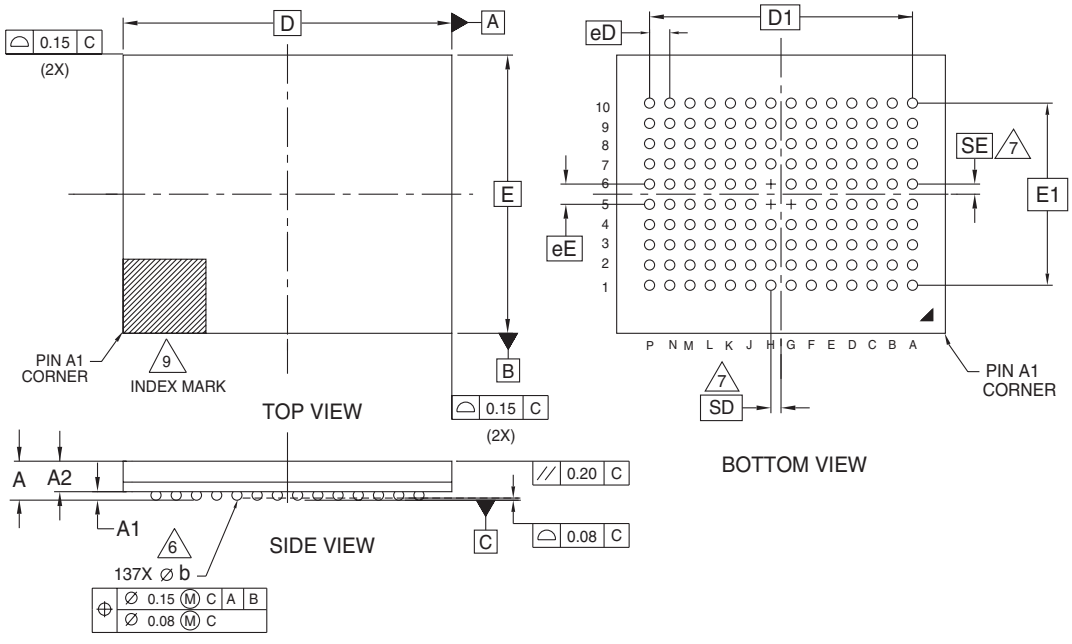
5.2 FVD137—137-ball Fine-Pitch Ball Grid Array (FBGA) 13 x 11 mm Package



PACKAGE	FVD 137			NOTE
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.10	---	---	BALL HEIGHT
A2	1.09	---	1.24	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	10.40 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	137			BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD SE	0.40 BSC.			SOLDER BALL PLACEMENT
	G5,H5,H6			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

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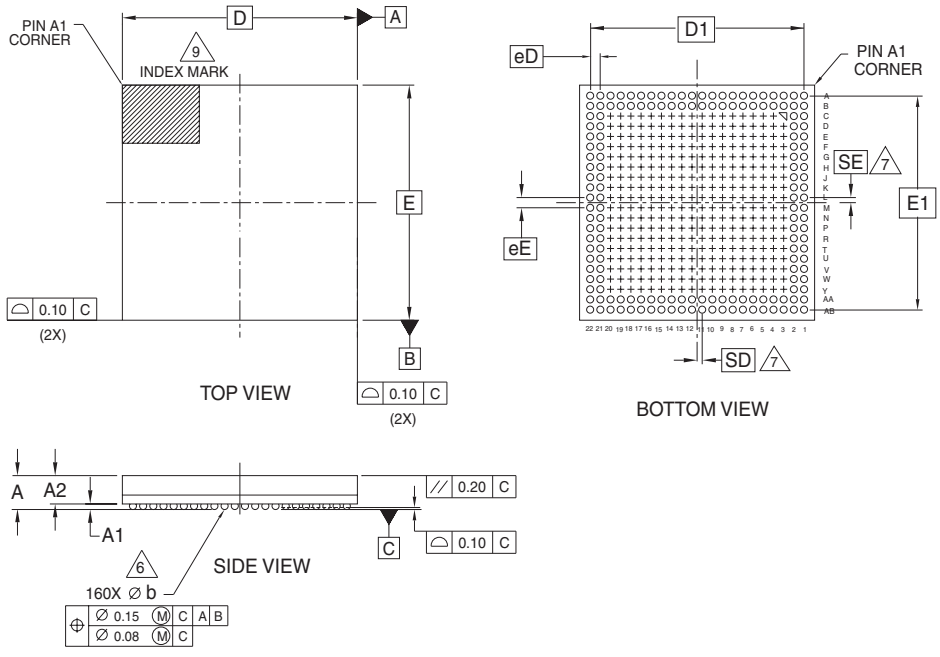
5.3 BWB160—160-ball Fine-Pitch Ball Grid Array (FBGA) 15 x 15 mm Package



PACKAGE	BWB 160			NOTE
JEDEC	N/A			
D x E	15.00 mm x 15.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.30	PROFILE
A1	0.40	---	---	BALL HEIGHT
A2	0.74	---	0.84	BODY THICKNESS
D		15.00 BSC.		BODY SIZE
E		15.00 BSC.		BODY SIZE
D1		13.65 BSC.		MATRIX FOOTPRINT
E1		13.65 BSC.		MATRIX FOOTPRINT
MD		22		MATRIX SIZE D DIRECTION
ME		22		MATRIX SIZE E DIRECTION
n		160		BALL COUNT
N		160		MAXIMUM NUMBER OF BALLS
R		2		NUMBER OF LAND PARAMETERS
Øb	0.45	0.50	0.55	BALL DIAMETER
eE		0.65 BSC.		BALL PITCH
eD		0.65 BSC.		BALL PITCH
SD / SE		0.325 BSC.		SOLDER BALL PLACEMENT
?	C3~C20,D3~D20,E3~E20,F3~F20 G3~G20,H3~H20,J3~J20,K3~K20 L3~L20,M3~M20,N3~N20,P3~P20 R3~R20,T3~T20,U3~U20,V3~V20 W3~W20,Y3~Y20			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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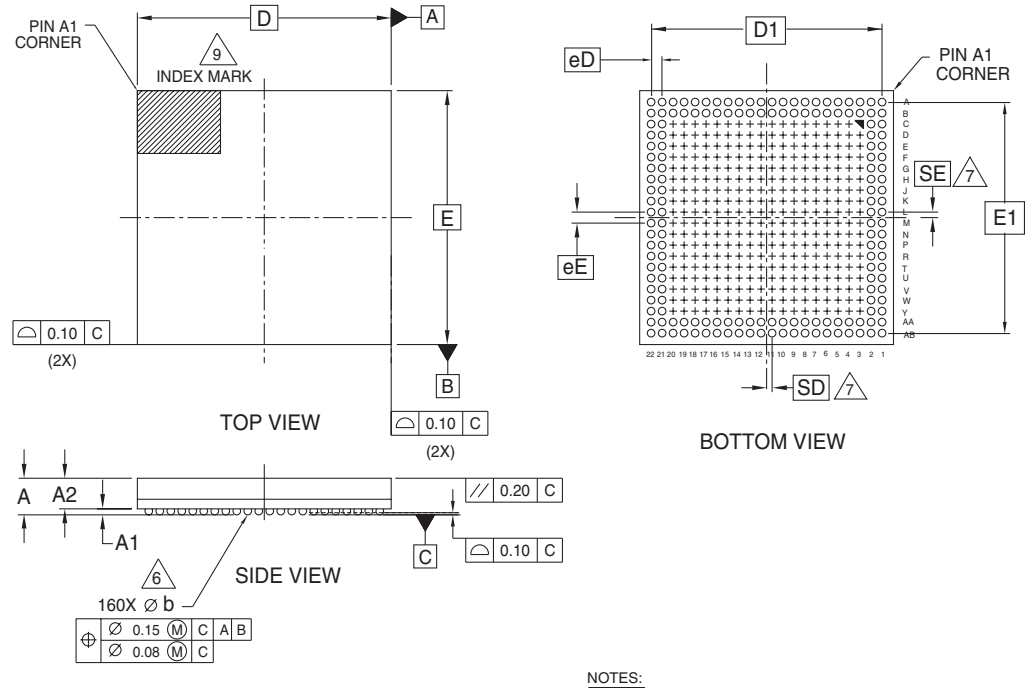
5.4 BTA160—160-ball Fine-Pitch Ball Grid Array (FBGA) 15 x 15 mm Package



PACKAGE	BTA 160			NOTE
JEDEC	N/A			
D x E	15.00 mm x 15.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.30	PROFILE
A1	0.40	---	---	BALL HEIGHT
A2	0.74	---	0.84	BODY THICKNESS
D	15.00 BSC.			BODY SIZE
E	15.00 BSC.			BODY SIZE
D1	13.65 BSC.			MATRIX FOOTPRINT
E1	13.65 BSC.			MATRIX FOOTPRINT
MD	22			MATRIX SIZE D DIRECTION
ME	22			MATRIX SIZE E DIRECTION
n	160			BALL COUNT
N	160			MAXIMUM NUMBER OF BALLS
R	2			NUMBER OF LAND PARAMETERS
Ø b	0.45	0.50	0.55	BALL DIAMETER
eE	0.65 BSC.			BALL PITCH
eD	0.65 BSC.			BALL PITCH
SD SE	0.325 BSC.			SOLDER BALL PLACEMENT
	C3~C20,D3~D20,E3~E20,F3~F20 G3~G20,H3~H20,J3~J20,K3~K20 L3~L20,M3~M20,N3~N20,P3~P20 R3~R20,T3~T20,U3~U20,V3~V20 W3~W20,Y3~Y20			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

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6. Revision History

6.1 Revision A1 (February 23, 2006)

Initial release.

6.2 Revision A2 (March 29, 2006)

Modified Block Diagram for Section 2.1 and Section 2.2 2.

Updated PoP Connection Diagram in Section 3.2.2 3.

Updated Section 3.3 to append F-RDY and N-RY/BY# as separate signals

6.3 Revision A3 (April 11, 2006)

Added a note to the NOR Flash + (OR)NAND Flash + DRAM Products block diagram

Updated pin M8 on the 256Mb NOR Flash with 128Mb SDR/DDR-DRAM connection diagram

6.4 Revision A4 (May 29, 2006)

Added OPNs for products based on DRAM Type 5

Updated Product Selector Guide

Updated Ordering Information

Updated Valid Combinations

Colophon

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