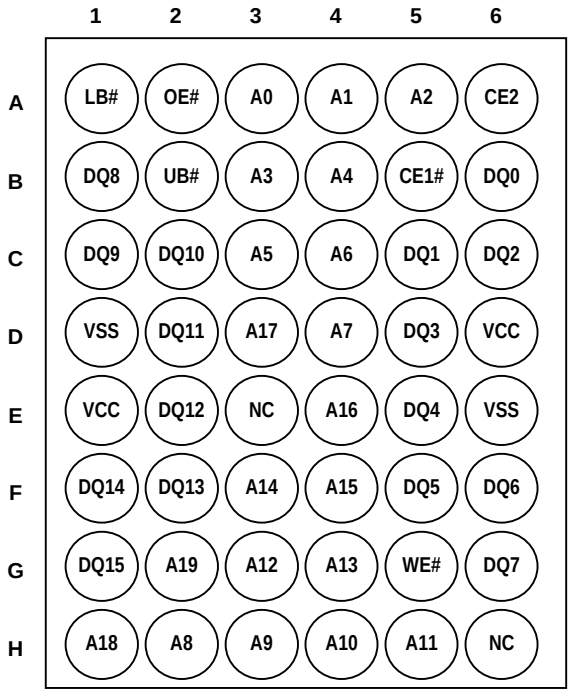
1M x 16 Pseudo SRAM

Preliminary, Rev 0.2 Apr. 2002

Features

- Organized as 1M words by 16 bits
- Fast Cycle Time : 70ns
- Standby Current : 100uA
- Deep power-down Current : 10uA (Memory cell data invalid)
- Byte data control: LB# (DQ0 - 7), UB# (DQ8 - 15)
- Compatible with low power SRAM
- Single Power Supply Voltage : 3.0V±0.3V
- Package Type : 48-ball FBGA, 6x8mm

Pin Assignment 48-Ball BGA, Top View



Pin Description

Symbol	Function
A0 – A19	Address Inputs
DQ0 – DQ15	Data Inputs/Outputs
CE1#	Chip Enable
CE2	Deep Power Down
OE#	Output Enable
WE#	Write Control
LB#	Lower Byte Control
UB#	Upper Byte Control
V_{CC}	Power Supply
V_{SS}	Ground

Overview

The EM566168 is a 16M-bit Pseudo SRAM organized as 1M words by 16 bits. It is designed with advanced CMOS technology specified RAM featuring low power static RAM compatible function and pin configuration. This device operates from a single power supply. Advanced circuit technology provides both high speed and low power. It is automatically placed in low-power mode when CS1# or both UB# and LB# are asserted high or CS2 is asserted low. There are three control inputs. CS1# and CS2 are used to select the device, and output enable (OE#) provides fast memory access. Data byte control pins (LB#,UB#) provide lower and upper byte access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed wide operating range, the EM566168 can be used in environments exhibiting extreme temperature conditions.

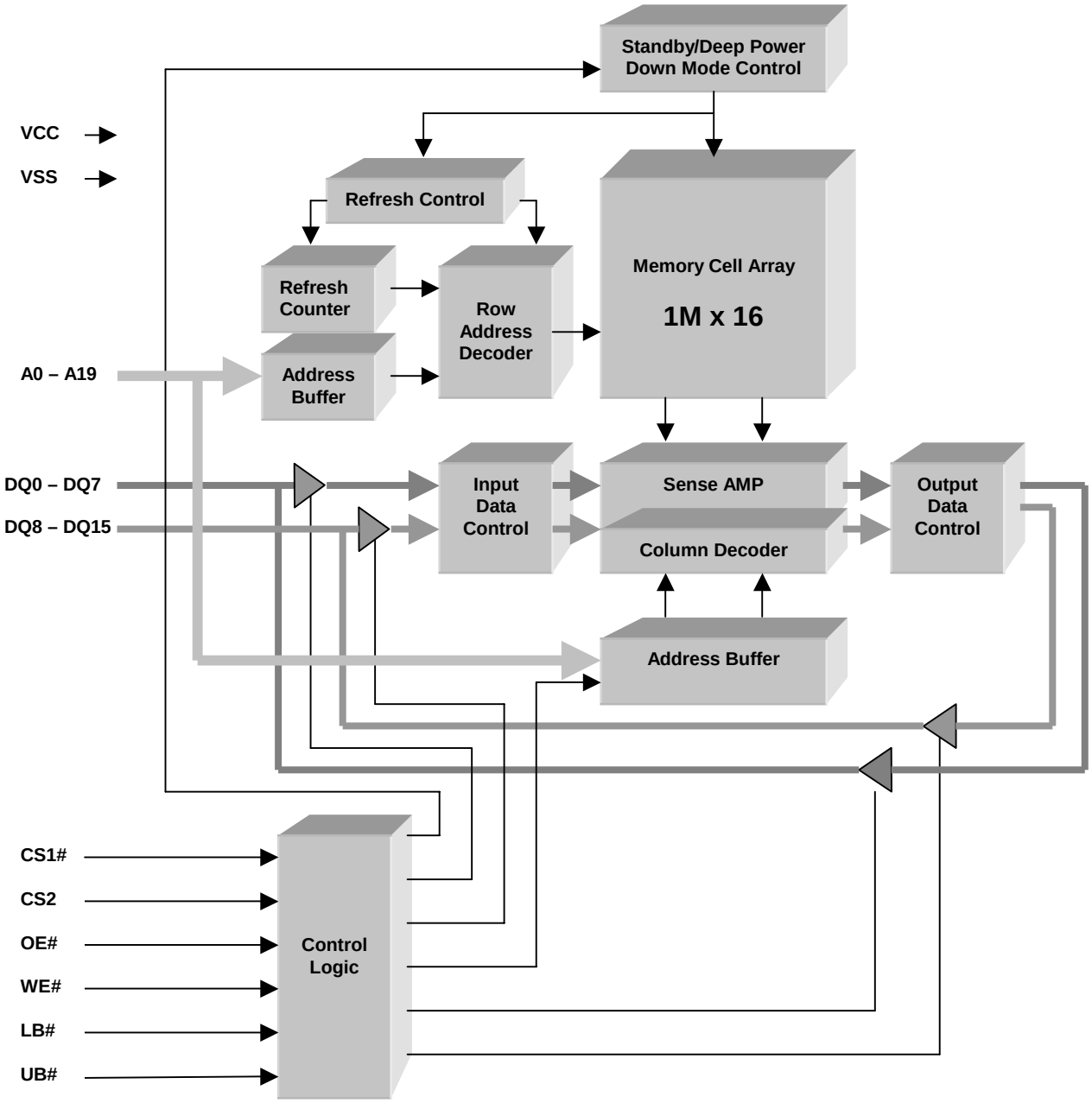
Pin Location

Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location	Symbol	Location
A0	A3	A8	H2	A16	E4	DQ3	D5	DQ11	D2	WE#	G5
A1	A4	A9	H3	A17	D3	DQ4	E5	DQ12	E2	LB#	A1
A2	A5	A10	H4	A18	H1	DQ5	F5	DQ13	F2	UB#	B2
A3	B3	A11	H5	A19	G2	DQ6	F6	DQ14	F1	VCC	D6
A4	B4	A12	G3	NC	H6	DQ7	G6	DQ15	G1	VCC	E1
A5	C3	A13	G4	DQ0	B6	DQ8	B1	CE1#	B5	GND	D1
A6	C4	A14	F3	DQ1	C5	DQ9	C1	CE2	A6	GND	E6
A7	D4	A15	F4	DQ2	C6	DQ10	C2	OE#	A2	NC	E3

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Block Diagram



Operating Mode

CS1#	CS2	OE#	WE#	LB#	UB#	DQ0~DQ7	DQ8~DQ15	Mode	Power
H	H	X	X	X	X	High-Z	High-Z	Deselect	Standby
X	L	X	X	X	X	High-Z	High-Z	Deselect	Deep Power Down
L	H	X	X	H	H	High-Z	High-Z	Deselect	Standby
L	H	H	H	L	X	High-Z	High-Z	Output Disabled	Active
L	H	H	H	X	L	High-Z	High-Z	Output Disabled	Active
L	H	L	H	L	H	D-out	High-Z	Lower Byte Read	Active
L	H	L	H	H	L	High-Z	D-out	Upper Byte Read	Active
L	H	L	H	L	L	D-out	D-out	Word Read	Active
L	H	X	L	L	H	D-in	High-Z	Lower Byte Write	Active
L	H	X	L	H	L	High-Z	D-in	Upper Byte Write	Active
L	H	X	L	L	L	D-in	D-in	Word Write	Active

Note: X=don't care. H=logic high. L=logic low.

Absolute Maximum Ratings[1)]

Supply voltage, V_{CC}	-0.2 to +3.6V
Input voltages, V_{IN}	-0.2 to VCC + 0.3V
Input and output voltages, V_{IN}, V_{OUT}	-2.0 to +3.6V*
Output short circuit current I_{SH}	100 mA
Operating temperature, T_A	-25 to +85°C
Storage temperature, T_{STRG}	-65 to +125°C
Soldering Temperature (10s), T_{SOLDER}	240°C
Power dissipation, P_D	1 W

Note: Absolute maximum DC requirements contains stress ratings only. Functional operation at the absolute maximum limits is not implied or guaranteed. Extended exposure to maximum ratings may affect device reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage	2.7	3.0	3.3	V
V_{SS}	Ground	0	–	0	V
V_{IH}	Input High Voltage	2.2	–	V_{CC}+0.2[1)]	V
V_{IL}	Input Low Voltage	-0.2[2)]	–	+0.6	V

Notes:

1. Overshoot: VCC + 2.0V in case of pulse width ≤ 20ns
2. Undershoot: -2.0V in case of pulse width ≤ 20ns
3. Overshoot and undershoot are sampled, not 100% tested.

DC Characteristics

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{DD}	-1	1	µA
I_{LO}	Output Leakage Current	$V_{IO} = V_{SS}$ to V_{DD} CE1# = V_{IH}, CE2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL}	-1	1	µA
I_{CC1}	Operating Current @ Min Cycle Time	Cycle time = Min., 100% duty I_{IO} = 0mA, CE1# = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL}	–	25	mA
I_{CC2}	Operating Current @ Max Cycle Time (1µs)	Cycle time = 1µs, 100% duty I_{IO} = 0mA, CE1# ≤ 0.2V, CE2 ≥ V_{DD} -0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{DD} -0.2V	–	3	mA
I_{SB1}	Standby Current (CMOS)	CE1# = V_{DD} – 0.2V and CE2 = V_{DD} – 0.2V, Other inputs = V_{SS} ~ V_{CC}	–	100	µA
I_{SBD}	Deep Power Down	CE2 ≤ 0.2V, Other inputs = V_{SS} ~ V_{CC}		10	µA
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -1.0mA	2.4	–	V

Capacitance (Ta = 25°C; f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C_{IN}	–	–	8	pF	V_{IN} = GND
Output capacitance	C_{OUT}	–	–	10	pF	V_{OUT} = GND

Notes: These parameters are sampled and not 100% tested.

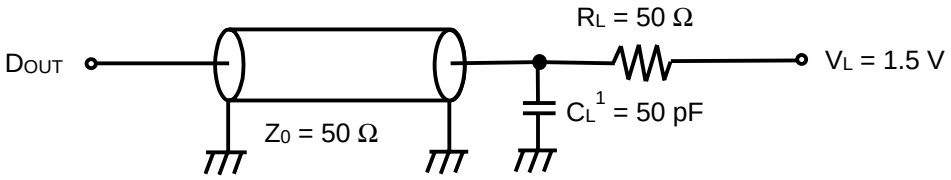
AC Characteristics and Operating Conditions (Ta = -25°C to 85°C, V_{CC} = 2.7V to 3.3V)

Symbol	Parameter	-85		-70		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{RC}	Read cycle time	85	–	70	–	ns
t_{AA}	Address access time	–	85	–	70	ns
t_{CO1}	Chip Enable (CE1#) Access Time	–	85	–	70	ns
t_{CO2}	Chip Enable (CE2) Access Time	–	85	–	70	ns
t_{OE}	Output enable access time	–	40	–	35	ns
t_{BA}	Data Byte Control Access Time	–	85	–	70	ns
t_{LZ}	Chip Enable Low to Output in Low-Z	10	–	10	–	ns
t_{OLZ}	Output enable Low to Output in Low-Z	5	–	5	–	ns
t_{BLZ}	Data Byte Control Low to Output in Low-Z	10	–	10	–	ns
t_{HZ}	Chip Enable High to Output in High-Z	–	35	–	25	ns
t_{OHZ}	Output Enable High to Output in High-Z	–	35	–	25	ns
t_{BHZ}	Data Byte Control High to Output in High-Z	–	35	–	25	ns
t_{OH}	Output Data Hold Time	10	–	10	–	ns
Write Cycle						
t_{WC}	Write Cycle Time	85	–	70	–	ns
t_{WP}	Write Pulse Width	60	–	50	–	ns
t_{AW}	Address Valid to End of Write	70	–	60	–	ns
t_{CW}	Chip Enable to End of Write	70	–	60	–	ns
t_{BW}	Data Byte Control to End of Write	70	–	60	–	ns
t_{AS}	Address Setup Ttime	0	–	0	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	ns
t_{WHZ}	WE# Low to Output in High-Z	–	30	–	20	ns
t_{OW}	WE# High to Output in Low-Z	5	–	5	–	ns
t_{DW}	Data to Write Overlap	30	–	30	–	ns
t_{DH}	Data Hold Time	0	–	0	–	ns

AC Test Condition

- Output load : 50pF + one TTL gate
- Input pulse level : 0.4V, 2.4
- Timing measurements : 0.5 x V_{CC}
- tR, tF : 5ns

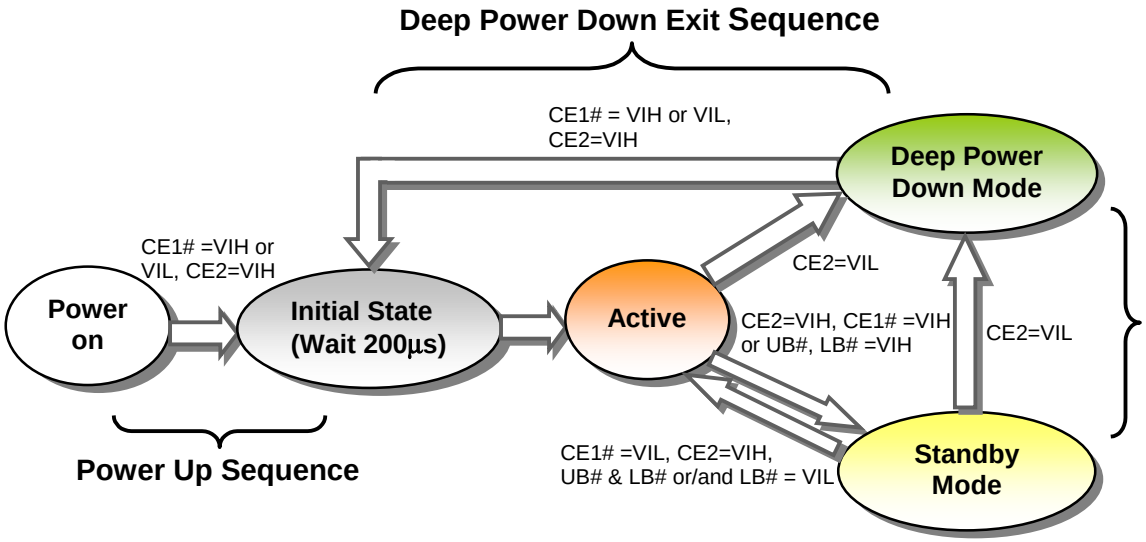
AC Test Loads



Note:

1. Including scope and jig capacitance

State Diagram

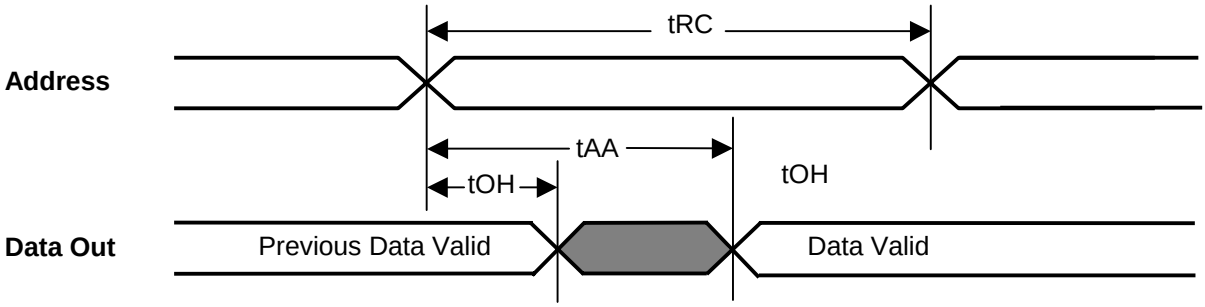


Standby Mode Characteristics

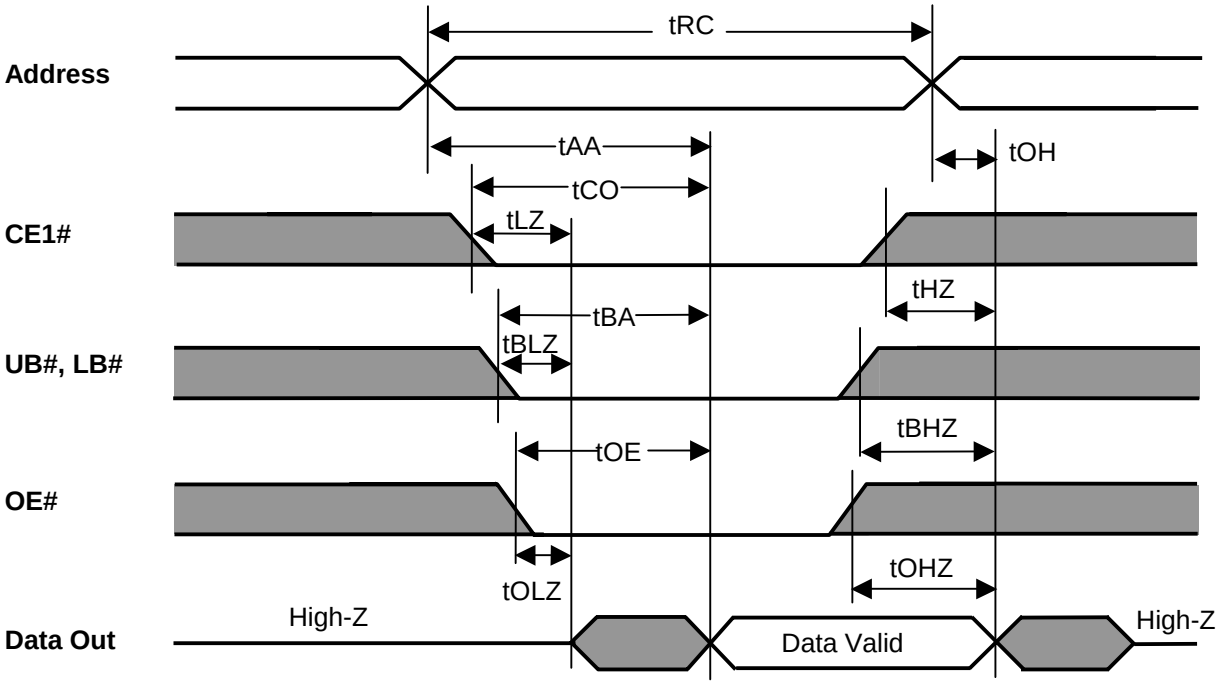
Power Mode	Memory Cell Data	Standby Current (µA)	Wait Time (µs)
Standby	Valid	100	0
Deep Power Down	Invalid	10	200

Timing Diagrams

Read Cycle 1 – Addressed Controlled[1)]



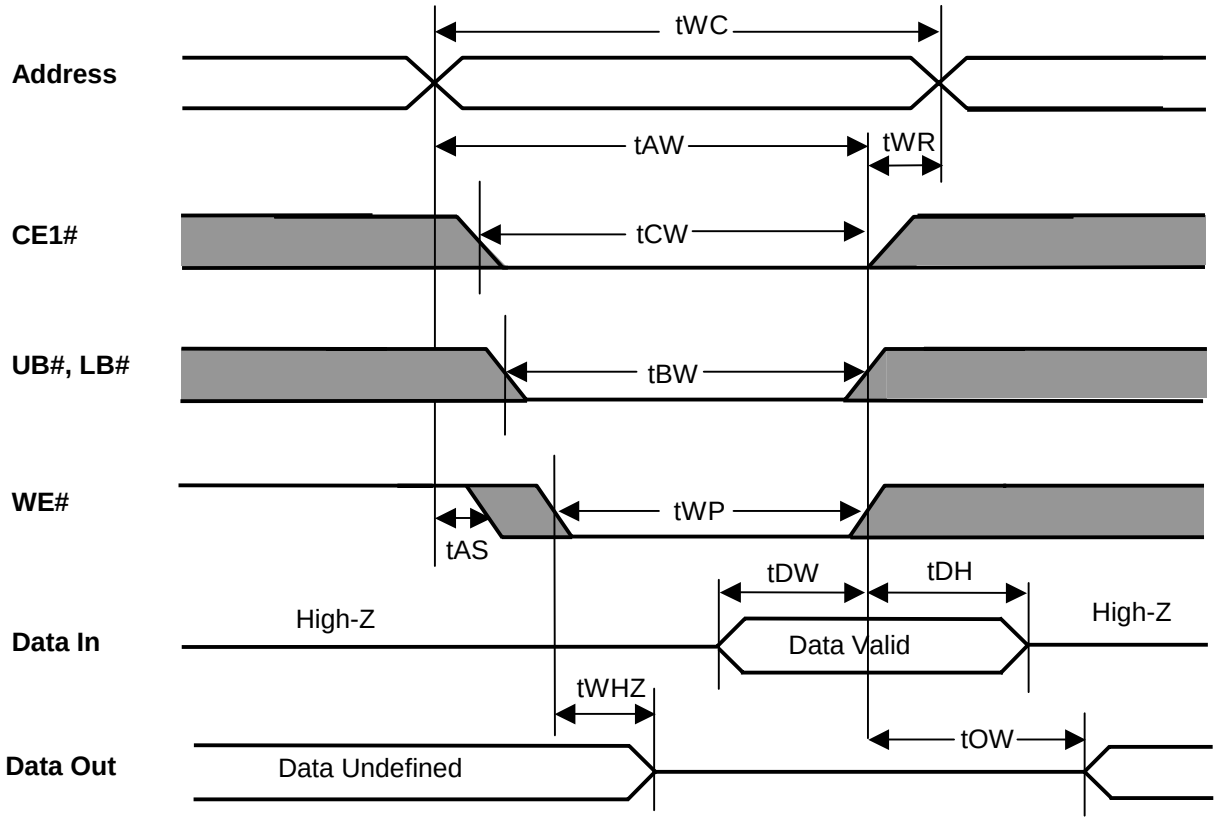
Read Cycle 2 – CS1# Controlled[2)]



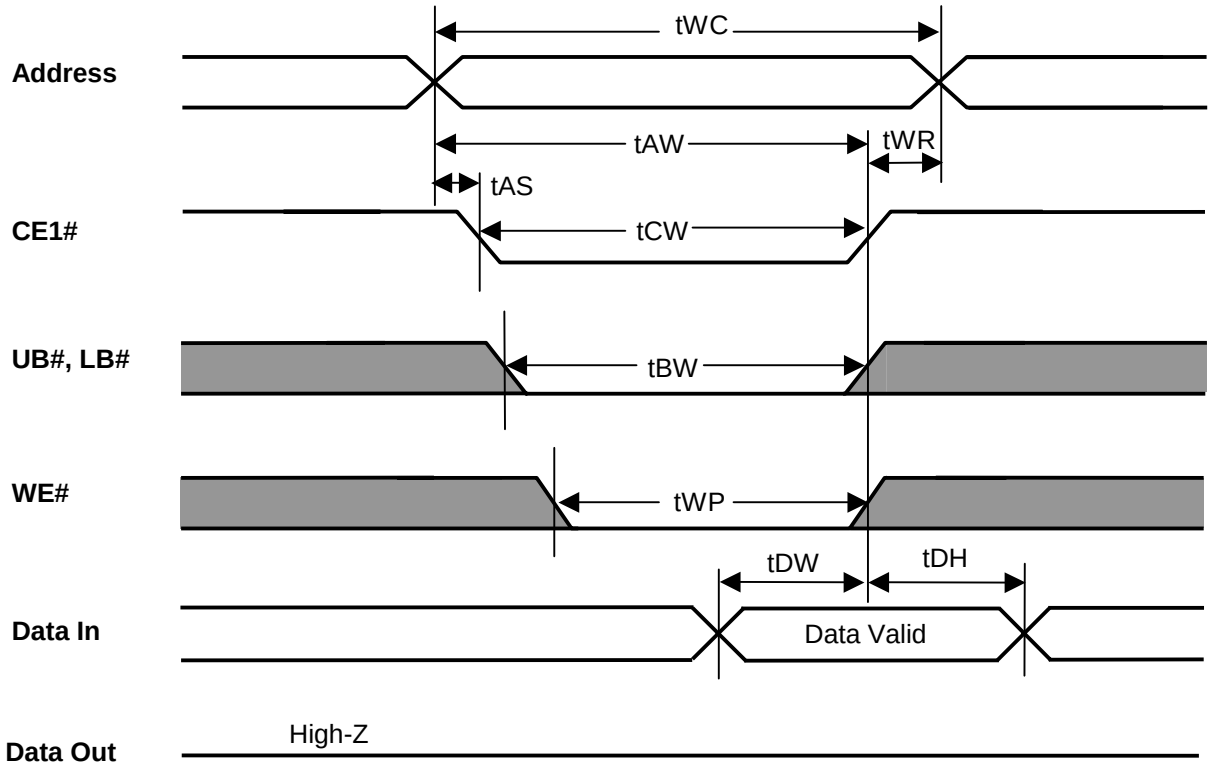
Notes:

1. CE1# = OE# = V_{IL}, CE2 = WE# = V_{IH}, UB# or/and LB# = V_{IL}
2. CE2 = WE# = V_{IH}

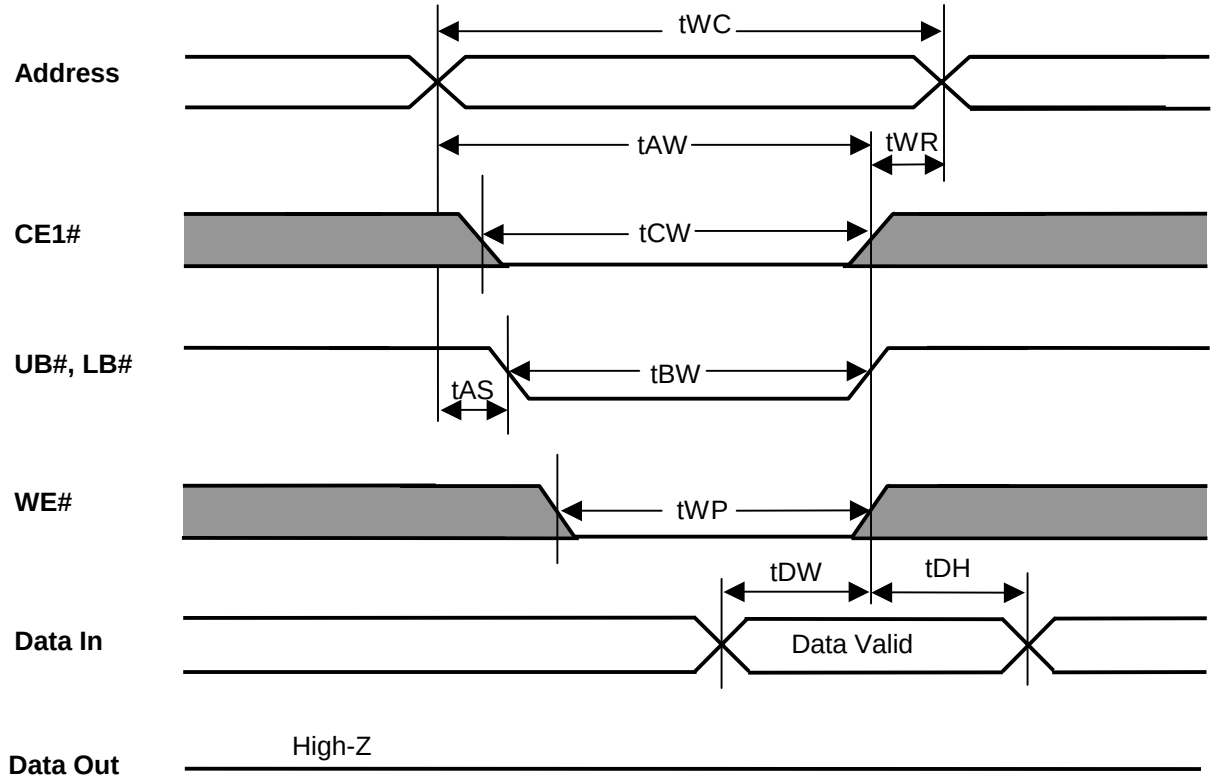
Write Cycle 1 – WE# Controlled[1) 2)]



Write Cycle 2 – CS1# Controlled[1) 2)]



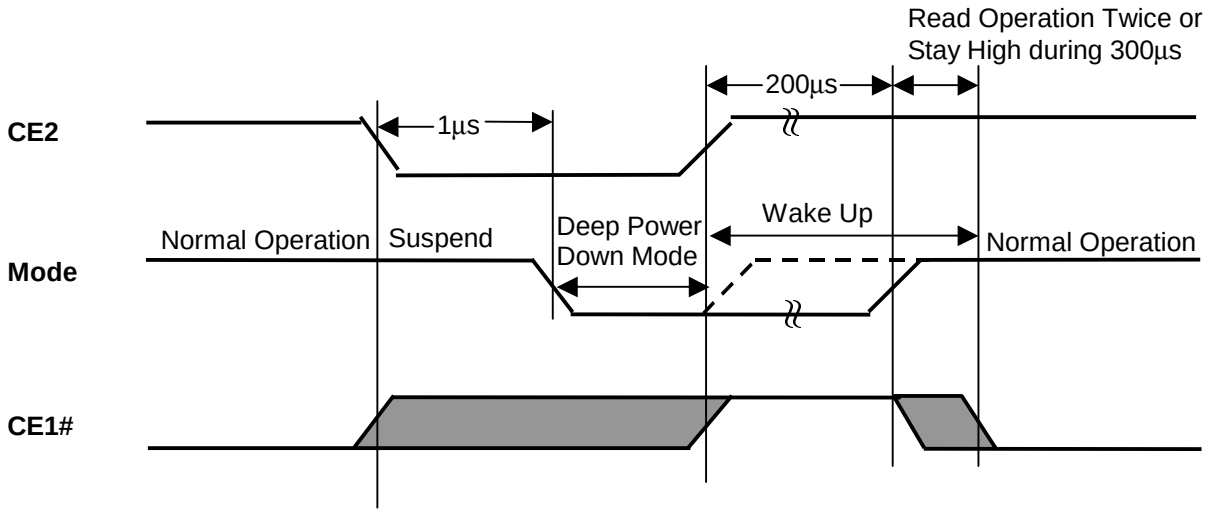
Write Cycle 3 – UB#, LB# Controlled[1) 2)]



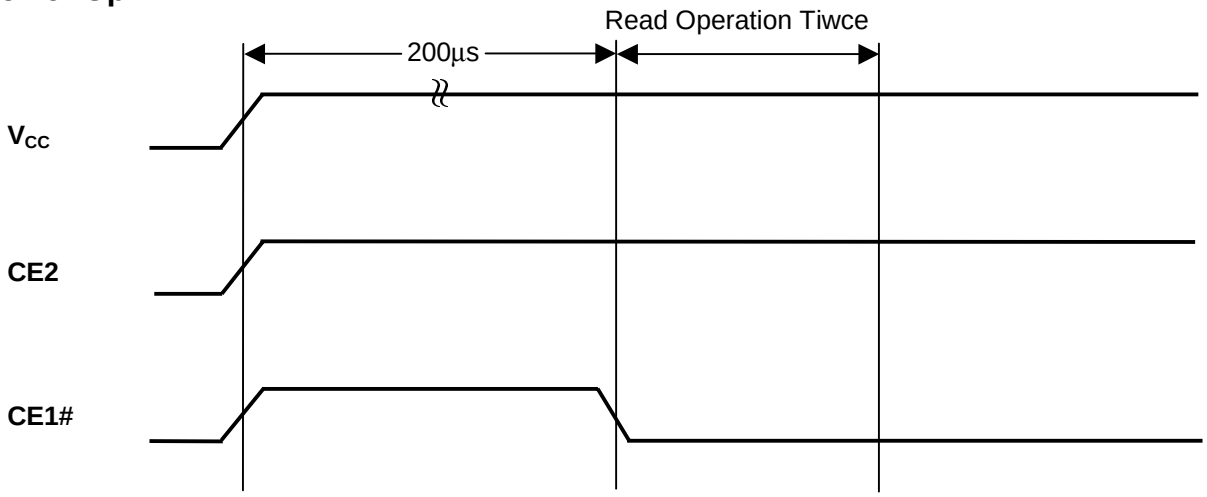
Notes:

1. CE2 = V_{IH}
2. CE2 = WE# = V_{IH}

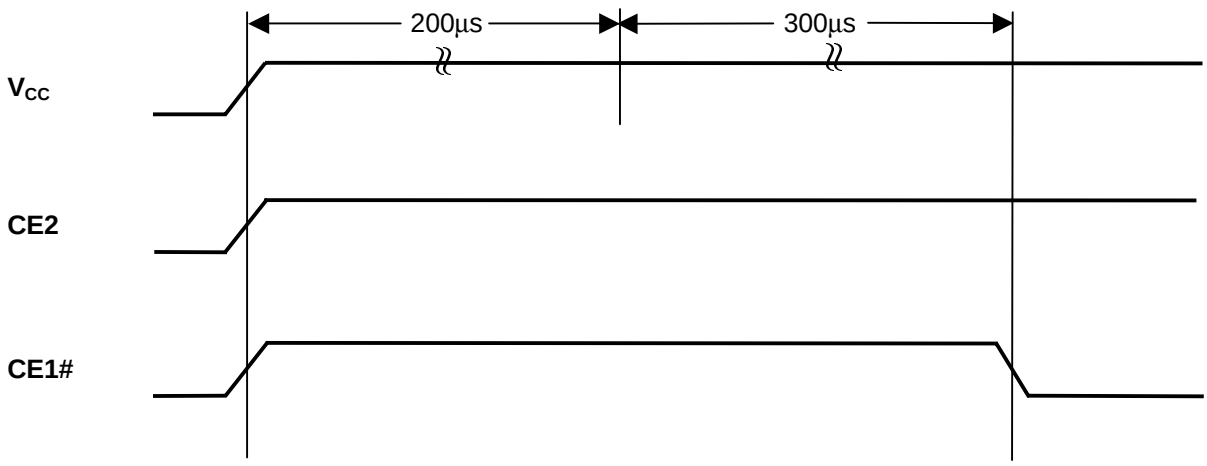
Deep Power Down Mode



Power Up 1



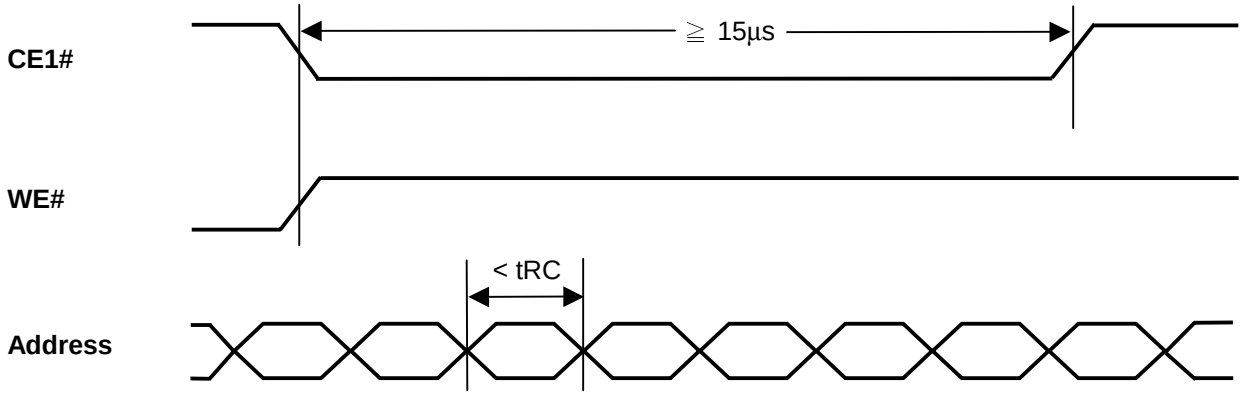
Power Up 2 (No Dummy Cycle)



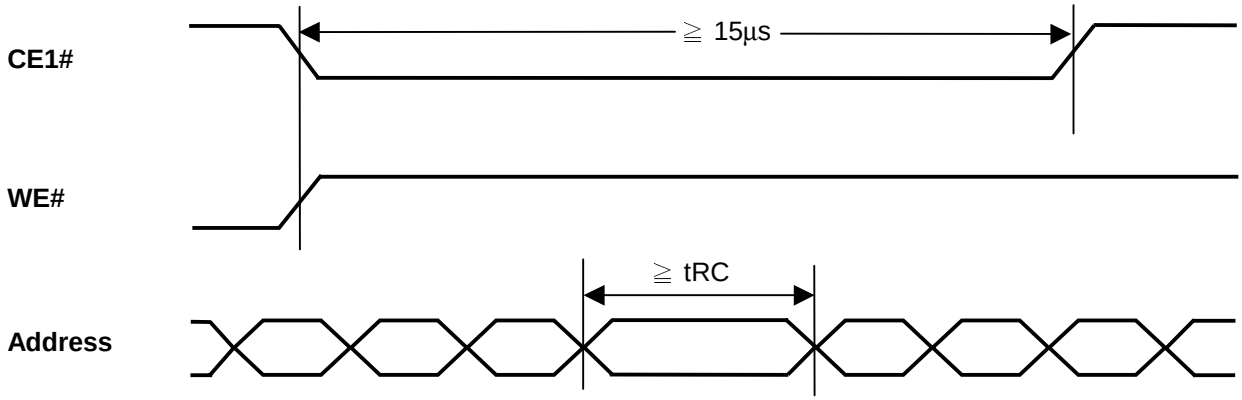
Avoid Timing

Etron Pseudo SRAM has a timing which is not supported at read operation. If your system has multiple invalid address signal shorter than tRC during over 15µs at read operation shown as in Abnormal Timing, it requires a normal read timing at leat during 15 µs shown as in Avoidable timing 1 or toggle CE1# to high (≧tRC) one time at least shown as in Avoidable Timing 2.

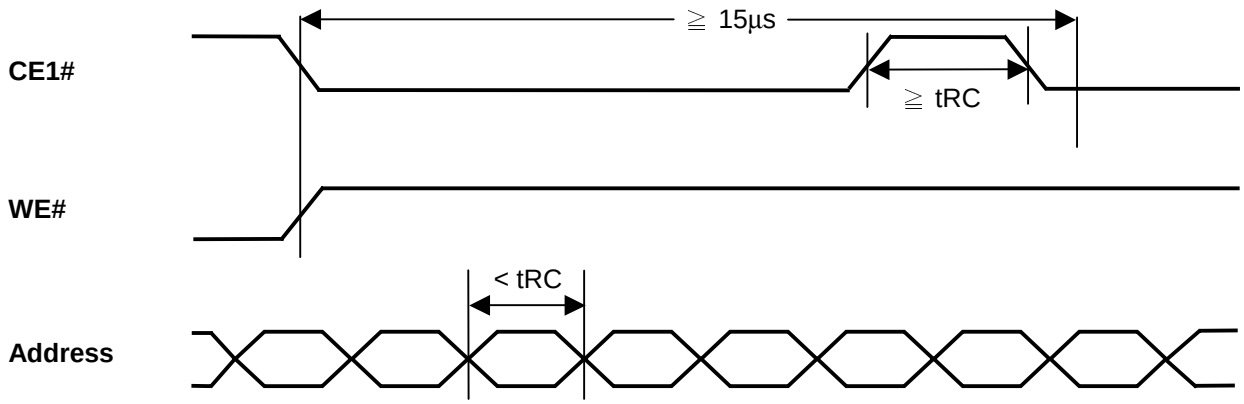
Abnormal Timing



Avoidable Timing 1



Avoidable Timing 2



Package Diagrams
48-Ball BGA
Units in mm

