8K X25097 1024 x 8 Bit

5MHz Low Power SPI Serial E²PROM with IDLock™ Memory

FEATURES

- **5MHz Clock Rate**
- **IDLock™ Memory**
  - **—IDLock First or Last Page, any 1/4 or Lower 1/2 of E²PROM Array**
- **Low Power CMOS**
  - **—<1μA Standby Current**
  - **—<3mA Active Current during Write**
  - **—<400μA Active Current during Read**
- **1.8V to 3.6V, 2.7V-5.5V or 4.5V to 5.5V Operation**
- **Built-in Inadvertent Write Protection**
  - **—Power-Up/Power-Down Protection Circuitry**
  - **—Write Enable Latch**
  - **—Write Protect Pin**
- **SPI Modes (0,0 & 1,1)**
- **1024 x 8 Bits**
  - **—16 Byte Page Mode**
- **Self-Timed Write Cycle**
  - **—5ms Write Cycle Time (Typical)**
- **High Reliability**
  - **—Endurance: 100,000 Cycles/Byte**
  - **—Data Retention: 100 Years**
  - **—ESD: 2000V on all pins**
- **8-Lead TSSOP Package**
- **8-Lead SOIC Package**
- **8-Lead PDIP Package**

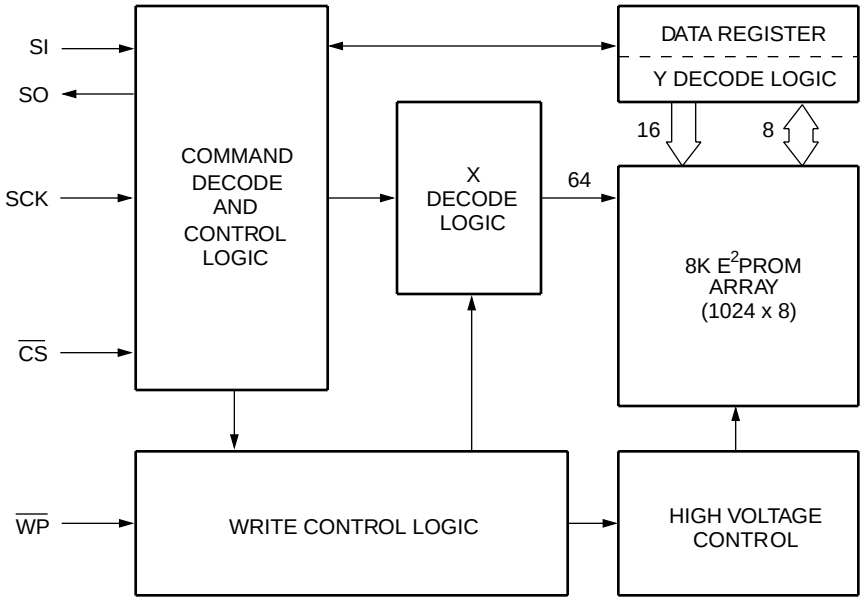
DESCRIPTION

The X25097 is a CMOS 8K-bit serial E²PROM, internally organized as 1024 x 8. The X25097 features a Serial Peripheral Interface (SPI) and software protocol allowing operation on a simple four-wire bus. The bus signals are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a chip select ($\overline{CS}$) input, allowing any number of devices to share the same bus.

IDLock is a programmble locking mechanism which allows the user to lock system ID and parametric data in different portions of the E²PROM memory space, ranging from as little as one page to as much as 1/2 of the total array. The X25097 also features a $\overline{WP}$ pin that can be used for hardwire protection of the part, disabling all write attempts, as well as a Write Enable Latch that must be set before a write operation can be initiated.

The X25097 utilizes Xicor's proprietary Direct Write™ cell, providing a minimum endurance of 100,000 cycles per byte and a minimum data retention of 100 years.

FUNCTIONAL DIAGRAM



7038 FRM F01

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PIN DESCRIPTIONS

Serial Output (SO)

SO is a push/pull serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

Serial Input (SI)

SI is a serial data input pin. All opcodes, byte addresses, and data to be written to the memory are input on this pin. Data is latched by the rising edge of the serial clock.

Serial Clock (SCK)

The Serial Clock controls the serial bus timing for data input and output. Opcodes, addresses, or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin change after the falling edge of the clock input.

Chip Select ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X25097 is deselected and the SO output pin is at high impedance and unless an internal write operation is underway, the X25097 will be in the standby power mode. $\overline{CS}$ LOW enables the X25097, placing it in the active power mode. It should be noted that after power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Write Protect ($\overline{WP}$)

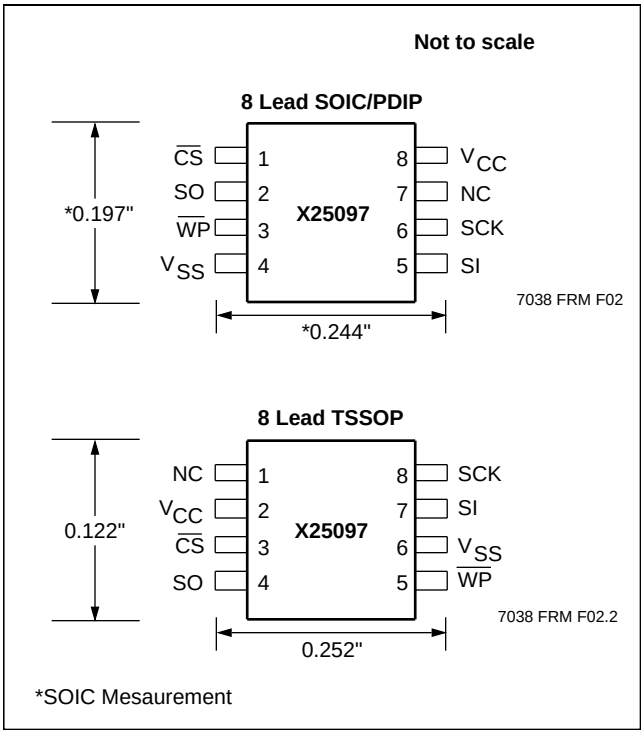
When $\overline{WP}$ is LOW, nonvolatile writes to the X25097 are disabled, but the part otherwise functions normally. When $\overline{WP}$ is held HIGH, all functions, including nonvolatile writes operate normally. $\overline{WP}$ going LOW while $\overline{CS}$ is still LOW will interrupt a write to the X25097. If the internal write cycle has already been initiated, $\overline{WP}$ going low will have no affect on this write.

PIN NAMES

Symbol	Description
$\overline{CS}$	Chip Select Input
SO	Serial Output
SI	Serial Input
SCK	Serial Clock Input
$\overline{WP}$	Write Protect Input
V_{SS}	Ground
V_{CC}	Supply Voltage
NC	No Connect

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PIN CONFIGURATION



PRINCIPLES OF OPERATION

The X25097 is a 1024 x 8 E^2PROM designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families.

The X25097 contains an 8-bit instruction register. It is accessed via the SI input, with data being clocked in on the rising edge of SCK. $\overline{CS}$ must be LOW and the $\overline{WP}$ input must be HIGH during the entire operation. Table 1 contains a list of the instructions and their opcodes. All instructions, addresses and data are transferred MSB first.

Data input is sampled on the first rising edge of SCK after $\overline{CS}$ goes LOW. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Write Enable Latch

The X25097 contains a “Write Enable” latch. This latch must be SET before a write operation is initiated. The WREN instruction will set the latch and the WRDI instruction will reset the latch (Figure 4). This latch is automatically reset upon a power-up condition and after the completion of a byte or page write cycle.

IDLock Memory

Xicor's IDLock Memory provides a flexible mechanism to store and lock system ID and parametric information. There are seven distinct IDLock Memory areas within the array which vary in size from one page to as much as half of the entire array. These areas and associated address ranges are IDLocked by writing the appropriate two byte IDLock instruction to the device as described in Table 1 and Figure 7. Once an IDLock instruction has been completed, that IDLock setup is held in a nonvolatile Status Register (Figure 1) until the next IDLock instruction is issued. The sections of the memory array that are IDLocked can be read but not written until IDLock Protection is removed or changed.

Figure 1. Status Register/IDLock Byte

7	6	5	4	3	2	1	0
0	0	0	0	0	IDL2	IDL1	IDL0

Note: Bits [7:3] specified to be "0's"

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Clock and Data Timing

Data input on the SI line is latched on the rising edge of SCK. Data is output on the SO line by the falling edge of SCK.

Read Sequence

When reading from the E^2PROM memory array, $\overline{CS}$ is first pulled LOW to select the device. The 8-bit READ instruction is transmitted to the X25097, followed by the 16-bit address, of which the last 10 bits are used (bits [15:10] specified to be zeroes). After the READ opcode and address are sent, the data stored in the memory at the selected address is shifted out on the SO line. The data stored in memory at the next address can be read sequentially by continuing to provide clock pulses. The address is automatically incremented to the next higher address after each byte of data is shifted out. When the highest address is reached (03FFh), the address counter rolls over to address 0000h, allowing the read cycle to be continued indefinitely. The read operation is terminated by taking $\overline{CS}$ HIGH. Refer to the Read Operation Sequence illustrated in Figure 2.

Read Status Operation

If there is not a nonvolatile write in progress, the Read Status instruction returns the ID Lock byte from the Status Register which contains the ID Lock bits IDL2-IDL0 (Figure 1). The ID Lock bits define the ID Lock condition (Figure 1/Table1). The other bits are reserved and will return '0' when read. See Figure 3.

If a nonvolatile write is in progress, the Read Status Instruction returns a HIGH on SO. When the nonvolatile write cycle is completed, the status register data is read out.

Clocking SCK is valid during a nonvolatile write in progress, but is not necessary. If the SCK line is clocked, the pointer to the status register is also clocked, even though the SO pin shows the status of the nonvolatile write operation (See Figure 3).

Write Sequence

Prior to any attempt to write data into the X25097, the "Write Enable" latch must first be set by issuing the WREN instruction (See Table 1 and Figure 4). $\overline{CS}$ is first taken LOW. Then the WREN instruction is clocked into the X25097. After all eight bits of the instruction are transmitted, $\overline{CS}$ must then be taken HIGH. If the user continues the write operation without taking $\overline{CS}$ HIGH after issuing the WREN instruction, the write operation will be ignored.

To write data to the E^2PROM memory array, the user then issues the WRITE instruction, followed by the 16 bit address and the data to be written. Only the last 10 bits of the address are used and bits [15:10] are specified to be zeroes. This is minimally a thirty-two clock operation. $\overline{CS}$ must go LOW and remain LOW for the duration of the operation. The host may continue to write up to 16 bytes of data to the X25097. The only restriction is the 16 bytes must reside on the same page. If the address counter reaches the end of the page and the clock continues, the counter will "roll over" to the first address of the page and overwrite any data that may have been previously written.

For a byte or page write operation to be completed, $\overline{CS}$ can only be brought HIGH after bit 0 of the last data byte to be written is clocked in. If it is brought HIGH at any other time, the write operation will not be completed. Refer to Figures 5 and 6 for detailed illustration of the write sequences and time frames in which $\overline{CS}$ going HIGH are valid.

IDLock Operation

Prior to any attempt to perform an IDLock Operation, the WREN instruction must first be issued. This instruction sets the “Write Enable” latch and allows the part to respond to an IDLock sequence (Figure 7). The IDLock instruction follows and consists of one command byte followed by one IDLock byte (See Figure 1). This byte contains the IDLock bits IDL2-IDL0. The rest of the bits [7:3] are unused and must be written as zeroes. Bringing $\overline{CS}$ HIGH after the two byte IDLock instruction initiates a nonvolatile write to the Status Register. Writing more than one byte to the Status Register will overwrite the previously written IDLock byte. See Table 1.

Operational Notes

The X25097 powers up in the following state:

- The device is in the low power, standby state.
- A HIGH to LOW transition on $\overline{CS}$ is required to enter an active state and receive an instruction.
- SO pin is at high impedance.
- The “Write Enable” latch is reset.

Data Protection

The following circuitry has been included to prevent inadvertant writes:

- The “Write Enable” latch is reset upon power-up.
- A WREN instruction must be issued to set the “Write Enable” latch.
- $\overline{CS}$ must come HIGH at the proper clock count in order to start a write cycle.

Table 1. Instruction Set and Block Lock Protection Byte Definition

Instruction Format*	Instruction Name and Operation
0000 0110	WREN: Set the Write Enable Latch (Write Enable Operation)
0000 0100	WRDI: Reset the Write Enable Latch (Write Disable Operation)
0000 0001	**IDLock Instruction—followed by:** **IDLock Byte: (See Figure 1)** 0000 0000 --->NO IDLock: 00h-00h- - - - - - - - - - ->None of the Array 0000 0001 --->IDLock Q1: 0000h-00FFh - - - - - - - ->Lower Quadrant (Q1) 0000 0010 --->IDLock Q2: 0100h-01FFh - - - - - - - ->Q2 0000 0011 --->IDLock Q3: 0200h-02FFh - - - - - - - ->Q3 0000 0100 --->IDLock Q4: 0300h-03FFh - - - - - - - ->Upper Quadrant (Q4) 0000 0101 --->IDLock H1: 0000h-01FFh - - - - - - - ->Lower Half of the Array (H1) 0000 0110 --->IDLock P0: 0000h-000Fh - - - - - - - ->Lower Page (P0) 0000 0111 --->IDLock Pn: 03F0h-03FFh - - - - - - - ->Upper Page (Pn)
0000 0101	READ STATUS: Reads IDLock & write in progress status on SO Pin
0000 0010	WRITE: Write operation followed by address and data
0000 0011	READ: Read operation followed by address

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*Instructions are shown with MSB in leftmost position. Instructions are transferred MSB first.

Figure 2. Read Operation Sequence

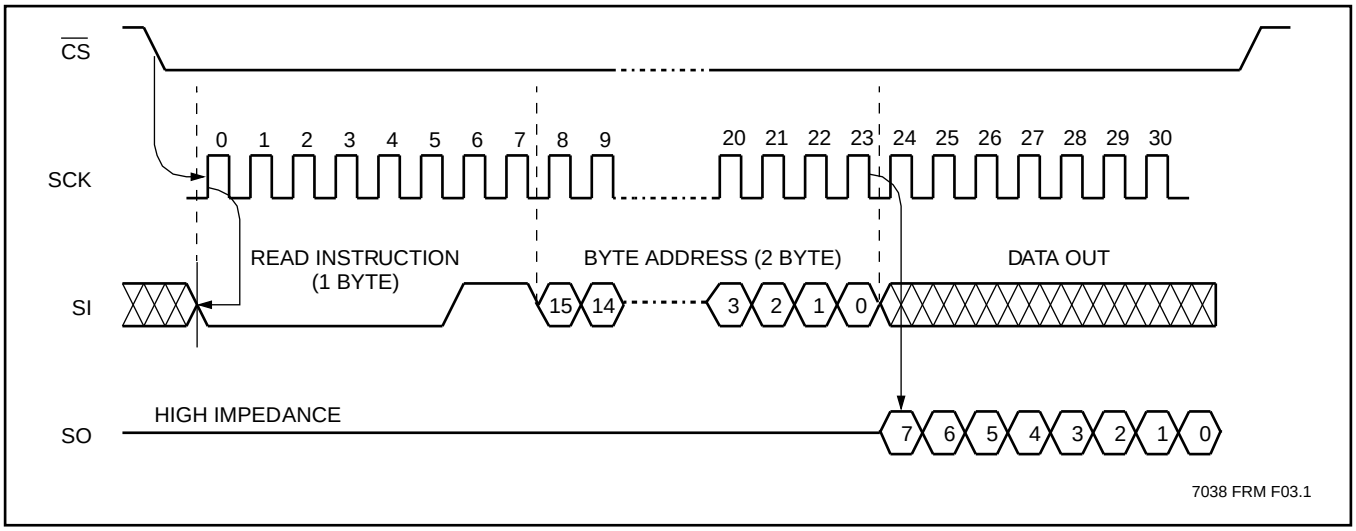


Figure 3. Read Status Operation Sequence

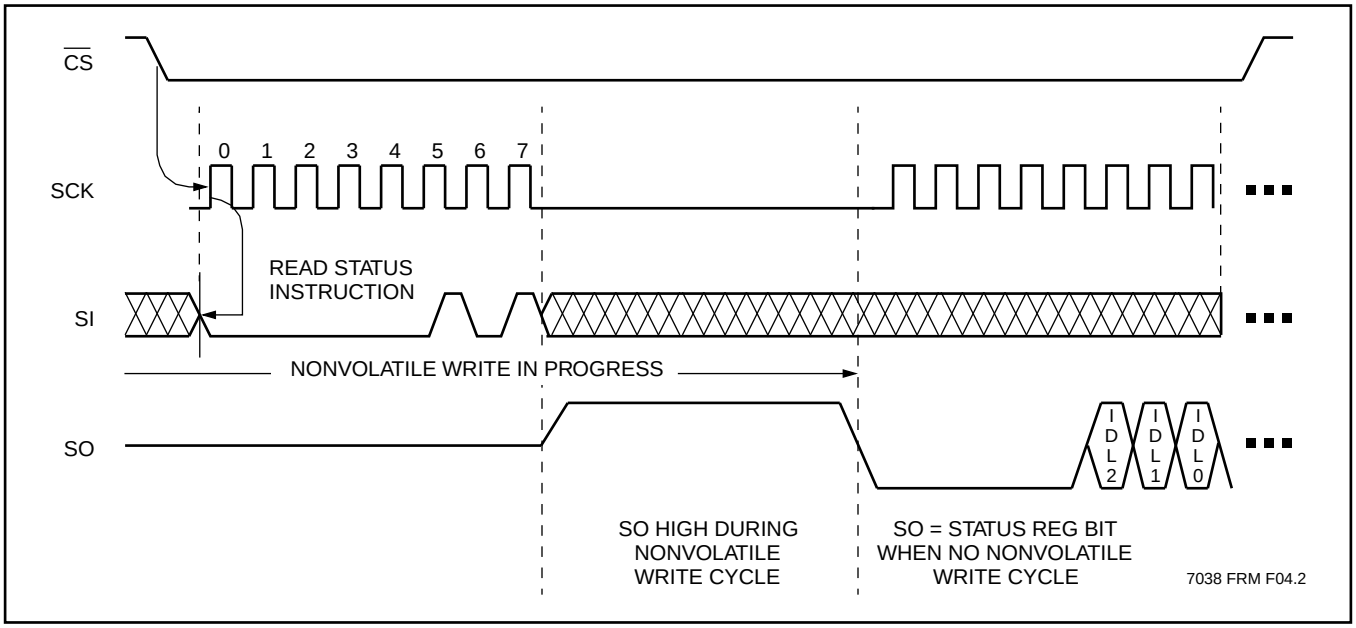


Figure 4. WREN/WRDI Sequence

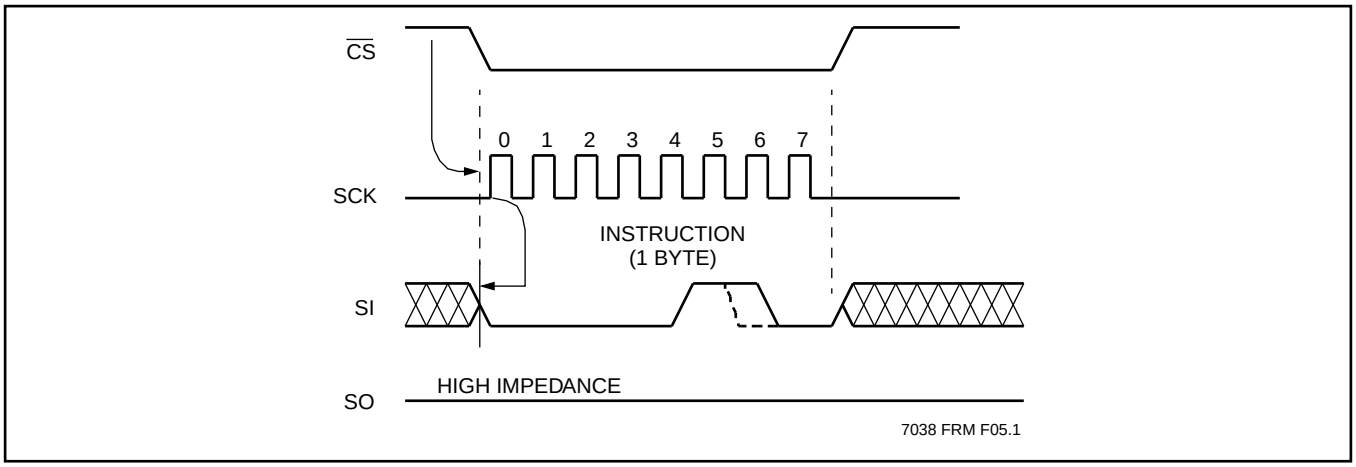


Figure 5. Byte Write Operation Sequence

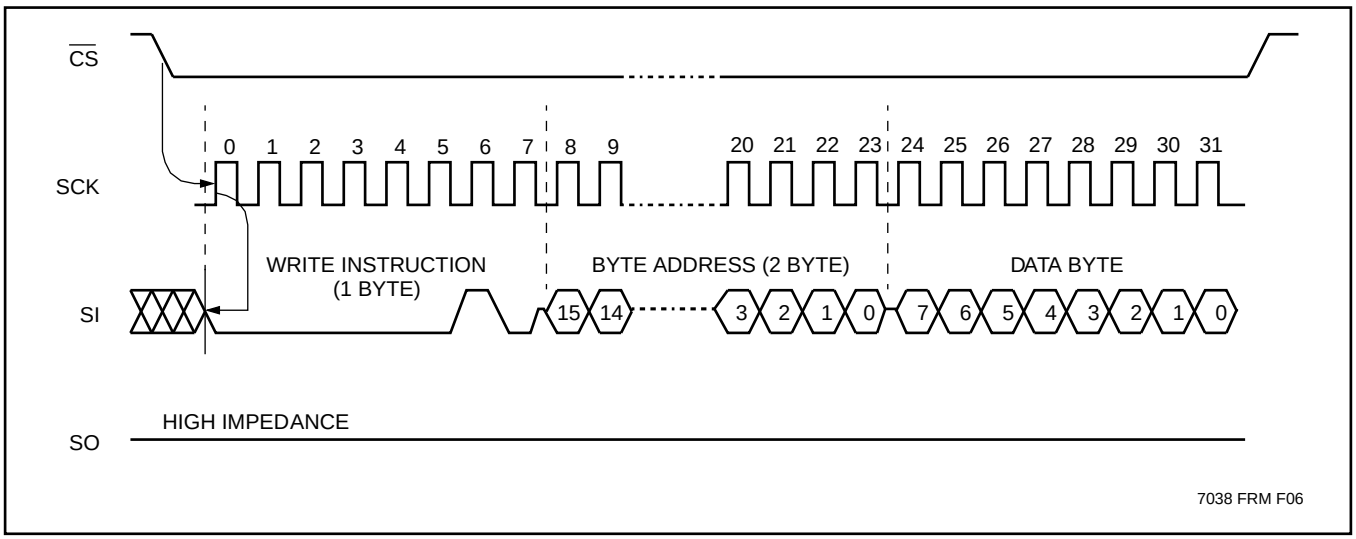


Figure 6. Page Write Operation Sequence

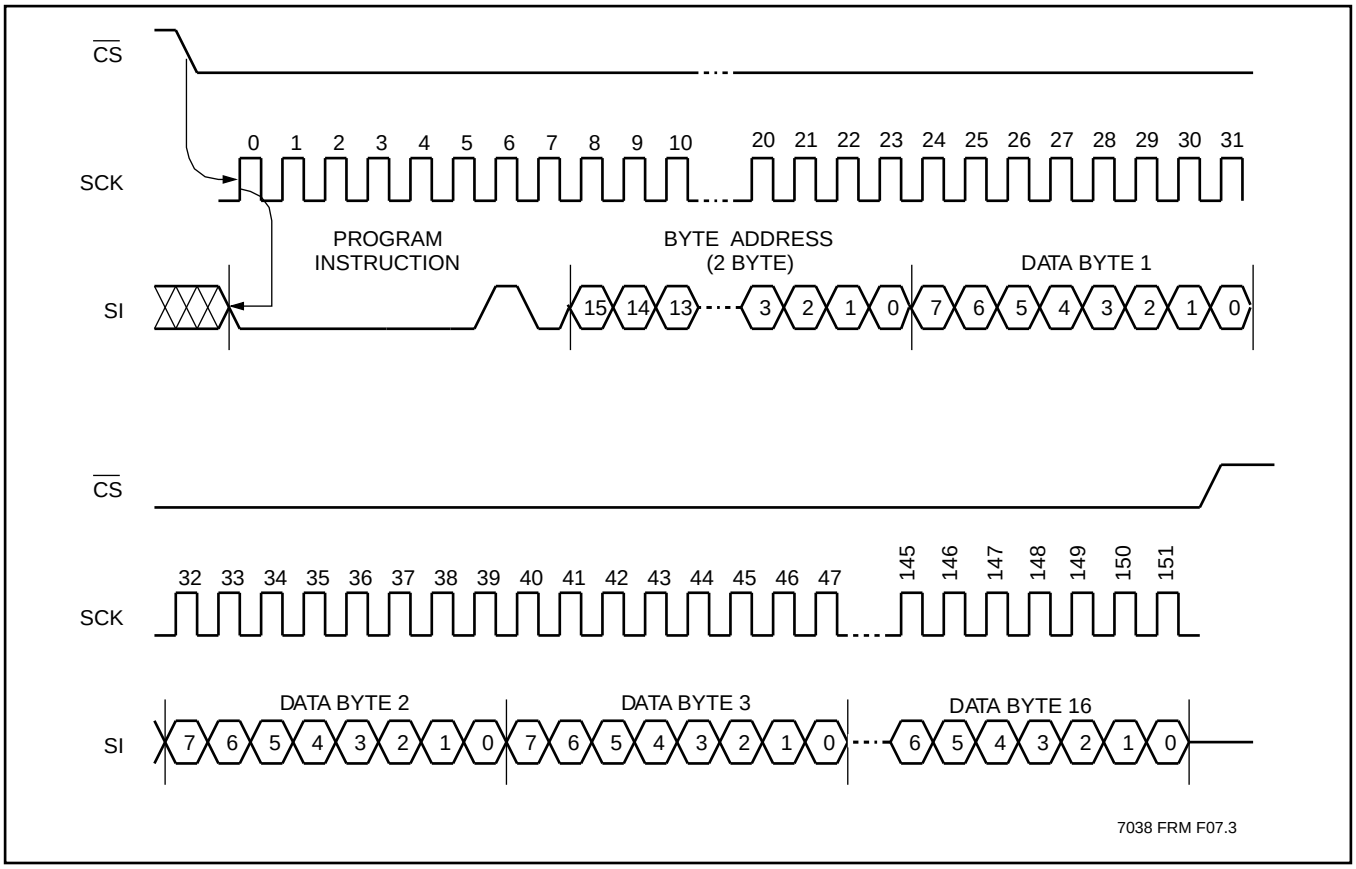
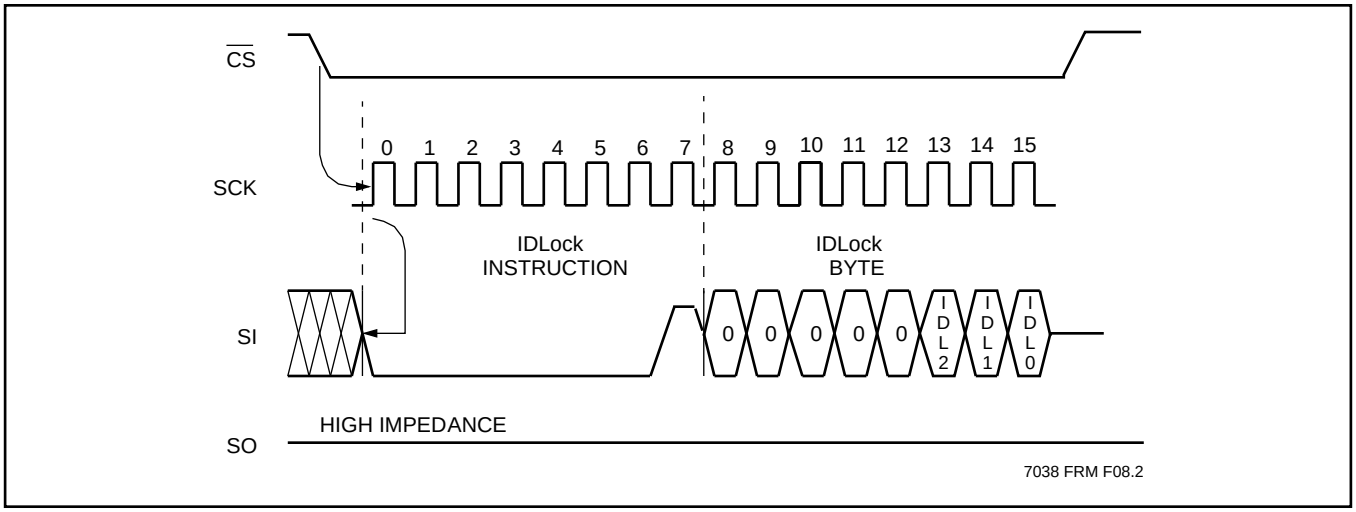


Figure 7. IDLock Operation Sequence



ABSOLUTE MAXIMUM RATINGS*

Temperature under Bias ..... –65°C to +135°C
Storage Temperature ..... –65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1V to +7V
D.C. Output Current..... 5mA
Lead Temperature
(Soldering, 10 seconds)..... 300°C

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C

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Supply Voltage	Limits
X25097	4.5V to 5.5V
X25097-2.7	2.7V to 5.5V
X25097-1.8	1.8V to 3.6V

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D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC1}	V_{CC} Supply Current (Write)		3	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 5MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{CC2}	V_{CC} Supply Current (Read)		400	µA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 5MHz, SO = Open, $\overline{CS}$ = V_{SS}
I_{SB}	V_{CC} Supply Current (Standby)		1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW Voltage	–0.5	V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH Voltage	V_{CC} x 0.7	V_{CC} + 0.5	V	
V_{OL1}	Output LOW Voltage		0.4	V	V_{CC} > 3.3V, I_{OL} = 2.1mA
V_{OL2}	Output LOW Voltage		0.4	V	2V < V_{CC} ≤ 3.3V, I_{OL} = 1mA
V_{OL3}	Output LOW Voltage		0.4	V	V_{CC} ≤ 2V, I_{OL} = 0.5mA
V_{OH1}	Output HIGH Voltage	V_{CC} – 0.8		V	V_{CC} > 3.3V, I_{OH} = -1.0mA
V_{OH2}	Output HIGH Voltage	V_{CC} – 0.4		V	2V < V_{CC} ≤ 3.3V, I_{OH} = -0.4mA
V_{OH3}	Output HIGH Voltage	V_{CC} – 0.2		V	V_{CC} ≤ 2V, I_{OH} = -0.25mA

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POWER-UP TIMING

Symbol	Parameter	Min.	Max.	Units
t_{PUR}(2)	Power-up to Read Operation		1	ms
t_{PUW}(2)	Power-up to Write Operation		5	ms

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Notes: (1) V_{IL} Min. and V_{IH} Max. are for reference only and are not 100% tested.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

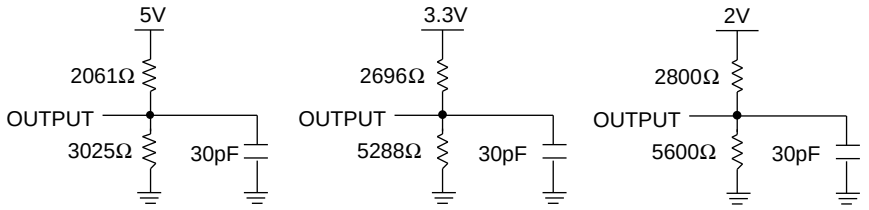
CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5.0V.

Symbol	Parameter	Max.	Units	Conditions
C_{OUT}(3)	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}(3)	Input Capacitance (SCK, SI, $\overline{CS}$, $\overline{WP}$)	6	pF	V_{IN} = 0V

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Notes: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



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A.C. TEST CONDITIONS

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10ns
Input and Output Timing Level	V_{CC} X 0.5

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A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

Data Input Timing

Symbol	Parameter	Voltage	Min.	Max.	Units
f_{SCK}	Clock Frequency	2.7V–5.5V 1.8V–3.6V	0	5 3.3	MHz
t_{CYC}	Cycle Time	2.7V–5.5V 1.8V–3.6V	200 300		ns
t_{LEAD}	$\overline{CS}$ Lead Time	2.7V–5.5V 1.8V–3.6V	100 150		ns
t_{LAG}	$\overline{CS}$ Lag Time	2.7V–5.5V 1.8V–3.6V	100 150		ns
t_{WH}	Clock HIGH Time	2.7V–5.5V 1.8V–3.6V	80 130		ns
t_{WL}	Clock LOW Time	2.7V–5.5V 1.8V–3.6V	80 130		ns
t_{SU}	Data Setup Time		20		ns
t_H	Data Hold Time		20		ns
t_{RI}(3)	Data In Rise Time			2	µs
t_{FI}(3)	Data In Fall Time			2	µs
t_{CS}	$\overline{CS}$ Deselect Time		100		ns
t_{WC}(4)	Write Cycle Time			10	ms

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Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

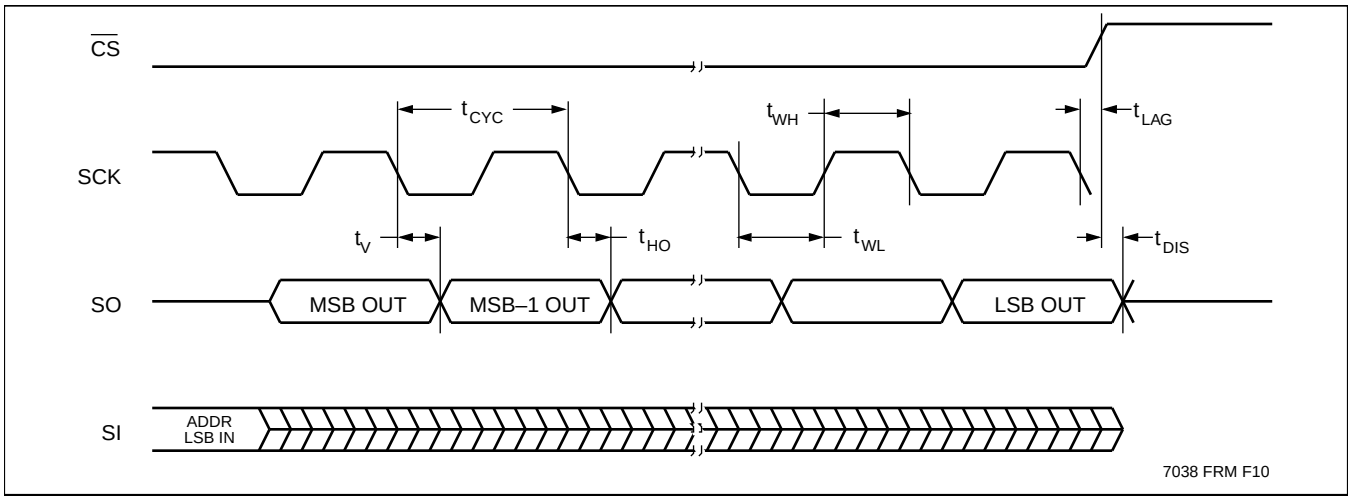
Data Output Timing

Symbol	Parameter	Voltage	Min.	Max.	Units
f_{SCK}	Clock Frequency	2.7V–5.5V 1.8V–3.6V	0	5 3.3	MHz
t_{DIS}	Output Disable Time	2.7V–5.5V 1.8V–3.6V		100 150	ns
t_V	Output Valid from Clock LOW	2.7V–5.5V 1.8V–3.6V		80 130	ns
t_{HO}	Output Hold Time		0		ns
t_{RO}(5)	Output Rise Time			50	ns
t_{FO}(5)	Output Fall Time			50	ns

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Notes: (5) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

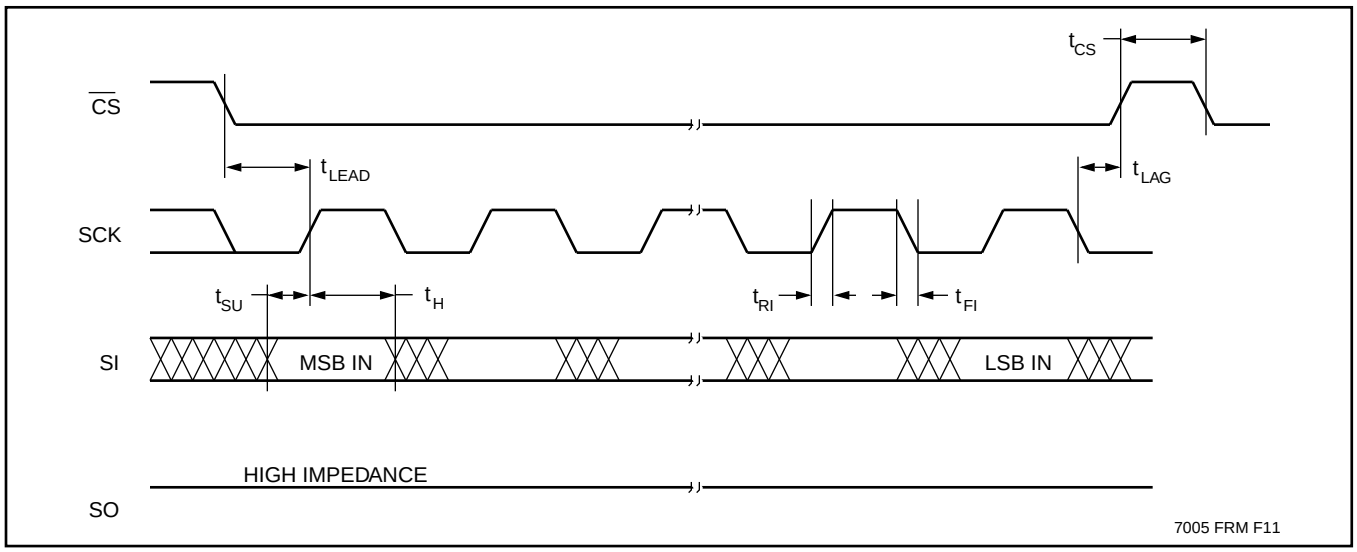
Figure 8. Serial Output Timing



SYMBOL TABLE

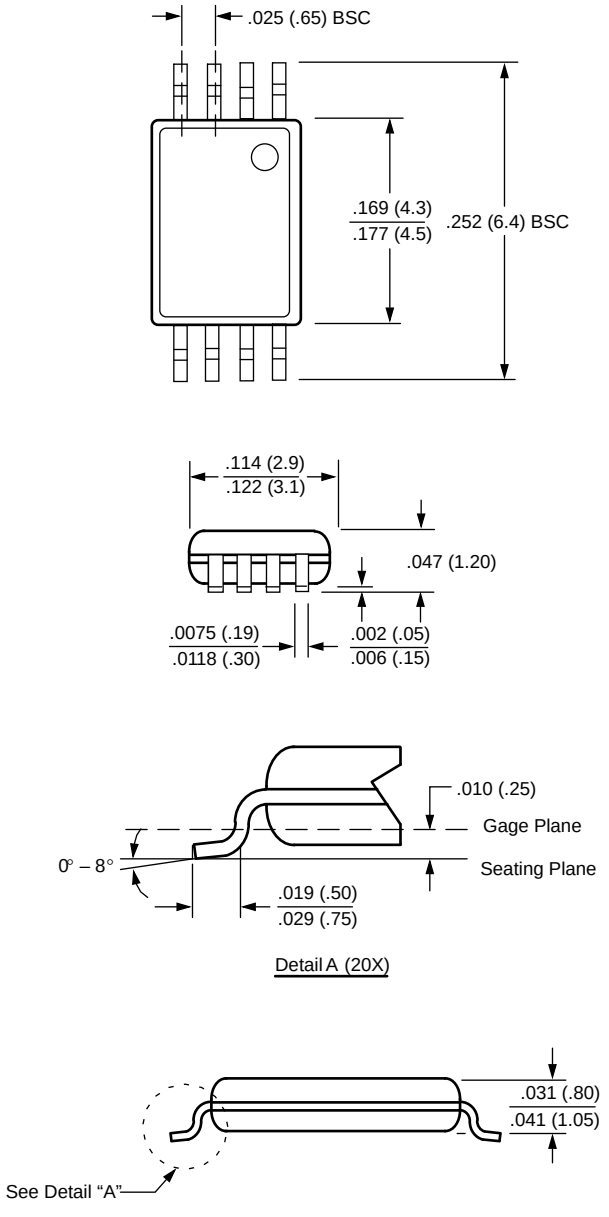
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Figure 9. Serial Input Timing



PACKAGING INFORMATION

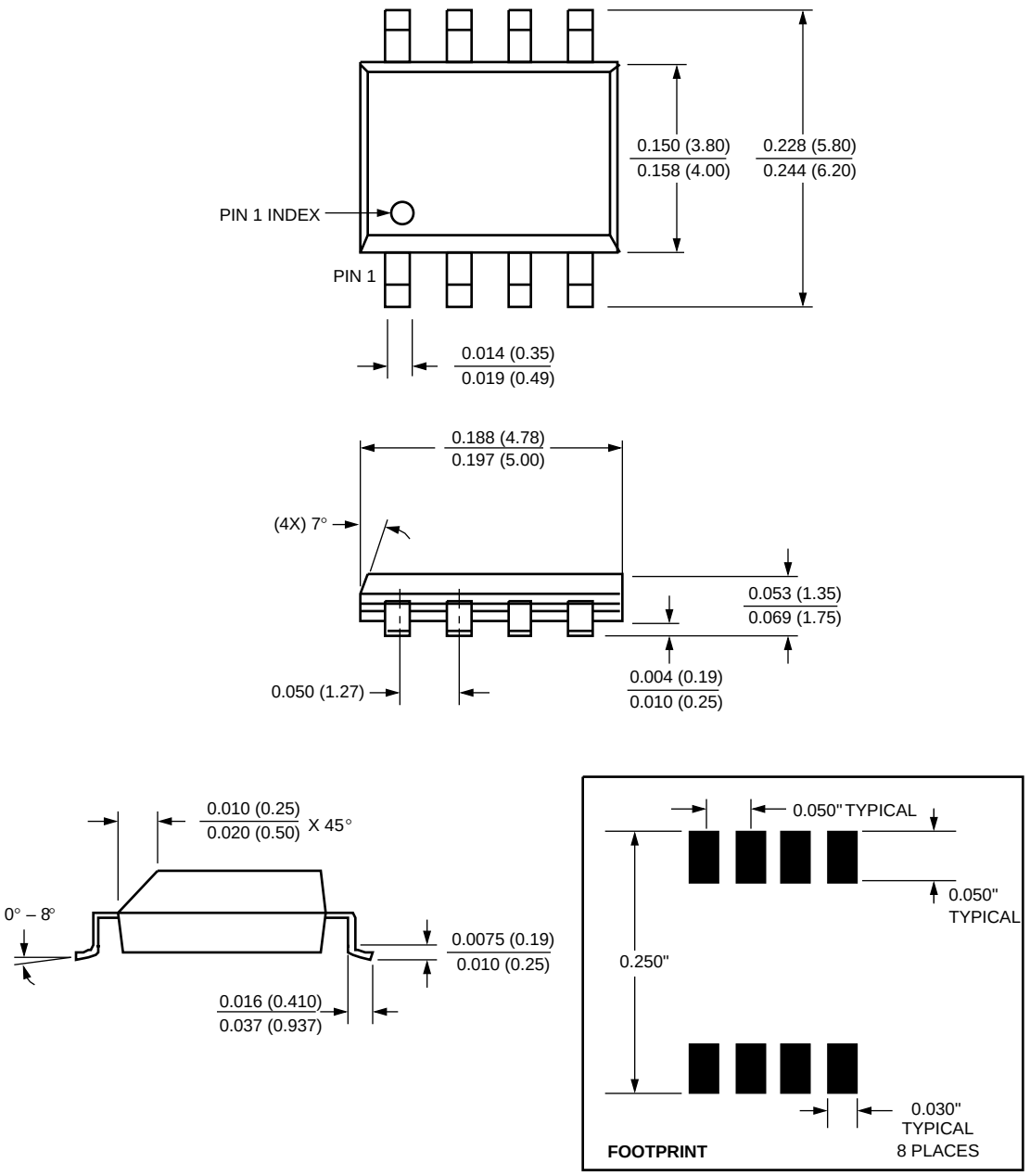
8-LEAD PLASTIC, TSSOP, PACKAGE TYPE V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S

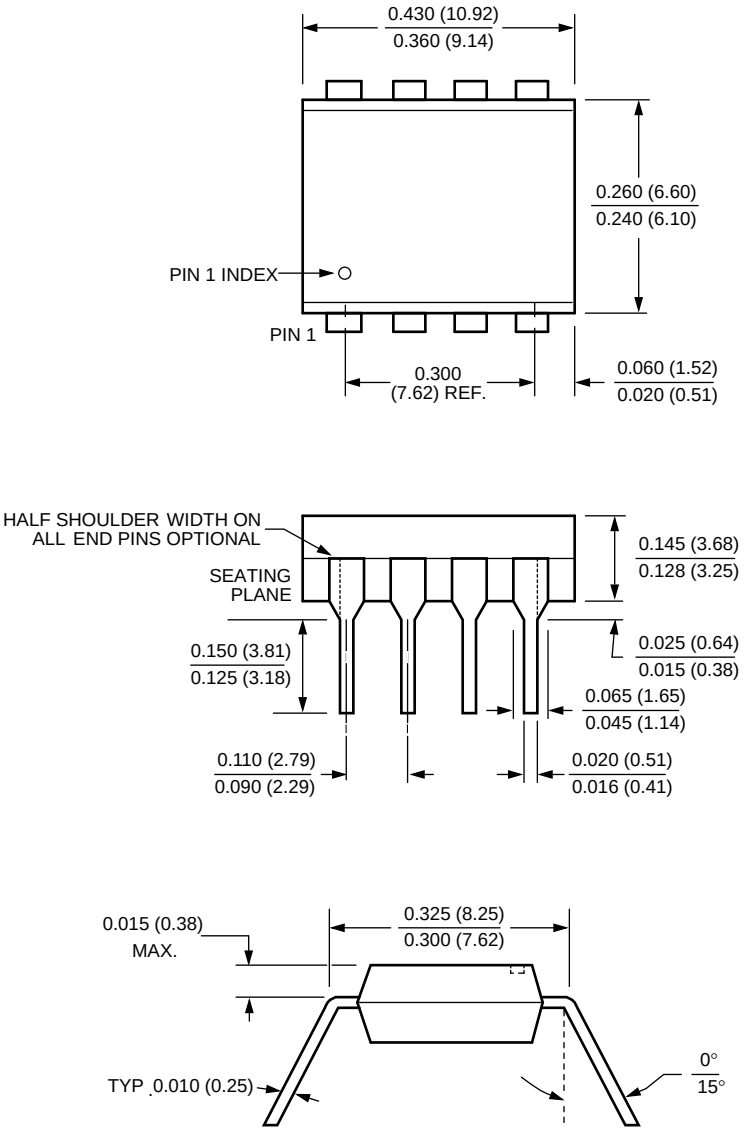


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FRM F22.1

PACKAGING INFORMATION

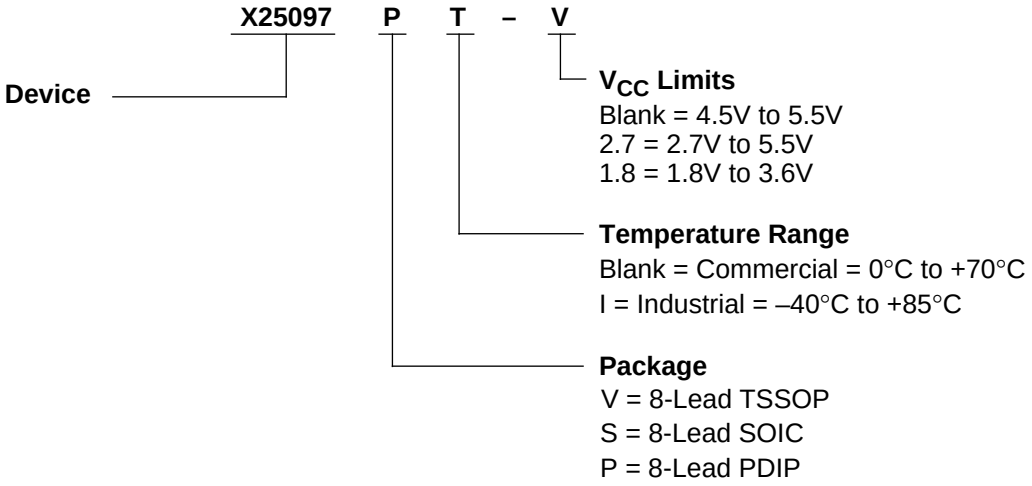
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

ORDERING INFORMATION



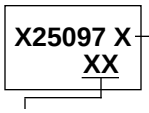
Part Mark Convention

8-Lead TSSOP



AG = 1.8 to 3.6V, 0 to +70°C
AH = 1.8 to 3.6V, -40 to +85°C
F = 2.7 to 5.5V, 0 to +70°C
G = 2.7 to 5.5V, -40 to +85°C
Blank = 4.5 to 5.5V, 0 to +70°C
I = 4.5 to 5.5V, -40 to +85°C

8-Lead SOIC/PDIP



Blank = 8-Lead SOIC
P = 8-Lead PDIP

AG = 1.8 to 3.6V, 0 to +70°C
AH = 1.8 to 3.6V, -40 to +85°C
F = 2.7 to 5.5V, 0 to +70°C
G = 2.7 to 5.5V, -40 to +85°C
Blank = 4.5 to 5.5V, 0 to +70°C
I = 4.5 to 5.5V, -40 to +85°C

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U.S. PATENTS

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LIFE RELATED POLICY

In situations where semiconductor component failure may endanger life, system designers using this product should design the system with appropriate error detection and correction, redundancy and back-up features to prevent such an occurence.

Xicor's products are not authorized for use in critical components in life support devices or systems.

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.