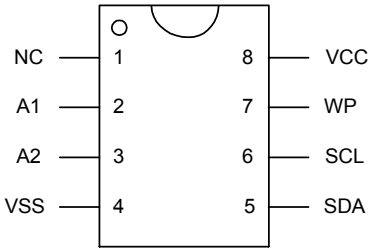
■ Features

- State- of- the- art architecture
  - Non-volatile data storage
  - Standard voltage and low voltage operation (Vcc = 2.7V to 5.5V) for AM24LC04
- 2-wire I^2C serial interface
  - Provides bi-directional data transfer protocol
- 16-byte page write mode
  - Minimizes total write time per word
- Self-timed write-cycle (including auto-erase)
- Durable and Reliable
  - 40 years data retention
  - Minimum of 1M write/erase cycles per word
  - Unlimited read cycles
  - ESD protection
- Low standby current
- Packages: PDIP-8L, SOP-8L, TSSOP-8L

■ General Description

The AM24LC04 is a non-volatile, 4096-bit serial EEPROM with conforms to all specifications in I^2C 2 wire protocol. The whole memory can be disabled (Write Protected) by connecting the WP pin to Vcc. This section of memory then becomes unalterable unless WP is switched to Vss. The AM24LC04 communication protocol uses CLOCK(SCL) and DATA I/O(SDA) lines to synchronously clock data between the master (for example a microcomputer)and the slave EEPROM devices(s) .In addition, the bus structure allows for a maximum of 16K of EEPROM memory. This supports the family in 2K, 4K, 8K devices, allowing the user to configure the memory as the application requires with any combination of EEPROMs (not to exceed 16K).
Anachip EEPROMs are designed and tested for application requiring high endurance, high reliability, and low power consumption.

■ Connection Diagram



PDIP / SOP / TSSOP

■ Pin Assignments

Name	Description
NC	No connect
A1, A2	Device address inputs
VSS	Ground
SDA	Data I/O
SCL	Clock input
WP	Write protect
VCC	Power pin

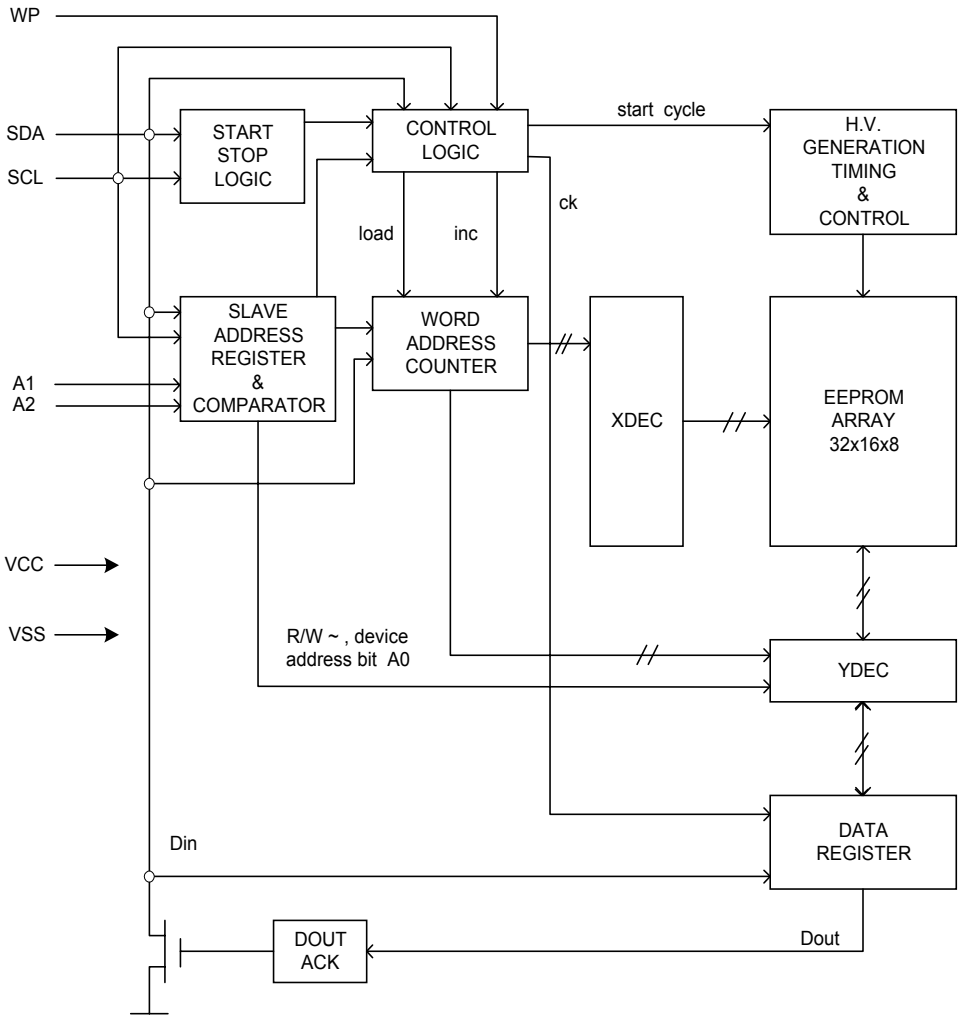
■ Ordering Information

AM 24 LC 04 X XX X

Operating Voltage	Type	Temp. grade	Package	Packing
LC: 2.7~5.5V, CMOS	04 =4K	Blank : 0°C ~ +70°C I : – 40°C ~ +85°C V : – 40°C ~ +125°C	S: SOP-8L N: PDIP-8L TS: TSSOP-8L	Blank : Tube A : Taping

This datasheet contains new product information. Anachip Corp. reserves the rights to modify the product specification without notice. No liability is assumed as a result of the use of this product. No rights under any patent accompany the sale of the product.

■ Block Diagrams



■ Absolute Maximum Ratings

Characteristics	Symbol	Values	Unit
Storage Temperature	T_S	-65 to + 125	°C
Voltage with Respect to Ground		-0.3 to + 6.5	V

Note: These are STRESS rating only. Appropriate conditions for operating these devices given elsewhere may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

■ Operating Conditions

Temperature under bias	Values	Unit
AM24LC04	0 to + 70	°C
AM24LC04I	-40 to +85	°C
AM24LC04V	-40 to +125	°C

■ Electrical Characteristics

DC Electrical Characteristics (Vcc =2.7~5.5V, Ta = 25°C)

Parameter	Symbol	Conditions	AM24LC04		Units
			Min	Max	
Operating Current (Program) **	I_{CC1}	SCL = 100KHZ CMOS Input Levels	—	3	mA
Operating Current (Read) **	I_{CC2}	SCL = 100KHZ CMOS Input Levels	—	200	µA
Standby Current	I_{SB1}	SCL=SDA=0V, Vcc=5V	—	10	µA
Standby Current	I_{SB2}	SCL=SDA=0V, Vcc=3V	—	1	µA
Input Leakage	I_{IL}	VIN = 0 V to VCC	-1	+1	µA
Output Leakage	I_{OL}	VOUT = 0 V to Vcc	-1	+1	µA
Input Low Voltage**	V_{IL}		-0.1	Vcc x 0.3	V
Input High Voltage**	V_{IH}		Vcc x 0.7	V_{CC}+ 0.2	V
Output Low Voltage	V_{OL1}	IOL = 2.1mA TTL	—	0.4	V
Output Low Voltage	V_{OL2}	IOL = 10uA CMOS	—	0.2	V
VCC Lockout Voltage	V_{LK}	Programming Command Can Be Executed	Default	—	V

Note ** : I_{CC1}, I_{CC2}, V_{IL} min and V_{IH} max are for reference only and are not tested.

■ Switching Characteristics (Under Operating Conditions)

AC Electrical Characteristics (Vcc =2.7~5.5V)

Parameter	Symbol	AM24LC04		Units
		Min	Max	
Clock frequency	Fscl	0	100	kHz
Clock high time	Thigh	4000	—	ns
Clock low time	Tlow	4700	—	ns
SDA and SCL rise time**	Tr	—	1000	ns
SDA and SCL fall time**	Tf	—	300	ns
START condition hold time	Thd:Sta	4000	—	ns
START condition setup time	Tsu:Sta	4700	—	ns
Data input hold time	Thd:Dat	0	—	ns
Data input setup time	Tsu:Dat	250	—	ns
STOP condition setup time	Tsu:Sto	4000	—	ns
Output valid from clock	Taa	300	3500	ns
Bus free time **	Tbuf	4700	—	ns
Data out hold time	Tdh	300	—	ns
Write cycle time	Twr	—	10	ms
5V, 25ºC, Byte Mode	Endurance**	1M	—	write cycles

Note **: This parameter is characterized and is not 100% tested.

Pin Capacitance ** (Ta= 25°C, f=250KHz)

Symbol	Parameter	Max	Units
C_{OUT}	Output capacitance	5	pF
C_{IN}	Input capacitance	5	pF

Note ** : This parameter is characterized and is not 100% tested.

AC. Conditions of Test

Input Pulse Levels	Vcc x 0.1 to Vcc x 0.9
Input Rise and Fall times	10 ns
Input and Output Timming level	Vcc x 0.5
Output Load	1 TTL Gate and CL = 100pf

■ Pin Descriptions

Serial Clock (SCL)
The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)
SDA is a bidirection pin used to transfer data into and out of the device.
It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. Thus, the SDA bus requires a pull-up resistor to Vcc (typical 4.7KΩ for 100KHz)

Device Address Inputs (A0, A1, A2)
The following table (Table A) shows the active pins across the AM24LCXX device family.

Table A

Device	A0	A1	A2
AM24LC02	ADR	ADR	ADR
AM24LC04	XP	ADR	ADR
AM24LC08	XP	XP	ADR
AM24LC16	XP	XP	XP

ADR indicates the device address pin.
XP indicates that device address pin don't care but refers to an internal PAGE BLOCK memory segment.

Write Protection (WP)
If WP is connected to Vcc, PROGRAM operation onto the whole memory will not be executed. READ operations are possible. If WP is connected to Vss, normal memory operation is enabled, READ/WRITE over the entire memory is possible.

■ Functional Description

Applications
ATC's electrically erasable programmable read only memories (EEPROMs) write protect function, two write modes, three read modes, and a wide variety of memory size. Typical applications for the I^2C bus and AM24LCXX memories are included in SANs(small-area-networks), stereos, televisions, automobiles and other scaled-down systems that don't require tremendous speeds but instead cost efficiency and design simplicity.

Endurance and Data Retention
The AM24LC04 is designed for applications requiring up to 1M programming cycles (BYTE WRITE and PAGE WRITE). It provides 40 years of secure data retention without power.

Device Operation
The AM24LC04 support a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the AM24LC04 is considered a slave in all applications.

Clock and Data Conventions
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. (Shown in Figures 1 and 2)

Start Condition
A HIGH to LOW transition of the SDA line while the clock (SCL) is HIGH determines a START condition. All commands must be preceded by a START condition. (Shown in Figure 2)

Stop Condition
A LOW to HIGH transition of the SDA line while the clock (SCL) is HIGH determines a STOP condition. All operations must be ended with a STOP condition. (Shown in Figure 2)

■ Functional Description (Continued)

Acknowledge
Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this acknowledge bit. The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition. (Shown in Figure 3)

Devices Addressing
After generating a START condition, the bus master transmits the slave address consisting of a 4-bit device code (1010) for the AM24LC04, 3-bit device address (A2 A1 A0) and 1-bit value indicating the read or write mode. All I^2C EEPROMs use and internal protocol that defines a PAGE BLOCK size of 4K bits. The eighth bit of slave address determines if the master device wants to read or write to the AM24LC04. (Refer to table B).

The AM24LC04 monitor the bus for its corresponding slave address all the time. It generates an acknowledge bit if the slave address was true and it is not in a programming mode.

Table B

Operation	Control Code	Chip Select	R/W
Read	1010	A2 A1 A0	1
Write	1010	A2 A1 A0	0

A1, A2 are used to access device address for AM24LC04; A0 is no connect.

■ Write Operations

Byte Write
Following the start signal from the master, the slave address is placed onto the bus by the master transmitter. This indicates to the addressed slave receiver that a byte with a word address will follow after it has generated a acknowledge bit during the ninth clock cycle.

Therefore the next byte transmitted by the master is the word address and will be written into the address pointer of the AM24LC04. After receiving another acknowledge signal from the AM24LC04 the master device will transmit the data word to be written into the addressed memory location. The AM24LC04 acknowledges again and the master generates a stop condition. This initiates the internal write cycle, and during this period the AM24LC04 will not generate acknowledge signals. (Shown in Figure 4)

Page Write
The write control byte, word address and the first data byte are transmitted to the AM24LC04 in the same way as in a byte write. But instead of generating a stop condition the master transmit up to 16 data bytes to the AM24LC04 which are temporarily stored in the on-chip page buffer and will be written into the memory after the master has transmitted a stop condition. After the receipt of each byte, the four lower order address pointer bits are internally incremented by one. The higher order five bits of the word address remains constant. If the master should transmit more than 16 bytes prior to generating the stop condition, the address counter will roll over and the previously received data will be overwritten. As with the byte write operation, once the stop condition is received an internal write cycle will begin. (Shown in Figure 5).

Acknowledge Polling
Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete (this feature can be used to maximize bus throughout). Once the stop condition for a write command has been issued from the master, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the master sending a start condition followed by the control byte for a write command (R/W = 0). If the device is still busy with the write cycle , then no ACK will returned. If the cycle is complete then the device will return the ACK and the master can then proceed with the next read or write commands.

■ Write Operations (Continued)

Write Protection
Programming will not take place if the WP pin of the AM24LC04 is connected to Vcc. The AM24LC04 will accept slave and byte addresses. But if the memory accessed is write protected by the WP pin, the AM24LC04 will not generate an acknowledge after the first byte of data has been received, and thus the programming cycle will not be started when the stop condition is asserted.

Read Operations
Read operations are initiated in the same way as write operations with the exception that the R/W bit of the slave address is set to one. There are three basic types of read operations: current address read, random read, and sequential read.

Current Address Read
The AM24LC04 contains an address counter that maintains the address of the last accessed word, internally incremented by one. Therefore if the previous access (either a read or write operation) was to address n, the next current address read operation would access data from address n + 1. Upon receipt of the slave address with R/W bit set to one, the AM24LC04 issues an acknowledge and transmits the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the AM24LC04 discontinues transmission. (Shown in Figure 6)

Random Read
Random read operations allow the master to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the AM24LC04 as part of a write operation. After the word address is sent, the master generates a start condition following the acknowledge. This terminates the write operation, but not before the internal address pointer is set. Then the master issues the control byte again but with R/W bit set to a one. The AM24LC04 will then issue an acknowledge and transmit the eight bit data word. The master will not acknowledge the transfer but does generate a stop condition and the AM24LC04 discontinues transmission. (Shown in Figure 7)

Sequential Read
Sequential reads are initiated by either a current address read or a random read. After the master receives a data word, it responds with an acknowledge. As long as the E^2PROM receives an acknowledge, it will continue to increment the data words. When the memory address limit is reached, the data word address will “roll over” and the sequential read will continue. The sequential read operation is terminated when the master does not respond with a zero but does generate a following stop condition.

■ Timing Diagram

Bus Timing

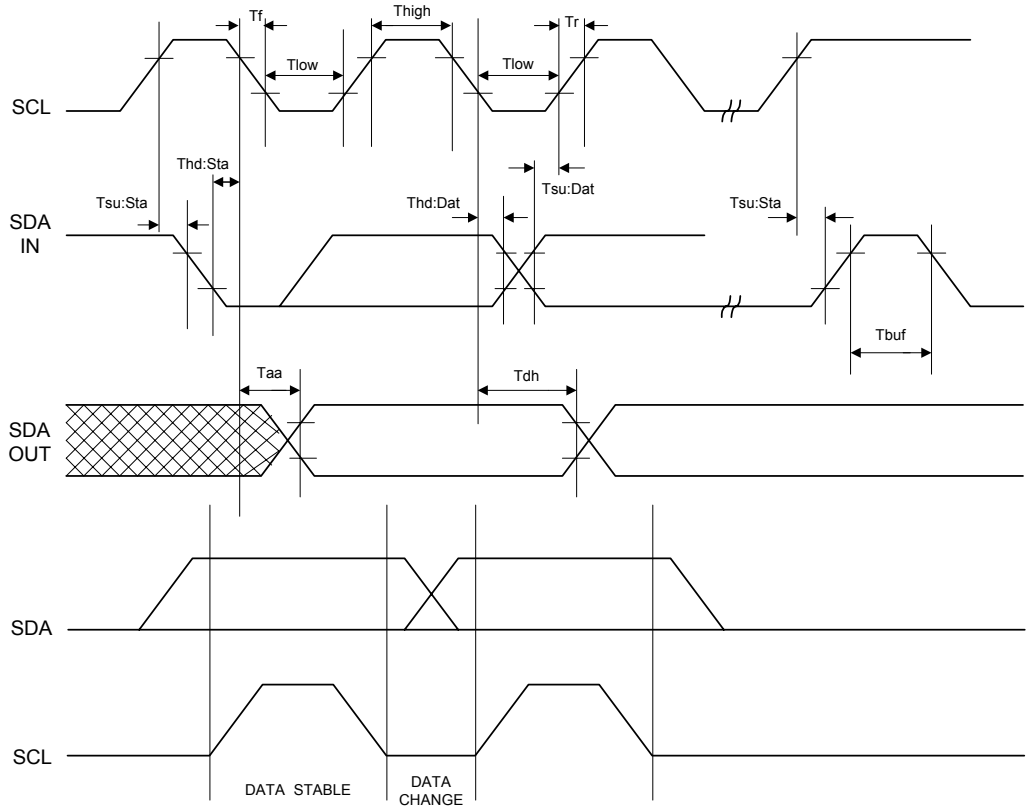


Figure 1. Data Validity

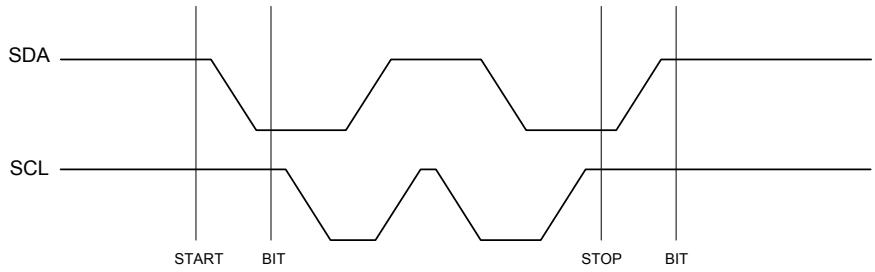


Figure 2. Definition of Start and Stop

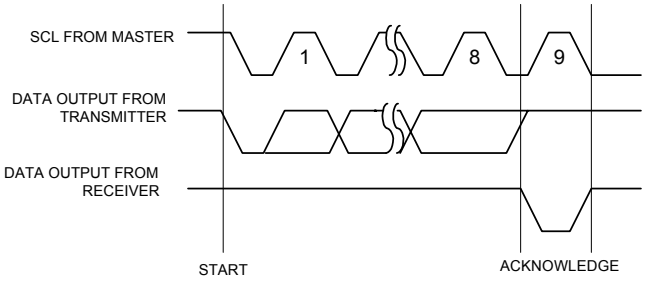


Figure 3. Acknowledge Response from Receiver

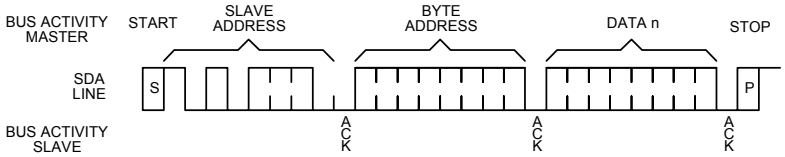


Figure 4. Byte Write for Data

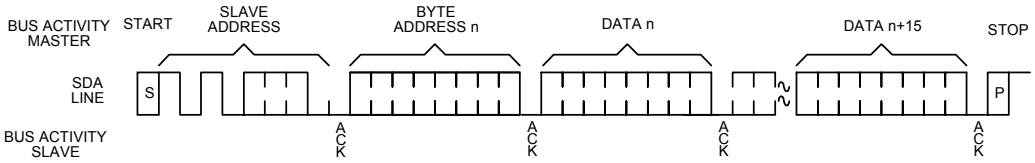


Figure 5. Page Write for Data

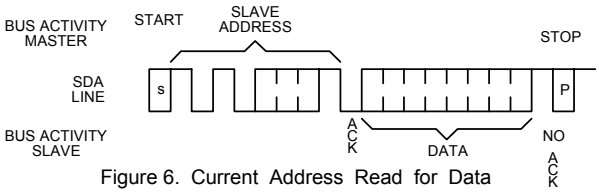


Figure 6. Current Address Read for Data

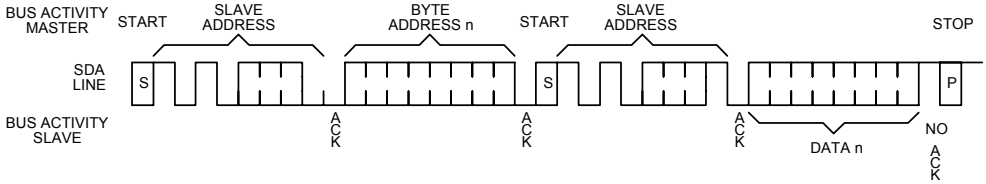


Figure 7. Random Read for Data

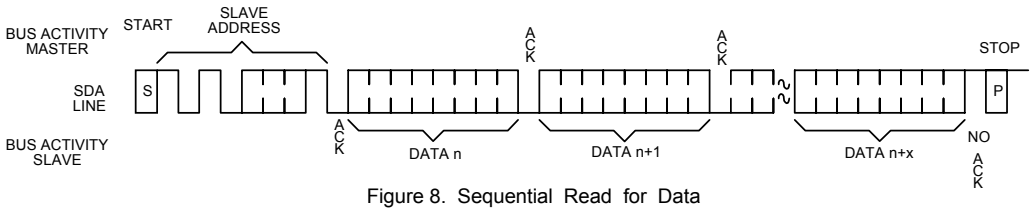
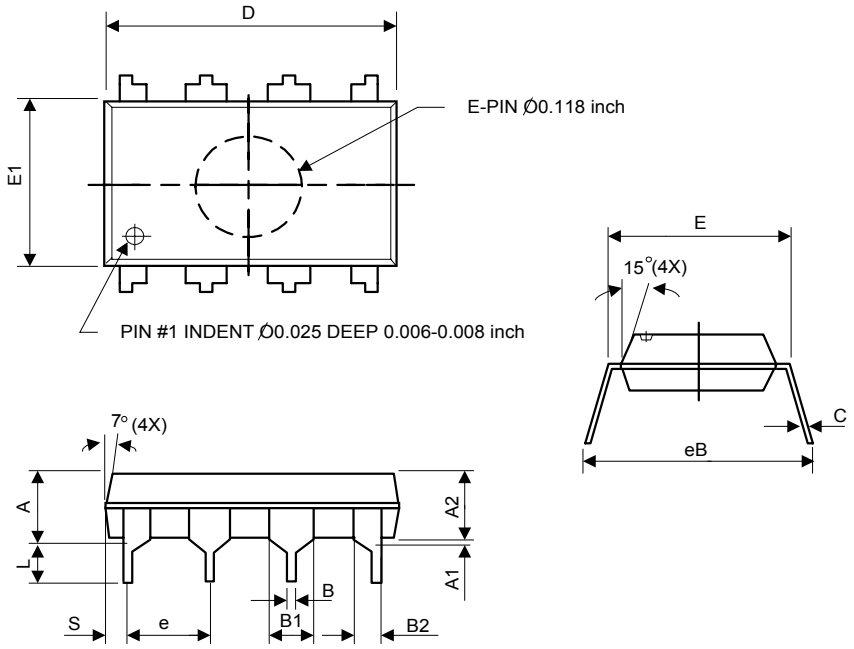


Figure 8. Sequential Read for Data

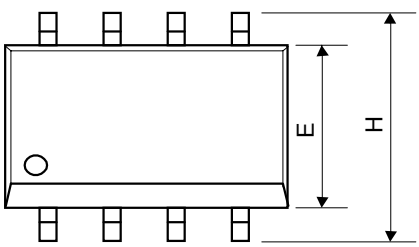
■ Package Information

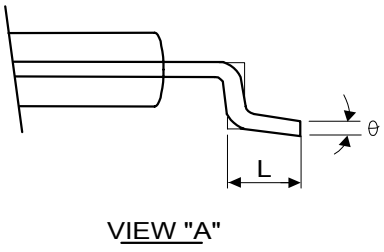
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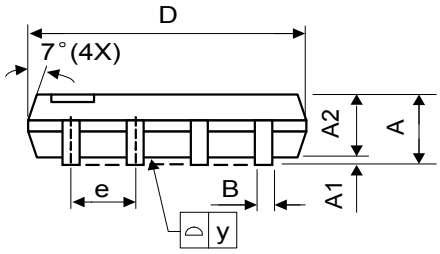


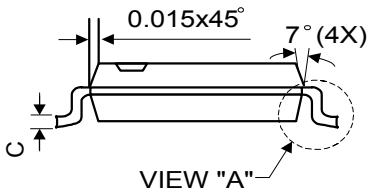
Symbol	Dimensions in millimeters			Dimensions in inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	5.33	-	-	0.210
A1	0.38	-	-	0.015	-	-
A2	3.1	3.30	3.5	0.122	0.130	0.138
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.4	1.52	1.65	0.055	0.060	0.065
B2	0.81	0.99	1.14	0.032	0.039	0.045
C	0.20	0.25	0.36	0.008	0.010	0.014
D	9.02	9.27	9.53	0.355	0.365	0.375
E	7.62	7.94	8.26	0.300	0.313	0.325
E1	6.15	6.35	6.55	0.242	0.250	0.258
e	-	2.54	-	-	0.100	-
L	2.92	3.3	3.81	0.115	0.130	0.150
eB	8.38	8.89	9.40	0.330	0.350	0.370
S	0.71	0.84	0.97	0.028	0.033	0.038

(2)Package Type: SOP-8L



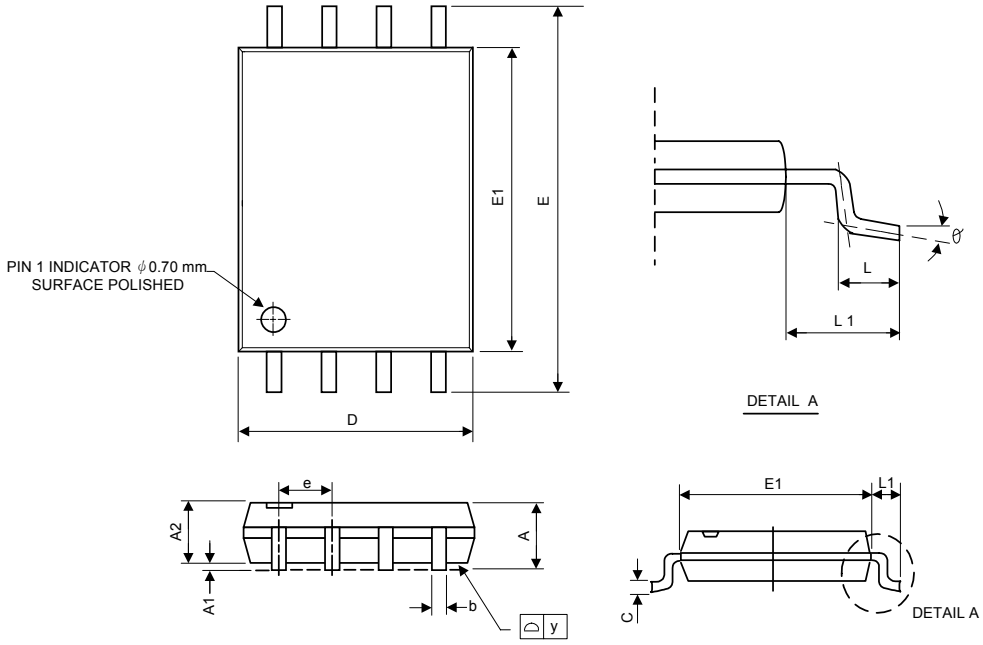






Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0^{O}	-	8^{O}	0^{O}	-	8^{O}

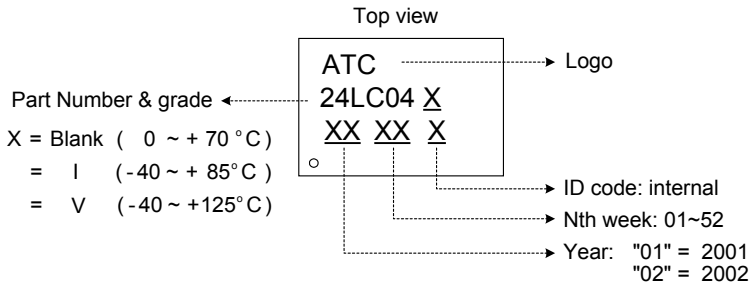
(3)Package Type: TSSOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.05	1.10	1.20	0.041	0.043	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	-	1.00	1.05	-	0.039	0.041
b	0.20	0.25	0.28	0.008	0.01	0.011
C	-	0.13	-	-	0.005	-
D	2.90	3.05	3.10	0.114	0.12	0.122
E	6.20	6.40	6.60	0.244	0.252	0.26
E1	4.30	4.40	4.50	0.169	0.173	0.177
e	-	0.65	-	-	0.026	-
L	0.50	0.60	0.70	0.02	0.024	0.028
L1	0.90	1.00	1.10	0.035	0.039	0.043
y	-	-	0.10	-	-	0.004
θ	0^O	4^O	8^O	0^O	4^O	8^O

■ Marking Information

(1) PDIP /SOP



PDIP/SOP

(2) TSSOP-8L

