

DATA SHEET

74F756

Octal inverter buffer (open-collector)

74F757

Octal buffer (open-collector)

74F760

Octal buffer (open-collector)

Product specification

1989 Nov 27

IC15 Data Handbook

Buffers

74F756/74F757/74F760

74F756 Octal Inverter Buffer (Open Collector)

74F757 Octal Buffer (Open Collector)

74F760 Octal Buffer (Open Collector)

FEATURES

- Octal bus interface
- Open collector versions of 74F240, 74F241 and 74F244

DESCRIPTION

The 74F756, 74F757 and 74F760 are octal buffers that are ideal for driving bus lines of buffer memory address registers. The 74F756 is the open collector version of 74F240, 74F757 is the open collector version of 74F241 and 74F760 is the open collector version of 74F244. These devices feature two Output Enables, $\overline{OE}a$ and $\overline{OE}b$ (or OEb for the 74F757), each controlling four of the outputs.

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F756	9.0ns	40mA
74F757	9.0ns	45mA
74F760	9.0ns	45mA

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PKG DWG #
	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	
20-pin plastic DIP	N74F756N, N74F757AN, N74F760N	SOT146-1
20-pin plastic SOL	N74F756D, N74F757AD, N74F760D	SOT163-1

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
Ian, Ibn	Data inputs	1.0/1.67	20 μ A/1.0mA
$\overline{OE}a$, $\overline{OE}b$	Output enable input (active Low)	1.0/1.67	20 μ A/0.2mA
OEb	Output enable input (active High 74F757)	1.0/1.67	20 μ A/1.0mA
Yan, Ybn	Data outputs (74F757, 74F760)	OC/106.7	OC/64mA
$\overline{Y}an$, $\overline{Y}bn$	Data outputs (74F756)	OC/106.7	OC/64mA

Notes:

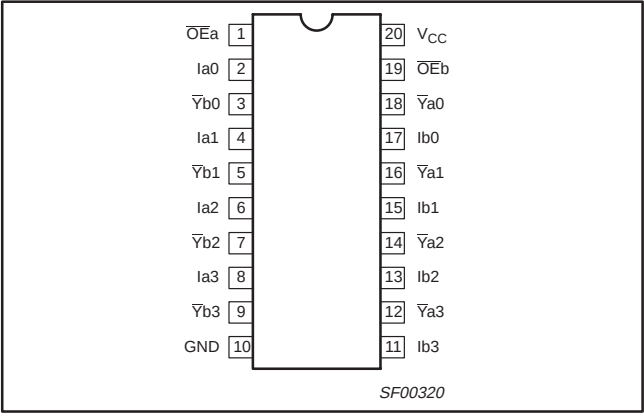
One (1.0) FAST unit load is defined as: 20 μ A in the high state and 0.6mA in the Low state.

OC=Open Collector

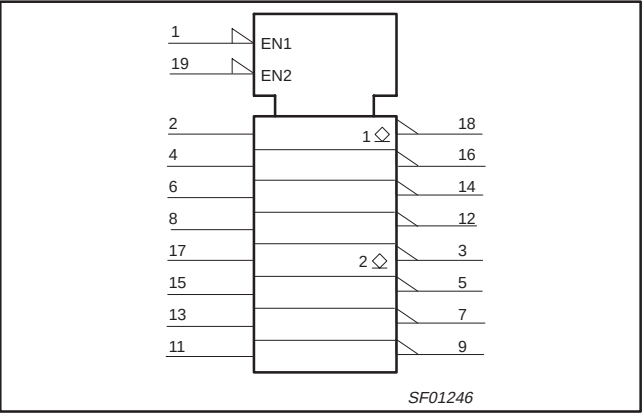
Buffers

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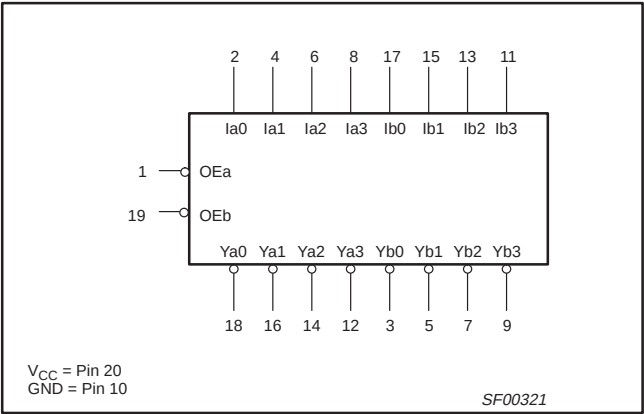
PIN CONFIGURATION for 74F756



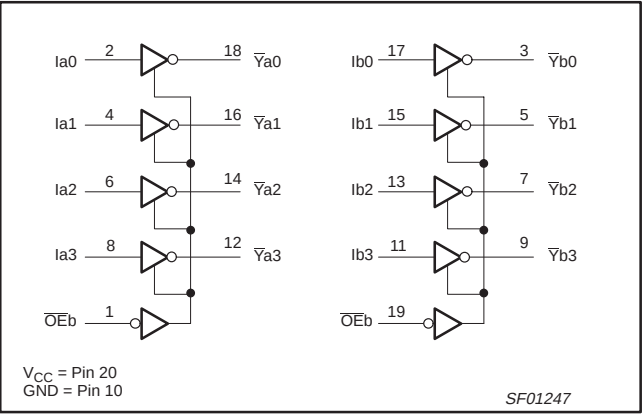
IEC/IEEE SYMBOL for 74F756



LOGIC SYMBOL for 74F756



LOGIC DIAGRAM for 74F756



FUNCTION TABLE for 74F756

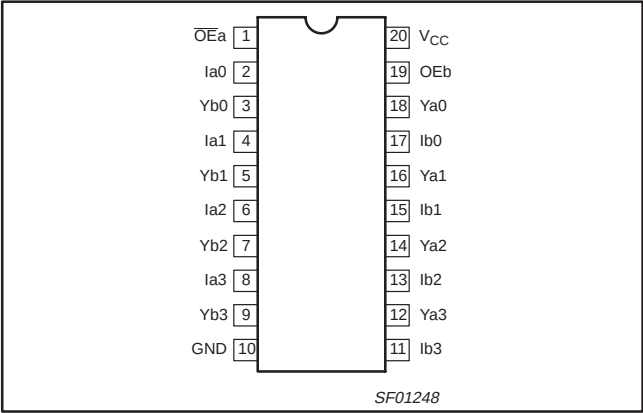
INPUTS				OUTPUTS	
$\overline{OEa}$	Ia	$\overline{OEb}$	Ib	$\overline{Ya}$	$\overline{Yb}$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	H (off)	H (off)

H = High voltage level
L = Low voltage level
X = Don't care

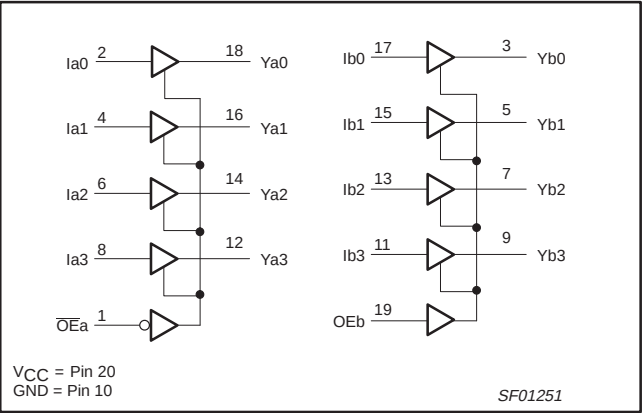
Buffers

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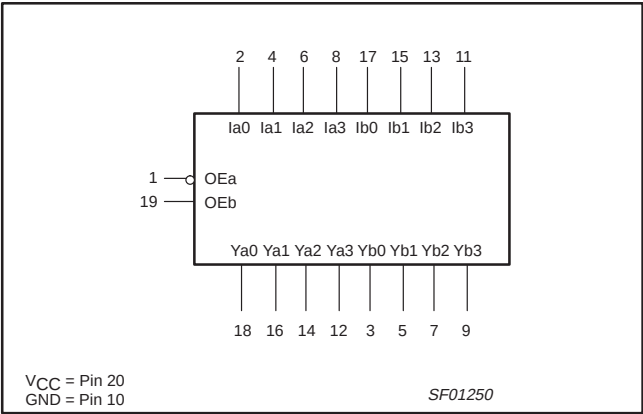
PIN CONFIGURATION for 74F757



LOGIC DIAGRAM for 74F757



LOGIC SYMBOL for 74F757

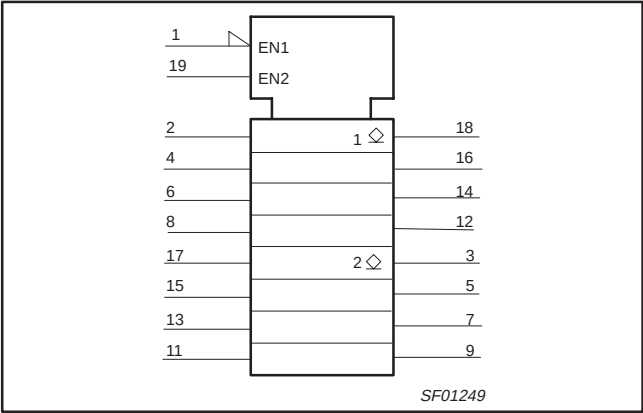


FUNCTION TABLE for 74F757

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	OEb	Ib	Ya	Yb
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	H (off)	H (off)

H = High voltage level
L = Low voltage level
X = Don't care

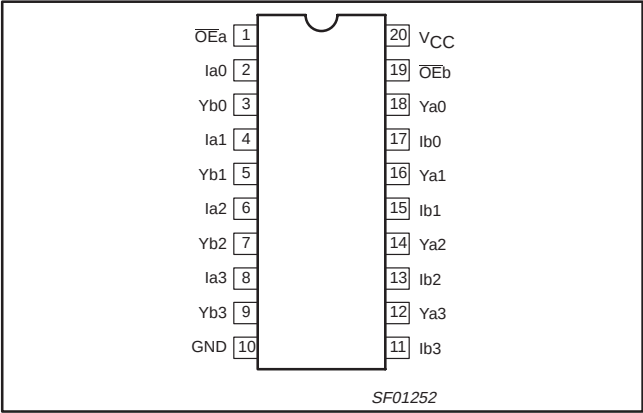
IEC/IEEE SYMBOL for 74F757



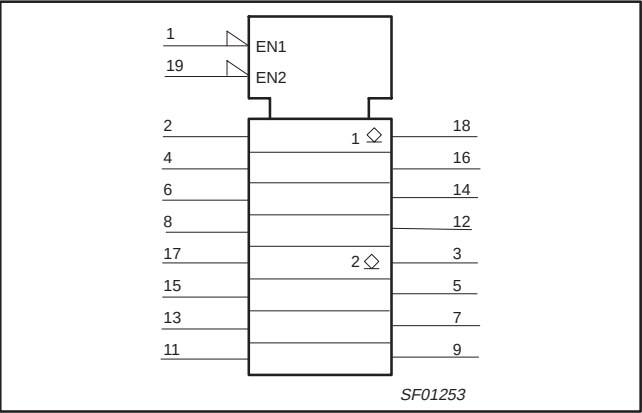
Buffers

74F756/74F757/74F760

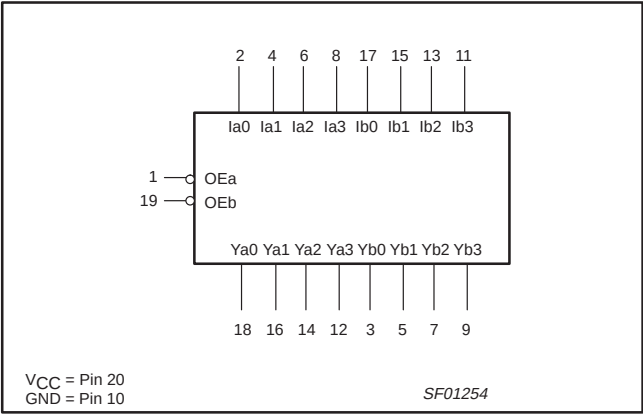
PIN CONFIGURATION for 74F760



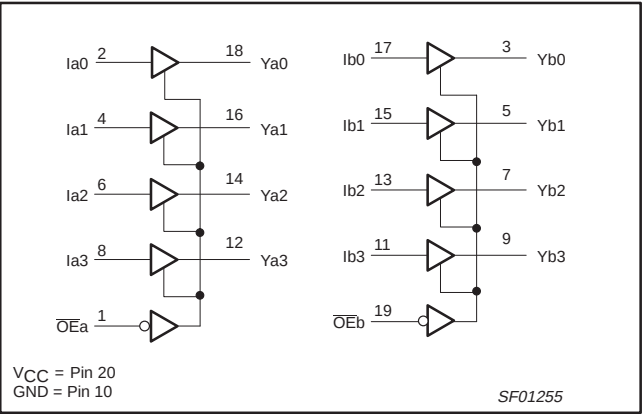
IEC/IEEE SYMBOL for 74F760



LOGIC SYMBOL for 74F760



LOGIC DIAGRAM for 74F760



FUNCTION TABLE for 74F760

INPUTS				OUTPUTS	
$\overline{OE}a$	Ia	$\overline{OE}b$	Ib	Ya	Yb
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	H (off)	H (off)

H = High voltage level
L = Low voltage level
X = Don't care

Buffers

74F756/74F757/74F760

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device.)

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	−0.5 to +7.0	V
V_{IN}	Input voltage	−0.5 to +7.0	V
I_{IN}	Input current	−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	−0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	128	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			−18	mA
V_{OH}	High-level output voltage			4.5	V
I_{OL}	Low-level output current			64	mA
T_{amb}	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER			TEST CONDITIONS ¹	LIMITS			UNIT
					MIN	TYP ²	MAX	
I_{OH}	High-level output current			$V_{CC} = \text{MIN}, V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN}, V_{OH} = \text{MAX}$			250	μA
V_{OL}	Low-level output voltage			$V_{CC} = \text{MIN},$ $V_{IL} = \text{MAX},$ $V_{IH} = \text{MIN},$ $I_{OL} = 48\text{MAX}$	$\pm 10\%V_{CC}$	0.38	0.55	V
				$I_{OL} = 64\text{mA}$	$\pm 5\%V_{CC}$	0.42	0.55	V
V_{IK}	Input clamp voltage			$V_{CC} = \text{MIN}, I_I = I_{IK}$		−0.73	−1.2	V
I_I	Input current at maximum input voltage			$V_{CC} = \text{MAX}, V_I = 7.0\text{V}$			100	μA
I_{IH}	High-level input current			$V_{CC} = \text{MAX}, V_I = 2.7\text{V}$			20	μA
I_{IL}	Low-level input current			$V_{CC} = \text{MAX}, V_I = 0.5\text{V}$			−1.0	mA
I_{CC}	Supply current (total)	74F756	I_{CCH}	$V_{CC} = \text{MAX}$		20	30	mA
			I_{CCL}			50	70	mA
		74F757	I_{CCH}			30	40	mA
			I_{CCL}			55	80	mA
		74F760	I_{CCH}			25	37	mA
			I_{CCL}			55	80	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.

Buffers

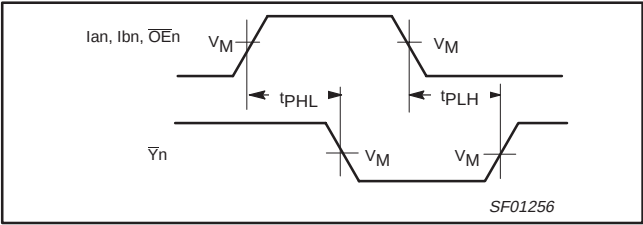
74F756/74F757/74F760

AC ELECTRICAL CHARACTERISTICS

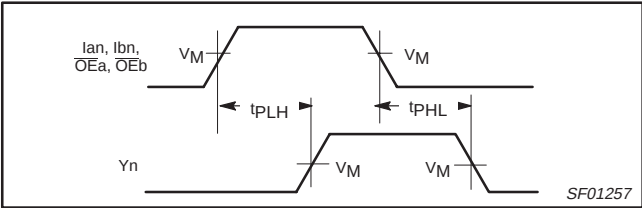
SYMBOL	PARAMETER		TEST CONDITION	LIMITS						UNIT
				T _{amb} = +25°C V _{CC} = +5.0V C _L = 50pF, R _L = 500Ω			T _{amb} = 0°C to +70°C V _{CC} = +5.0V ± 10% C _L = 50pF, R _L = 500Ω			
				MIN	TYP	MAX	MIN	MAX		
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to $\bar{Y}_n$	74F756	Waveform 1, 2	8.5 1.0	11.0 3.0	14.0 6.0	8.5 1.0	15.0 6.5	ns	
t _{PLH} t _{PHL}	Propagation delay $\bar{O}E_n$ to $\bar{Y}_n$		Waveform 1, 2	9.0 5.0	11.5 7.0	14.5 10.0	9.0 4.5	15.0 10.5	ns	
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to Y _n	74F757	Waveform 1, 2	7.5 3.0	10.5 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns	
t _{PLH} t _{PHL}	Propagation delay $\bar{O}E_a$ or $\bar{O}E_b$ to Y _n		Waveform 1, 2	9.0 4.5	10.5 7.0	15.0 10.0	8.5 4.0	16.0 10.5	ns	
t _{PLH} t _{PHL}	Propagation delay I _{an} , I _{bn} to Y _n	74F760	Waveform 1, 2	7.5 3.5	10.0 5.5	13.5 8.5	7.5 3.0	14.0 9.0	ns	
t _{PLH} t _{PHL}	Propagation delay $\bar{O}E_n$ to Y _n		Waveform 1, 2	9.5 5.0	11.5 7.0	14.5 10.5	9.0 4.5	15.0 10.5	ns	

AC WAVEFORMS

For all waveforms, V_M = 1.5V.

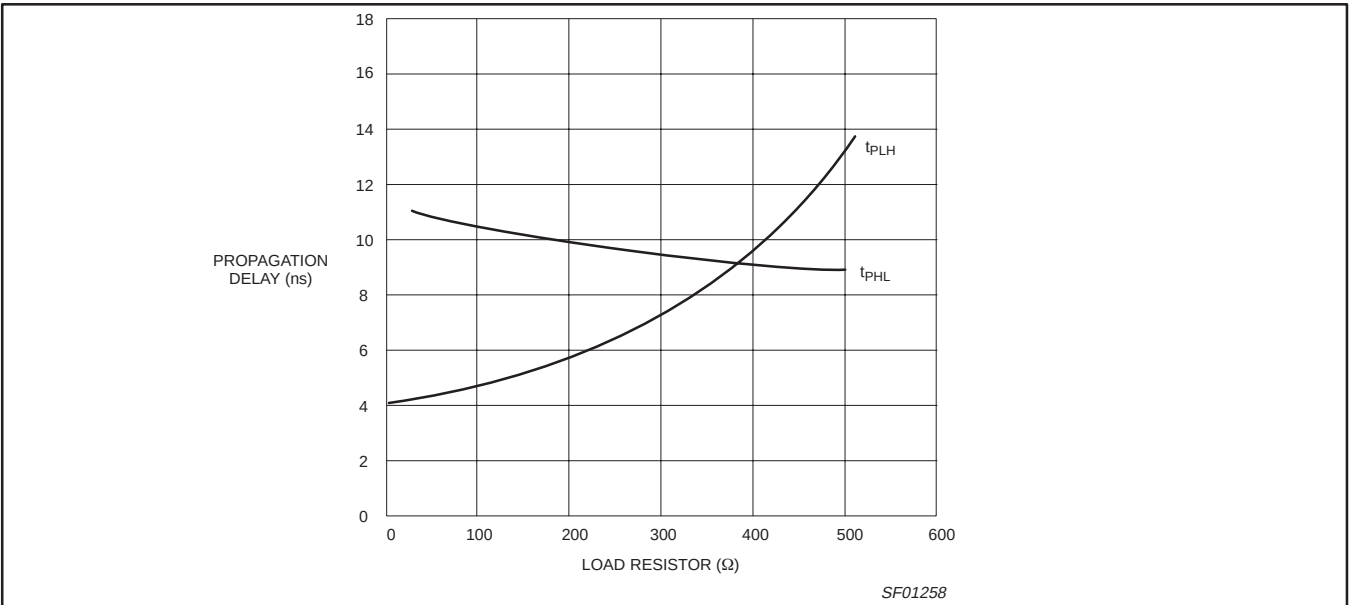


Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-inverting Outputs

TYPICAL PROPAGATION DELAYS VERSUS LOAD FOR OPEN COLLECTOR OUTPUTS

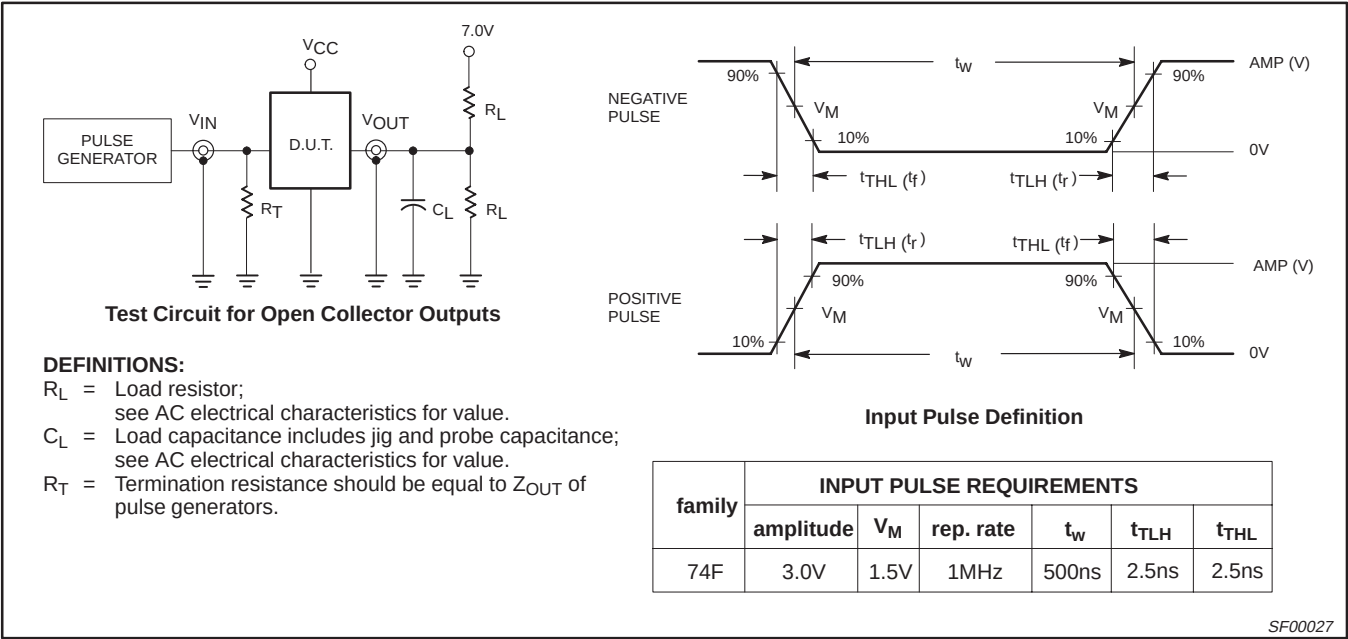


NOTE:
When using open-collector parts, the value of the pull-up resistor greatly affects the value of the t_{PLH}. For example, changing the pull-up resistor value from 500Ω to 100Ω will improve the t_{PLH} up to 50% with only slight increase in the t_{PHL}. However, if the pull-up resistor is changed, the user must make certain that the total I_{OL} current through the resistor and the total I_{IL}'s of the receivers do not exceed the I_{OL} maximum specification.

Buffers

74F756/74F757/74F760

TEST CIRCUIT AND WAVEFORMS

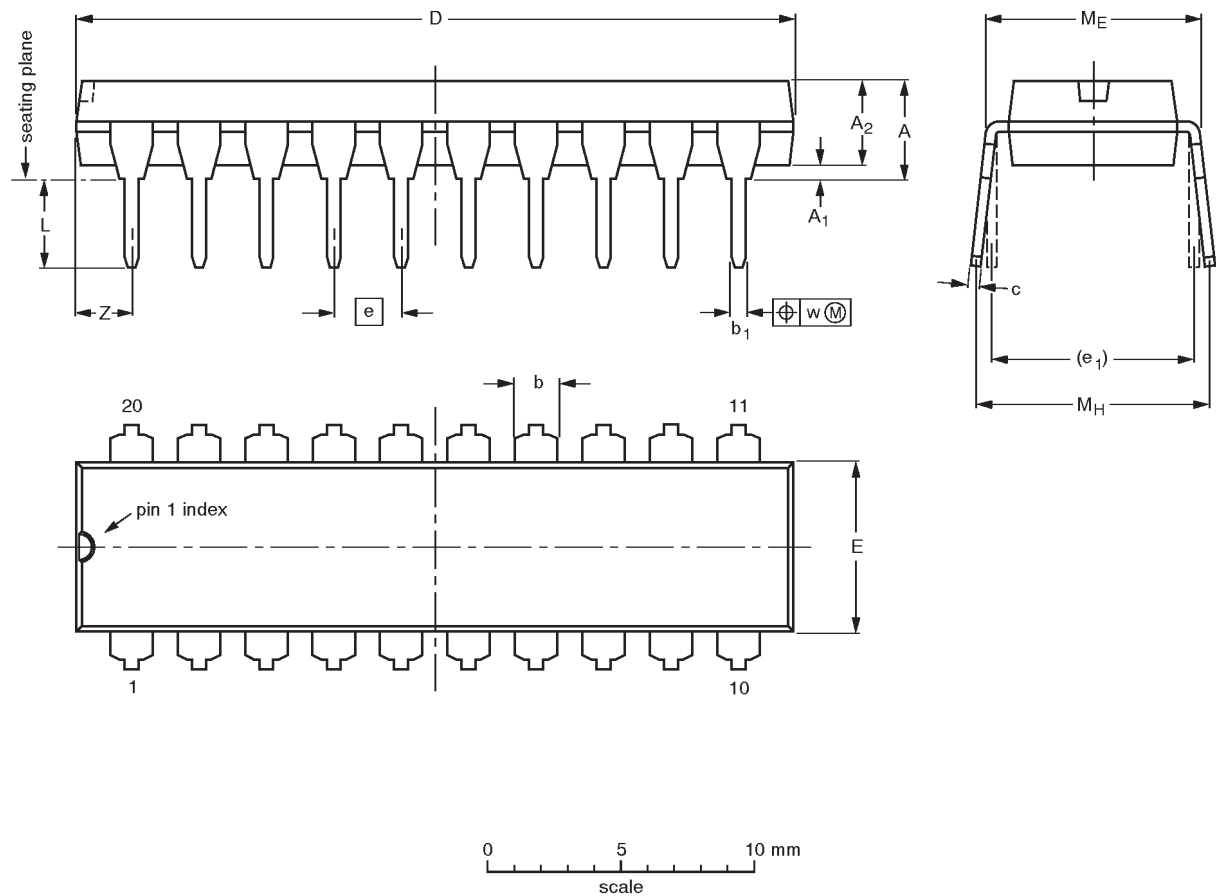


Buffers

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DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	c	D ⁽¹⁾	E ⁽¹⁾	e	e ₁	L	M _E	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

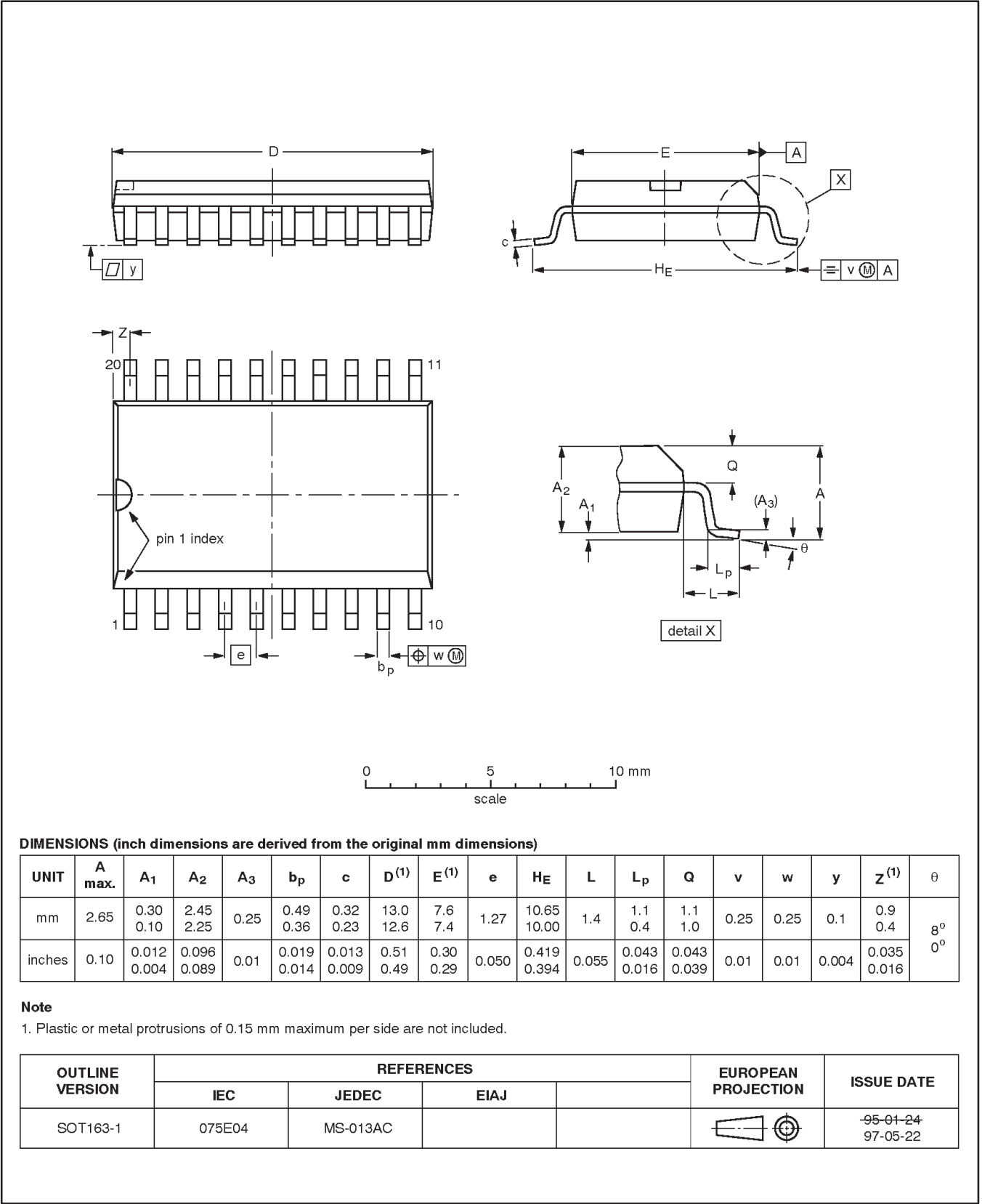
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

Buffers

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

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NOTES

Buffers

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Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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