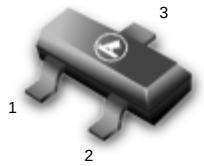
12V P-Channel Enhancement-Mode MOSFET

LP2305DSLT1G
S-LP2305DSLT1G

V_{DS}= -12V

$R_{DS(ON)}$, Vgs@-4.5V, Ids@±3.5A = 68 mΩ
$R_{DS(ON)}$, Vgs@-2.5V, Ids@±3A = 81 mΩ
$R_{DS(ON)}$, Vgs@-1.8V, Ids@±2A = 118 mΩ



SOT– 23 (TO–236AB)

Features

Advanced trench process technology

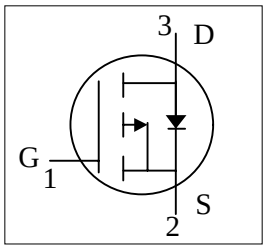
High Density Cell Design For Ultra Low On-Resistance

Fully Characterized Avalanche Voltage and Current

Improved Shoot-Through FOM

we declare that the material of product compliance with RoHS requirements.

S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



▼ Simple Drive Requirement

▼ Small Package Outline

▼ Surface Mount Device

Ordering Information

Device	Marking	Shipping
LP2305DSLT1G S-LP2305DSLT1G	P5S	3000/Tape&Reel
LP2305DSLT3G S-LP2305DSLT3G	P5S	10000/Tape&Reel

Maximum Ratings and Thermal Characteristics (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	- 12	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current	I_D	-4	A
Pulsed Drain Current [1)]	I_{DM}	-12	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	°C
Total Device Dissipation FR–5 Board T_A = 25°C	P_D	1100	mW

Note: 1. Repetitive Rating: Pulse width limited by the maximum junction temperature

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-a	Thermal Resistance Junction-ambient[3]	110	℃/W

LP2305DSLT1G , S-LP2305DSLT1G

ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static [1]						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = -250uA	- 12			V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -4.5V, I_D = -3.5A		47.0	68.0	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -2.5V, I_D = -3A		55.0	81.0	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = -1.8V, I_D = -2A		67.0	118.0	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = -250uA	-0.4		-0.9	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -6.4V, V_{GS} = 0V			1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ± 8V, V_{DS} = 0V			±100	nA
Forward Transconductance	g_{fs}	V_{DS} = -5V, I_D = -3.5A		8.5		S
On-State Drain Current [2]	$I_{D(on)}$	$V_{DS} \leq -5$ V, V_{GS} = –4.5 V	–6			A
		$V_{DS} \leq -5$ V, V_{GS} = –2.5 V	–3			
Source-Drain Diode						
Max. Diode Forward Current	I_S			–1.6		A
Diode Forward Voltage	V_{SD}	I_S = -1.6A, V_{GS} = 0V			-1.2	V
Dynamic [3]						
Input Capacitance	C_{iss}	V_{DS} = –4 V, V_{GS} = 0, f = 1MHZ		1245		pF
Output Capacitance	C_{oss}			375		
Reverse Transfer Capacitance	C_{rss}			210		
Switching [3]						
Turn-On Time	$t_{d(on)}$	V_{DD} = –4 V, R_L = 4 Ω I_D = –1.0 A, V_{GEN} = –4.5 V R_G = 6 Ω		13	20	ns
	t_r			25	40	
Turn-Off Time	$t_{d(off)}$			55	80	
	t_f			19	35	

Note: 1. Static parameters are based on package level with recommended wire-bonding
2.For DESIGN AID ONLY, not subject to production testing.
3.Pulse test: PW ≤300 μs duty cycle ≤2%.

LP2305DSLT1G , S-LP2305DSLT1G

TYPICAL ELECTRICAL CHARACTERISTICS

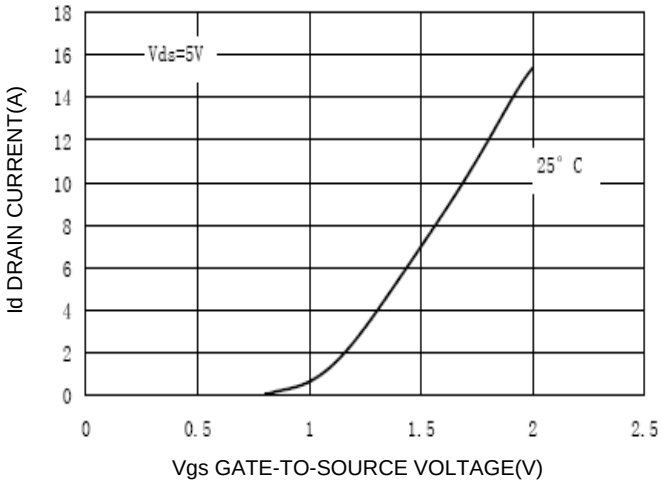


Figure 1. Transfer Characteristics

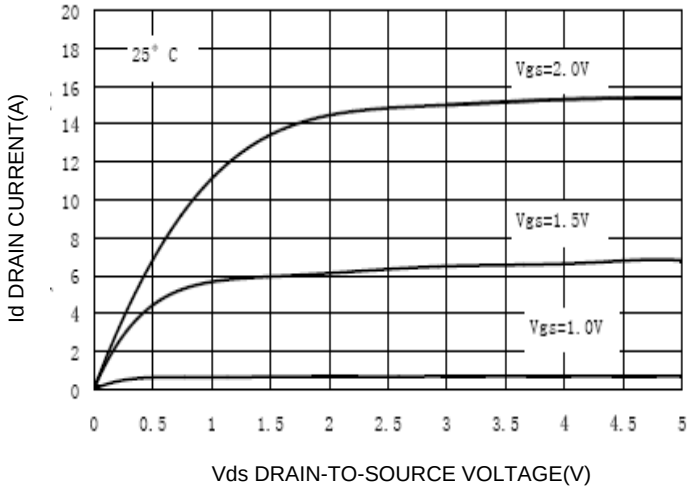


Figure 2. On–Region Characteristics

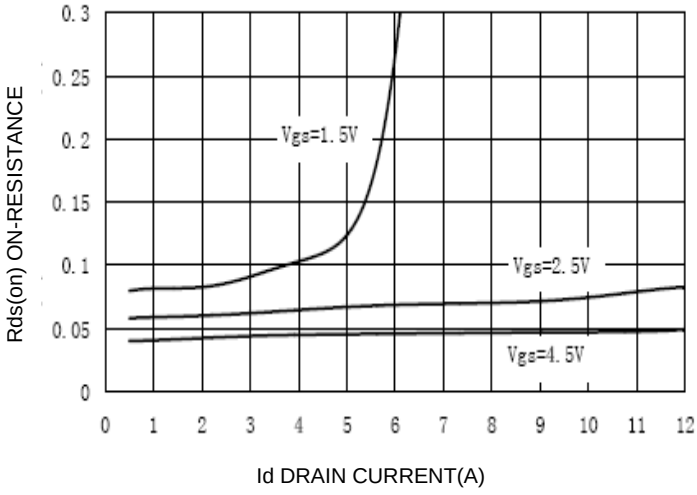


Figure 3. On–Resistance versus Drain Current

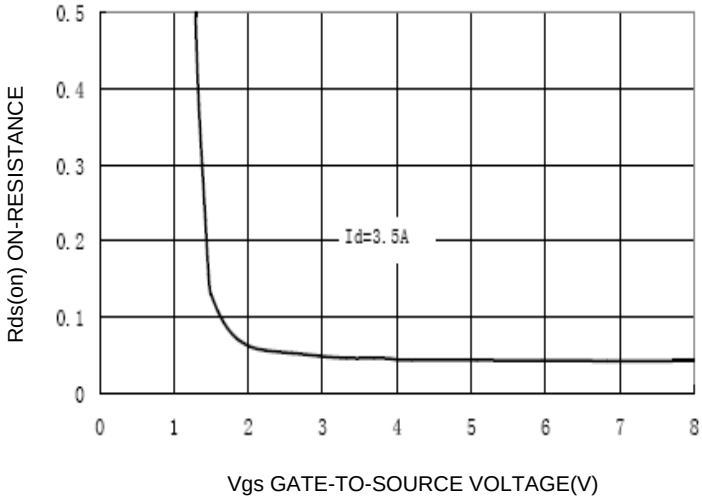


Figure 4. On-Resistance vs. Gate-to-Source Voltage

LP2305DSLT1G , S-LP2305DSLT1G

TYPICAL ELECTRICAL CHARACTERISTICS

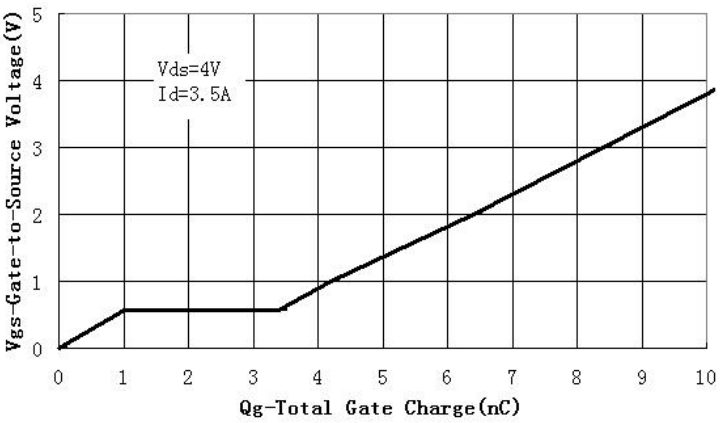


Figure 5. Gate Charge

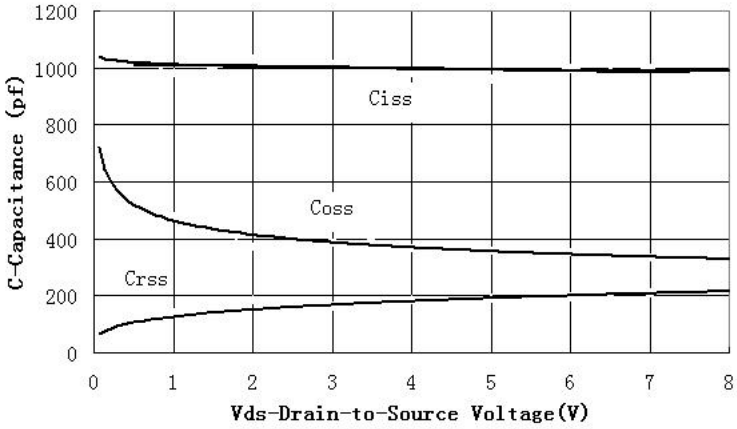


Figure 6. Capacitance

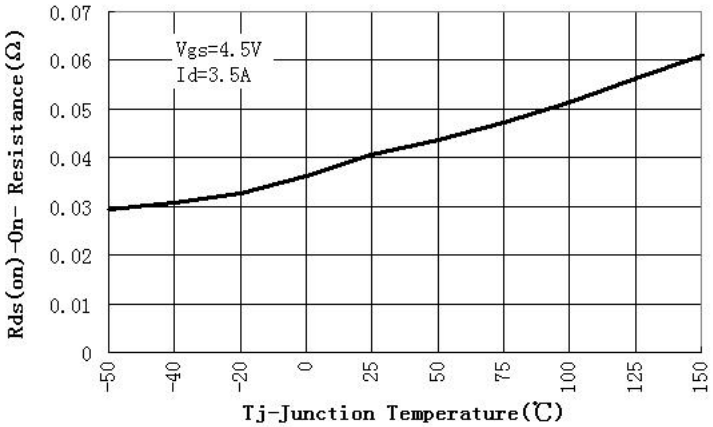
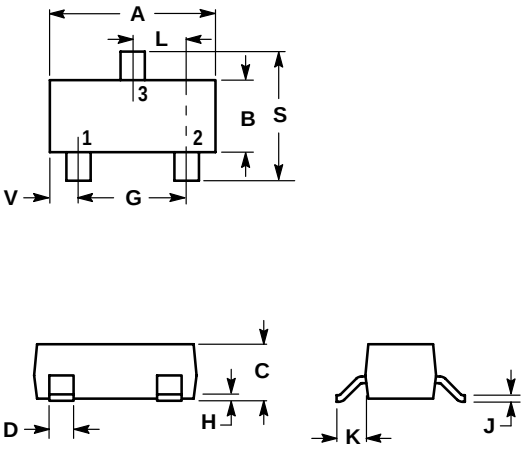


Figure 7. On-Resistance Vs.Junction Temperature

LP2305DSLT1G , S-LP2305DSLT1G

SOT–23



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M,1982
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.1102	0.1197	2.80	3.04
B	0.0472	0.0551	1.20	1.40
C	0.0350	0.0440	0.89	1.11
D	0.0150	0.0200	0.37	0.50
G	0.0701	0.0807	1.78	2.04
H	0.0005	0.0040	0.013	0.100
J	0.0034	0.0070	0.085	0.177
K	0.0140	0.0285	0.35	0.69
L	0.0350	0.0401	0.89	1.02
S	0.0830	0.1039	2.10	2.64
V	0.0177	0.0236	0.45	0.60