

CMLDM8005**SURFACE MOUNT
DUAL P-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFETS****PICOmini™****SOT-563 CASE**www.centrasemi.com**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CMLDM8005 consists of Dual P-Channel Enhancement-mode silicon MOSFETs designed for high speed pulsed amplifier and driver applications. These MOSFETs offer Very Low $r_{DS(ON)}$ and Low Threshold Voltage.

MARKING CODE: CC8**FEATURES:**

- ESD Protection up to 2kV
- 350mW Power Dissipation
- Very Low $r_{DS(ON)}$
- Low Threshold Voltage
- Logic Level Compatible
- Small, SOT-563 Surface Mount Package
- Complementary Dual N-Channel Device: CMLDM7005

APPLICATIONS:

- Load Switch / Level Shifting
- Battery Charging
- Boost Switch
- Electro-luminescent Backlighting

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Drain-Source Voltage	
Gate-Source Voltage	
Continuous Drain Current (Steady State - Note 1)	
Continuous Source Current (Body Diode)	
Maximum Pulsed Drain Current	
Power Dissipation (Note 1)	
Power Dissipation (Note 2)	
Power Dissipation (Note 2)	
Operating and Storage Junction Temperature	
Thermal Resistance (Note 1)	

SYMBOL

V_{DS}	20	V
V_{GS}	8.0	V
I_D	650	mA
I_S	250	mA
I_{DM}	1.0	A
P_D	350	mW
P_D	300	mW
P_D	150	mW
T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
Θ_{JA}	357	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=4.5\text{V}, V_{DS}=0$			10	μA
I_{DSS}	$V_{DS}=16\text{V}, V_{GS}=0$			100	nA
BV_{DSS}	$V_{GS}=0, I_D=250\mu\text{A}$	20			V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	0.5		1.0	V
V_{SD}	$V_{GS}=0, I_S=250\text{mA}$			1.1	V
$r_{DS(ON)}$	$V_{GS}=4.5\text{V}, I_D=350\text{mA}$		0.25	0.36	Ω
$r_{DS(ON)}$	$V_{GS}=2.5\text{V}, I_D=300\text{mA}$		0.37	0.5	Ω
$r_{DS(ON)}$	$V_{GS}=1.8\text{V}, I_D=150\text{mA}$			0.8	Ω

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0mm^2

(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0mm^2

(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4mm^2

R3 (27-September 2011)

CMLDM8005

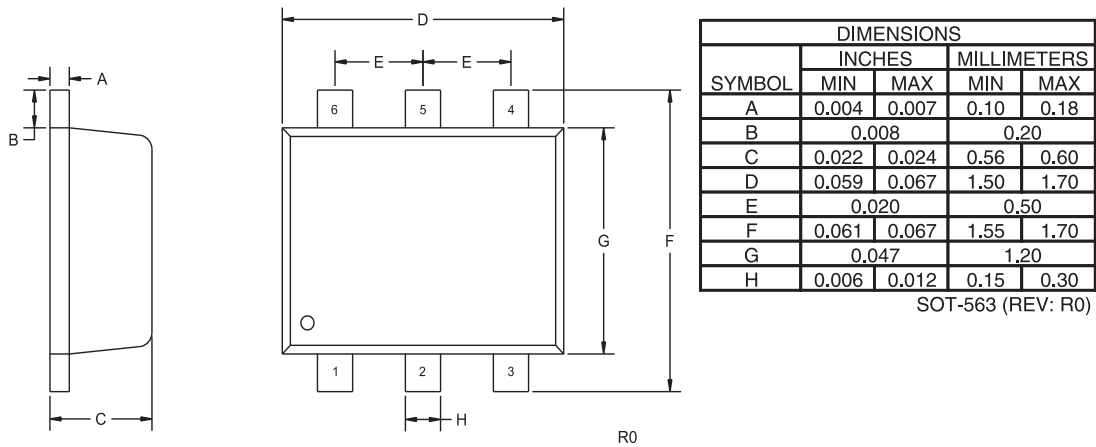
**SURFACE MOUNT
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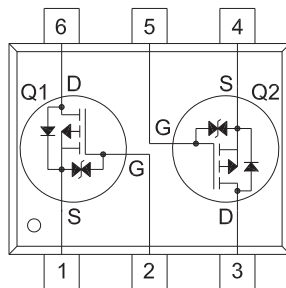
ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	UNITS
$Q_{g(\text{tot})}$	$V_{DS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=200\text{mA}$		1.2	nC
Q_{gs}	$V_{DS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=200\text{mA}$		0.24	nC
Q_{gd}	$V_{DS}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=200\text{mA}$		0.36	nC
g_{FS}	$V_{DS}=10\text{V}$, $I_D=200\text{mA}$	0.2		S
C_{rss}	$V_{DS}=16\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		25	pF
C_{iss}	$V_{DS}=16\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		100	pF
C_{oss}	$V_{DS}=16\text{V}$, $V_{GS}=0$, $f=1.0\text{MHz}$		21	pF
t_{on}	$V_{DD}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=200\text{mA}$, $R_G=10\Omega$		38	ns
t_{off}	$V_{DD}=10\text{V}$, $V_{GS}=4.5\text{V}$, $I_D=200\text{mA}$, $R_G=10\Omega$		48	ns

SOT-563 CASE - MECHANICAL OUTLINE



PIN CONFIGURATION



LEAD CODE:

- 1) Source Q1
- 2) Gate Q1
- 3) Drain Q2
- 4) Source Q2
- 5) Gate Q2
- 6) Drain Q1

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