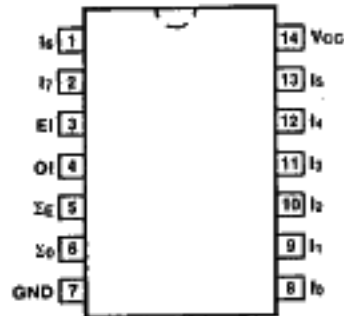


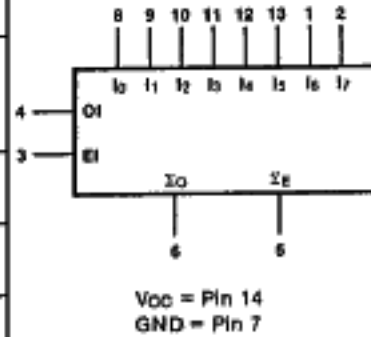
# 54/74180

## 8-BIT PARITY GENERATOR/CHECKER

### CONNECTION DIAGRAM PINOUT A



### LOGIC SYMBOL



**DESCRIPTION**—The '180 is a monolithic, 8-bit parity checker/generator which features control inputs and even/odd outputs to enhance operation in either odd or even parity applications. Cascading these circuits allows unlimited word length expansion. Typical application would be to generate and check parity on data being transmitted from one register to another. Typical power dissipation is 170 mW.

**ORDERING CODE:** See Section 9

| PKGS            | PIN OUT | COMMERCIAL GRADE  | MILITARY GRADE   | PKG TYPE |
|-----------------|---------|---|--|----------|
|                 |         | V <sub>CC</sub> = +5.0 V, ±5%,<br>T <sub>A</sub> = 0°C to +70°C | V <sub>CC</sub> = +5.0 V ±10%,<br>T <sub>A</sub> = -55°C to +125°C |          |
| Plastic DIP (P) | A       | 74180PC   |  | 9A       |
| Ceramic DIP (D) | A       | 74180DC   | 54180DM  | 6A       |
| Flatpak (F)     | A       | 74180FC   | 54180FM  | 3I       |

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

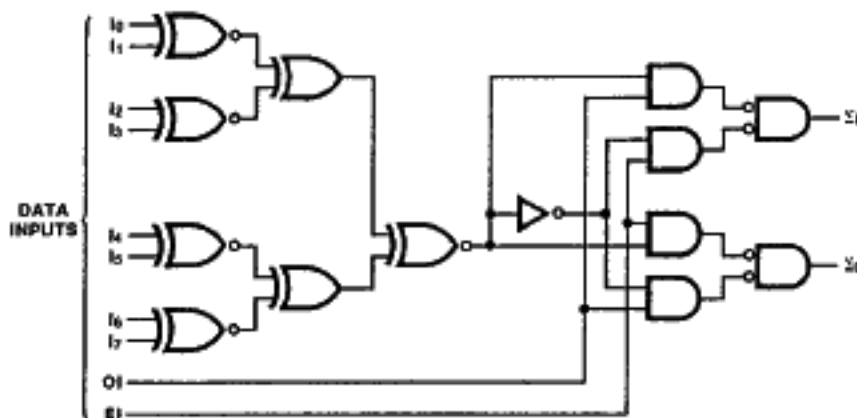
| PIN NAMES                       | DESCRIPTION        | 54/74 (U.L.) HIGH/LOW |
|---------------------------------|--------------------|-----------------------|
| I <sub>0</sub> — I <sub>7</sub> | Data Inputs        | 1.0/1.0               |
| O <sub>i</sub>                  | Odd Input          | 2.0/2.0               |
| E <sub>i</sub>                  | Even Input         | 2.0/2.0               |
| Σ <sub>O</sub>                  | Odd Parity Output  | 20/10                 |
| Σ <sub>E</sub>                  | Even Parity Output | 20/10                 |

### TRUTH TABLE

| Σ OF 1's AT 0 THRU 7 | INPUTS |     | OUTPUTS |       |
|----------------------|--------|-----|---------|-------|
|                      | EVEN   | ODD | Σ EVEN  | Σ ODD |
| EVEN                 | H      | L   | H       | L     |
| ODD                  | H      | L   | L       | H     |
| EVEN                 | L      | H   | L       | H     |
| ODD                  | L      | H   | H       | L     |
| X                    | H      | H   | L       | L     |
| X                    | L      | L   | H       | H     |

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| SYMBOL          | PARAMETER                    | 54/74 |     | UNITS | CONDITIONS |  |
|-----------------|------------------------------|-------|-----|-------|------------|--|
|                 |                              | Min   | Max |       |            |  |
| I <sub>os</sub> | Output Short Circuit Current | XM    | -20 | -55   | mA         | V <sub>CC</sub> = Max  |
|                 |                              | XC    | -18 | -55   |            |  |
| I <sub>cc</sub> | Power Supply Current         | XM    | 49  |       | mA         | V <sub>CC</sub> = Max, I <sub>n</sub> = Open<br>OI, EI = 4.5 V |
|                 |                              | XC    | 56  |       |            |  |

AC CHARACTERISTICS: V<sub>CC</sub> = +5.0 V, T<sub>A</sub> = +25°C (See Section 3 for waveforms and load configurations)

| SYMBOL                               | PARAMETER                                 | 54/74  |          | UNITS | CONDITIONS                 |
|--------------------------------------|---|--|----------|-------|----------------------------|
|                                      |   | C <sub>L</sub> = 15 pF<br>R <sub>L</sub> = 400 Ω |          |       |                            |
|                                      |   | Min  | Max      |       |                            |
| I <sub>PLH</sub><br>I <sub>PHL</sub> | Propagation Delay<br>I <sub>n</sub> to ΣE |  | 60<br>68 | ns    | Figs. 3-1, 3-5<br>OI = Gnd |
| I <sub>PLH</sub><br>I <sub>PHL</sub> | Propagation Delay<br>I <sub>n</sub> to ΣO |  | 48<br>38 | ns    | Figs. 3-1, 3-4<br>OI = Gnd |
| I <sub>PLH</sub><br>I <sub>PHL</sub> | Propagation Delay<br>I <sub>n</sub> to ΣE |  | 48<br>38 | ns    | Figs. 3-1, 3-5<br>EI = Gnd |
| I <sub>PLH</sub><br>I <sub>PHL</sub> | Propagation Delay<br>I <sub>n</sub> to ΣO |  | 60<br>68 | ns    | Figs. 3-1, 3-4<br>EI = Gnd |
| I <sub>PLH</sub><br>I <sub>PHL</sub> | Propagation Delay<br>EI or OI to ΣE       |  | 20<br>10 | ns    | Figs. 3-1, 3-5             |
| I <sub>PLH</sub><br>I <sub>PHL</sub> | Propagation Delay<br>EI or OI to ΣO       |  | 20<br>10 | ns    | Figs. 3-1, 3-4             |