



U74AHC00

CMOS IC

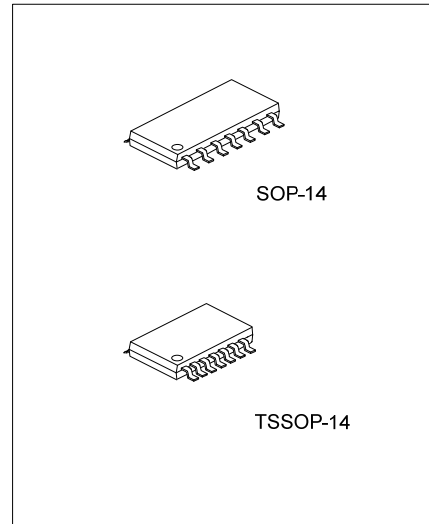
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

DESCRIPTION

The **U74AHC00** is QUADRUPLE 2-INPUT POSITIVE-NAND GATES. Which provides the function $Y = \overline{A \cdot B}$.

FEATURES

- * Operation voltage range: 2~5.5V
- * Max t_{pd} of 6.5 ns at 5 V
- * Low power consumption, 20-uA Max I_{CC}
- * $\pm 8mA$ output drive at 5 V



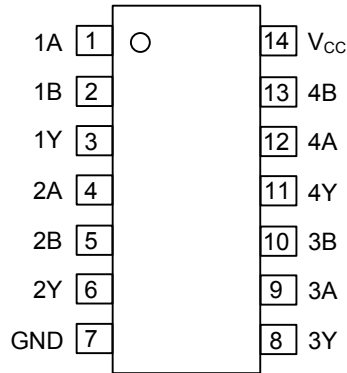
*Pb-free plating product number:
U74AHC00L

ORDERING INFORMATION

Ordering Number		Package	Packing
Normal	Lead Free Plating		
U74AHC00-S14-R	U74AHC00L-S14-R	SOP-14	Tape Reel
U74AHC00-S14-T	U74AHC00L-S14-T	SOP-14	Tube
U74AHC00-P14-R	U74AHC00L-P14-R	TSSOP-14	Tape Reel
U74AHC00-P14-T	U74AHC00L-P14-T	TSSOP-14	Tube

<p>U74AHC00L-S14-R</p> <p>(1) Packing Type (2) Package Type (3) Lead Plating</p>	<p>(1) R: Tape Reel, T: Tube (2) S14: SOP-14, P14: TSSOP-14 (3) L: Lead Free Plating, Blank: Pb/Sn</p>
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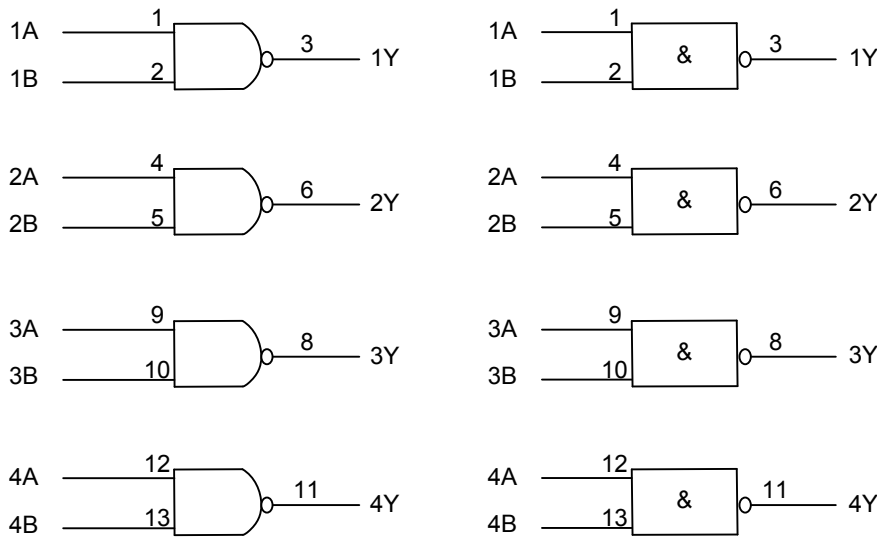
■ PIN CONFIGURATION



■ FUNCTION TABLE (each gate)

INPUT(A)	INPUT(B)	OUTPUT(Y)
L	L	H
L	H	H
H	L	H
H	H	L

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7	V
Input Voltage	V_{IN}	-0.5~7	V
Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Clamp Current	I_{IK}	-20	mA
Output Clamp Current	I_{OK}	±20	mA
Output Current	I_{OUT}	±25	mA
V_{CC} or GND Current	I_{CC}	±50	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2		5.5	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	t_R, t_F	$V_{CC}=3.3\pm 0.3V$			100	ns/V
		$V_{CC}=5.0\pm 0.5V$			20	
Operating Temperature	T_A		-40		85	°C

■ STATIC CHARACTERISTICS ($T_A=25^\circ C$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=2.0V$	1.5			V
		$V_{CC}=3.0V$	2.1			
		$V_{CC}=5.5V$	3.85			
Low-Level Input Voltage	V_{IL}	$V_{CC}=2.0V$			0.5	V
		$V_{CC}=3.0V$			0.9	
		$V_{CC}=5.5V$			1.65	
High-Level Output Voltage	V_{OH}	$V_{CC}=2.0V, I_{OH}=-50\mu A$	1.9	2.0		V
		$V_{CC}=3.0V, I_{OH}=-50\mu A$	2.9	3.0		
		$V_{CC}=4.5V, I_{OH}=-50\mu A$	4.4	4.5		
		$V_{CC}=3.0V, I_{OH}=-4mA$	2.58			
		$V_{CC}=4.5V, I_{OH}=-8mA$	3.94			
Low-Level Output Voltage	V_{OL}	$V_{CC}=2.0V, I_{OL}=50\mu A$			0.1	V
		$V_{CC}=3.0V, I_{OL}=50\mu A$			0.1	
		$V_{CC}=4.5V, I_{OL}=50\mu A$			0.1	
		$V_{CC}=3.0V, I_{OL}=4mA$			0.36	
		$V_{CC}=4.5V, I_{OL}=8mA$			0.36	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=0\sim 5.5V, V_{IN}=5.5$ or GND			±0.1	μA
Quiescent Supply Current	I_Q	$V_{CC}=5.5V, V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			2	μA
Input Capacitance	C_{IN}	$V_{CC}=5.0V, V_{IN}=V_{CC}$ or GND		2	10	pF

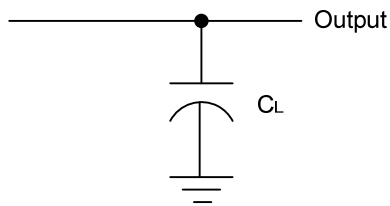
■ DYNAMIC CHARACTERISTICS ($T_A=25^\circ\text{C}$) (Input: $t_R, t_F \leq 3\text{ns}$; $\text{PRR} \leq 1\text{MHz}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay from Input (A and B) to Output(Y)	t_{PLH}	$V_{CC}=3.3\pm 0.3\text{V}, C_L=15\text{pF}$		5.5	7.9	ns
	t_{PHL}			5.5	7.9	
	t_{PLH}	$V_{CC}=3.3\pm 0.3\text{V}, C_L=50\text{pF}$		8	11.4	
	t_{PHL}			8	11.4	
Propagation Delay from Input (A and B) to Output(Y)	t_{PLH}	$V_{CC}=5.0\pm 0.5\text{V}, C_L=15\text{pF}$		3.7	5.5	ns
	t_{PHL}			3.7	5.5	
	t_{PLH}	$V_{CC}=5.0\pm 0.5\text{V}, C_L=50\text{pF}$		5.2	7.5	
	t_{PHL}			5.2	7.5	

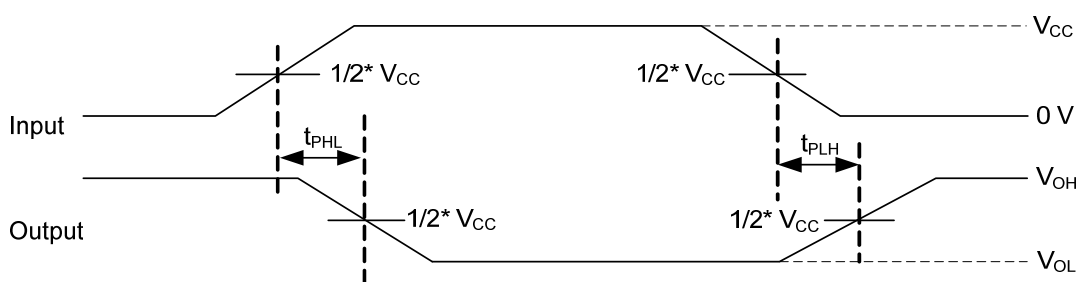
■ OPERATING CHARACTERISTICS ($V_{CC}=5\text{V}$; $T_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	No load, $f=1\text{MHz}$		9.5		pF

■ TEST CIRCUIT AND WAVEFORM



C_L includes probe and jig capacitance.



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