TS68C429A
CMOS ARINC 429 Multichannel Receiver/Transmitter (MRT)

Datasheet

Features

- **Eight Independent Receivers (Rx)**
- **Three Independent Transmitters (Tx)**
- **Full TS68K Family Microprocessor Interface Compatibility**
- **16-bit Data-bus**
- **ARINC 429 Interface: “1” and “0” Lines, RZ Code**
- **Support all ARINC 429 Data Rate Transfer and up to 2.5 Mbit/s**
- **Multi Label Capability**
- **Parity Control: Odd, Even, No Parity, Interrupt Capability**
- **Independent Programmable Frequency for Rx and Tx Channels**
- **Eight Messages FIFO per Tx Channel**
- **Independent Interrupt Request Line for Rx and Tx Functions**
- **Vectored Interrupts**
- **Daisy Chain Capability**
- **Direct Addressing of all Registers**
- **Test Modes Capability**
- **20 MHz Operating Frequency**
- **Self-test Capability for Receiver Label Memories and Transmit FiFO**
- **Low Power: 400 mW**

Description

The TS68C429A is an ARINC 429 controller. It is an enhanced version of the EF 4442 and it is designed to be connected to the new 16- or 32-bit microprocessors, especially these of the e2v TS68K family.

Screening

- **MIL-STD-883, Class B**
- **DESC Drawing 5962-955180**
- **e2v Standards**

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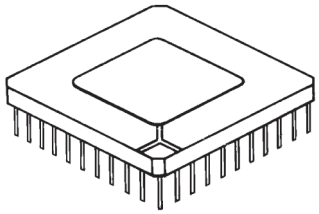
0848E–HIREL–02/08

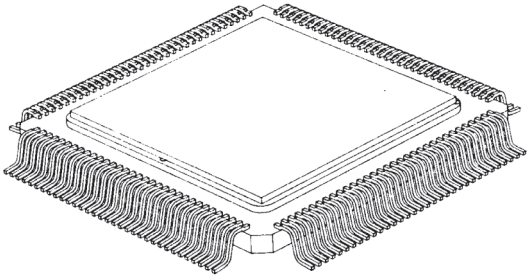
Application Note

- A detailed application note is available “AN 68C429A” on request.

R suffix
PGA 84
Ceramic Pin Grid Array



F suffix
CQFP 132
Ceramic Quad Flat Pack



1. Hardware Overview

The TS68C429A is a high performance ARINC 429 controller designed to interface primary to the e2v TS68K family microprocessor in a straight forward fashion (see “Application Notes” on page 35). It can be connected to any TS68K processor family with an asynchronous bus with some additional logic in some cases.

As shown in Figure 1-1 on page 3, the TS68C429A is divided into five main blocks, the microprocessor interface unit (MIU), the logical control unit (LCU), the interrupt control unit (ICU), the receiver channel unit (RCU) and the transmitter channel unit (TCU).

- The MIU handles the interface protocol of the host processor. Through this unit, the host sees the TS68C429A as a set of registers.
- The LCU controls the internal data flow and initializes the TS68C429A.
- The ICU manages one interrupt line for the RCU and one for the TCU. Each of these two parts has a daisy chain capability. All channels have a dedicated vectored interrupt answer. Receiver channels priority is programmable.
- The RCU is composed of 8 ARINC receiver channels made of:
  - a serial to parallel converter to translate the two serial signals (the “1” and “0” in RZ code) into two 16-bit words,
  - a memory to store the valid labels,
  - a control logic to check the validity of the received message,
  - a buffer to keep the last valid received message.
- The TCU is composed of three ARINC transmitter channels made of:
  - a parallel to serial converter to translate the messages into two serial signals (the “1” and “0” in RZ code),
  - a FIFO memory to store eight 32-bit ARINC messages,
  - a control logic to synchronize the message transmitter (parity, gap, speed, etc.).
- Test facility: Rx inputs can be internally connected to TX3 output.
- Self-test facility: The receiver control label matrix and transmitter FIFO can be tested. This self-test can be used to verify the integrity of the TS68C429A memories.

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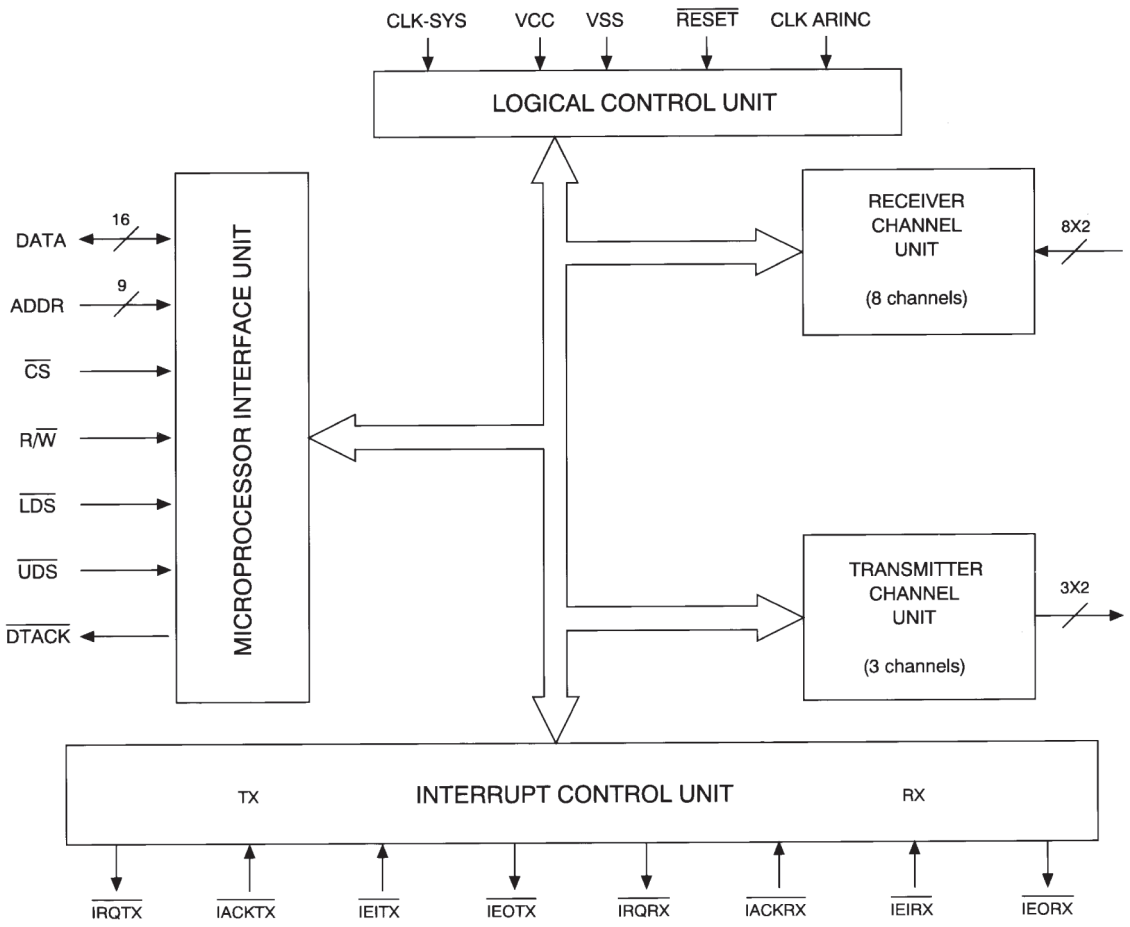
Figure 1-1. Simplified Block Diagram



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2. Package

See "Package Mechanical Data" on page 41 and "Terminal Connections" on page 42.

Table 2-1. Signal Description

Pin Name	Type	Function
A0-8	I	Address bus. The address bus is used to select one of the internal registers during a processor read or write cycle.
D0-15	I/O	This bi-directional bus is used to receive data from or transmit data to an internal register during a processor read or write cycle. During an interrupt acknowledge cycle, the vector number is given on the lower data bus (D0 - D7).
$\overline{CS}$	I	Chip select (active low). This input is used to select the chip for internal register access.
$\overline{LDS}$	I	Lower data strobe. This input (active low) validates lower data during R/$\overline{W}$ access (D0-D7).
$\overline{UDS}$	I	Upper data strobe. This input (active low) validates upper data during R/$\overline{W}$ access (D8-D15).
R/$\overline{W}$	I	Read/write. This input defines a data transfer as a read (high) or a write (low) cycle.
$\overline{DTACK}$	O	Data transfer acknowledge. If the bus cycle is a processor read, the chip asserts $\overline{DTACK}$ to indicate that the information on the data bus is valid. If the bus cycle is a processor write, $\overline{DTACK}$ acknowledges the acceptance of the data by the MRT. $\overline{DTACK}$ will be asserted during chip select access ($\overline{CS}$ asserted) or interrupt acknowledge cycle ($\overline{IACKTX}$ or $\overline{IACKRK}$ asserted).
$\overline{IRQTX}$	O	Interrupt transmit request. This open drain output signals to the processor that an interrupt is pending from the transmission part of the MRT. There are 6 causes that can generate an interrupt request (2 per channel: FIFO empty and end of transmission).
$\overline{IACKTX}$	I	Interrupt transmit acknowledge. If $\overline{IRQTX}$ is active, the MRT will begin an interrupt acknowledge cycle. The MRT will generate a vector number to the processor which is the highest priority channel requesting interrupt service.
$\overline{IEITX}$	I	Interrupt transmit enable in. This input, together with $\overline{IEOTX}$ signal, provides a daisy chained interrupt structure for a vectored scheme. $\overline{IEITX}$ (active low) indicates that no higher priority device is requesting interrupt service.
$\overline{IEOTX}$	O	Interrupt transmit enable out. This output, together with $\overline{IEITX}$ signal, provides a daisy chained interrupt structure for a vectored interrupt scheme. $\overline{IEOTX}$ (active low) indicates to lower priority devices that neither the TS68C429A nor any highest priority peripheral is requesting an interrupt.
$\overline{IRQRX}$	O	Interrupt transmit request. This open drain output signals to the processor that an interrupt is pending from the receiving part of the chip. There are 9 causes that can generate an interrupt request (1 per channel: valid message received, and 1 for bad parity on a received message).
$\overline{IACKRX}$	I	Interrupt receive acknowledge. Same function as $\overline{IACKTX}$ but for receiver part.
$\overline{IEIRX}$	I	Interrupt receive enable in. Same function as $\overline{IEITX}$ but for receiver part.
$\overline{IEORX}$	I	Interrupt receive enable out. Same function as $\overline{IEOTX}$ but for receiver part.
TX1H	O	Transmission "1" line of the channel 1.
TX1L	O	Transmission "0" line of the channel 1.
TX2H	O	Transmission "1" line of the channel 2.
TX2L	O	Transmission "0" line of the channel 2.
TX3H	O	Transmission "1" line of the channel 3.
TX3L	O	Transmission "0" line of the channel 3.
RX1H	I	Receiving "1" line of the channel 1.

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Table 2-1. Signal Description (Continued)

Pin Name	Type	Function
RX1L	I	Receiving “0” line of the channel 1.
RX2H	I	Receiving “1” line of the channel 2
RX2L	I	Receiving “0” line of the channel 2.
RX3H	I	Receiving “1” line of the channel 3.
RX3L	I	Receiving “0” line of the channel 3.
RX4H	I	Receiving “1” line of the channel 4.
RX4L	I	Receiving “0” line of the channel 4.
RX5H	I	Receiving “1” line of the channel 5.
RX5L	I	Receiving “0” line of the channel 5.
RX6H	I	Receiving “1” line of the channel 6.
RX6L	I	Receiving “0” line of the channel 6.
RX7H	I	Receiving “1” line of the channel 7.
RX7L	I	Receiving “0” line of the channel 7.
RX8H	I	Receiving “1” line of the channel 8.
RX8L	I	Receiving “0” line of the channel 8.
$\overline{\text{RESET}}$	I	This input (active low) will initialize the TS68C429A registers.
V_{CC}/GND	I	These inputs supply power to the chip. The V_{CC} is powered at +5 volts and GND is the ground connection.
CLK-SYS	I	The clock input is a single-phase signal used for internal timing of processor interface.
CLK-ARINC	I	This input provides the timing clock to synchronize received/transmitted messaged.

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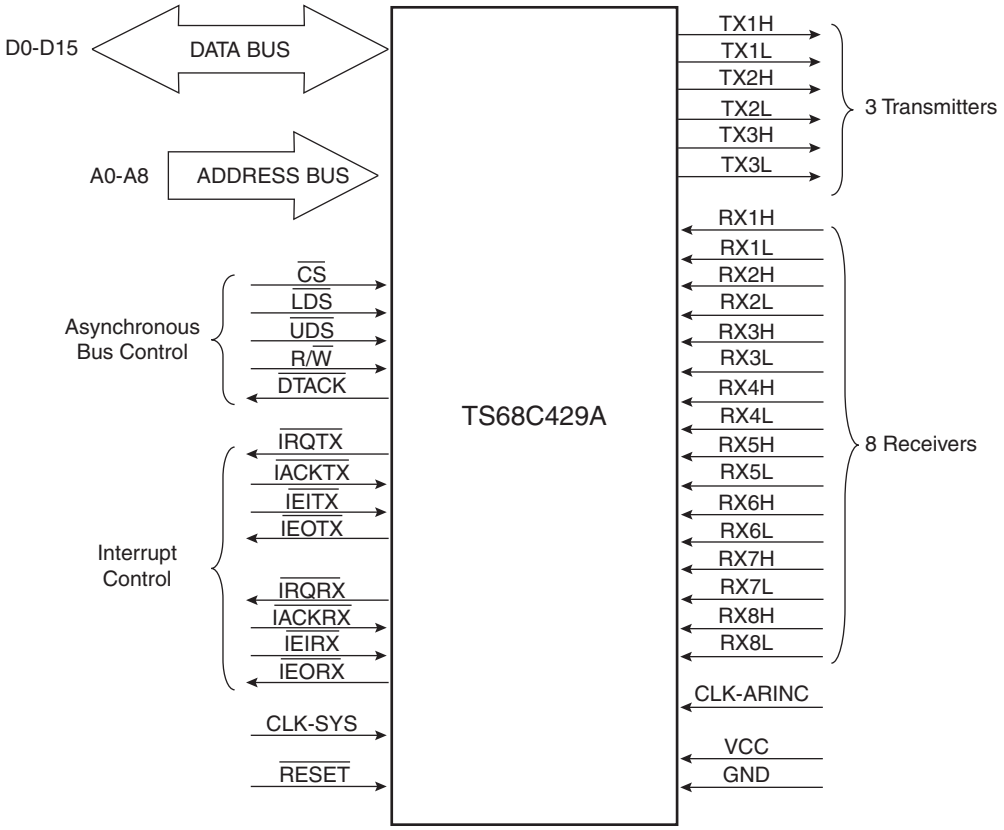
Figure 2-1 illustrates the functional signal groups.

Figure 2-1. Functional Signal Groups Diagram



3. Scope

This drawing describes the specified requirements for the ARINC multi channel receiver/transmitter, in compliance either with MIL-STD-863 class B or SMD drawing.

4. Applicable Documents

4.1 MIL-STD-883

1. MIL-STD-883: test methods and procedures for electronics
2. MIL-STD-38535: general specifications for microcircuits.
3. MIL-STD-1835 microcircuit case outlines.
4. DESC/SMD.

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5. Requirements

5.1 General

The microcircuits are in accordance with the applicable document and as specified herein.

5.2 Design and Construction

5.2.1 Terminal Connections

Depending on the package, the terminal connections is detailed in "Terminal Connections" on page 42.

5.2.2 Package

The circuits are packaged in a hermetically sealed ceramic package which is conform to case outlines of MIL-STD 1835 (when defined):

- PGA 84,
- CQFP 132.

The precise case outlines are described at the end of this specification ("Package Mechanical Data" on page 41) and into MIL-STD-1835.

5.2.3 Special Recommended Conditions for CMOS Devices

- CMOS Latch-up

The CMOS cell is basically composed of two complementary transistors (a P-channel and an N-channel), and, in the steady state, only one transistor is turned-on. The active P-channel transistor sources current when the output is a logic high and presents a high impedance when the output is a logic low. Thus the overall result is extremely low power consumption because there is no power loss through the active P-channel transistor. Also since only once transistor is determined by leakage currents.

Because the basic CMOS cell is composed of two complementary transistors, a parasitic semiconductor controlled rectifier (SCR) formed and may be triggered when an input exceeds the supply voltage. The SCR that is formed by this high input causes the device to become "latched" in a mode that may result in excessive current drain and eventual destruction of the device. Although the device is implemented with input protection diodes, care should be exercised to ensure that the maximum input voltages specification is not exceeded from voltage transients; others may require no additional circuitry.

- CMOS/TTL Levels

The TS68C429A doesn't satisfy totally the input/output drive requirements of TTL logic devices, see Table 7-1 on page 11.

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5.3 Electrical Characteristics

Table 5-1. Absolute Maximum Ratings

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{CC}	Supply Voltage		-0.3	+7.0	V
V_I	Input Voltage		-0.3	+7.0	V
P_{DMAX}	Max Power Dissipation			400	mW
T_{CASE}	Operating Temperature	M suffix	-55	+125	°C
		V suffix	-40	+85	°C
T_{STG}	Storage Temperature		-55	+150	°C
T_J	Junction Temperature			+160	°C
T_{LEADS}	Lead Temperature	Max 5 sec. soldering		+270	°C

Unless otherwise stated, all voltages are referenced to the reference terminal.

Table 5-2. Recommended Condition of Use

Symbol	Parameter	Test conditions	Min	Max	Units
V_{CC}	Supply Voltage		4.5	5.5	V
V_{IL}	Low Level Input Voltage		-0.5	0.8	V
V_{IH}	High Level Input Voltage		2.25	5.8	V
T_{CASE}	Operating Temperature	M suffix	-55	+125	°C
		V suffix	-40	+85	°C
C_L	Output Loading Capacitance			130	pF
$t_r(c)$	Clock Rise Time (See Figure 5-1 on page 9)			5	ns
$t_f(c)$	Clock Fall Time (See Figure 5-1 on page 9)			5	ns
f_c	Clock System Frequency (See Figure 5-1 on page 9)		0.5	20	MHz

This device contains protective circuitry against damage due to high static voltages or electrical fields: however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or VCC).

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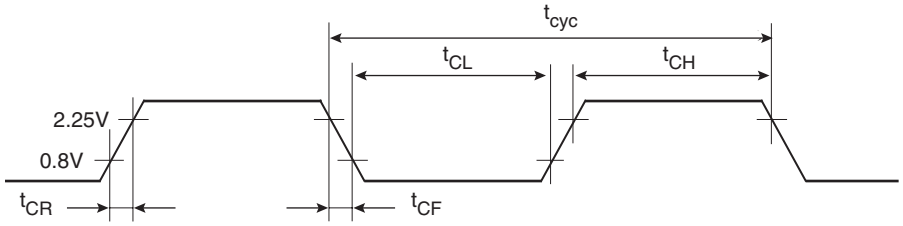
Figure 5-1. Clock Input Timing Diagram



Note: Timing measurements are referenced to and from a low of 0.8-volt and a high voltage of 2.25 volts, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8-volt and 2.25 volts.

Table 5-3. Thermal Characteristics

Package	Symbol	Parameter	Value	Unit
PGA 68	θ_{J-A}	Thermal Resistance Junction-to-ambient	28	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	2	°C/W
CQFP 132	θ_{J-A}	Thermal Resistance Junction-to-ambient	27	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	3	°C/W

5.3.1 Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts–Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins–User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K: (T_J + 273) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}).

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These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad (4)$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

5.4 Mechanical and Environment

The microcircuits shall meet all mechanical environmental requirements of either MIL-STD-883 for class B devices or DESC devices.

5.5 Marking

The document where are defined the marking are identified in the related reference documents. Each microcircuit are legibly and permanently marked with the following information as minimum:

- e2v logo
- Manufacturer's part number
- Class B identification
- Date-code of inspection lot
- ESD identifier if available
- Country of manufacturing

6. Quality Conformance Inspection

6.1 DESC/MIL-STD-883

Is in accordance with MIL-M-38510 and method 5005 of MIL-STD-883. Group A and B inspections are performed on each production lot. Group C and D inspections are performed on a periodic basis.

7. Electrical Characteristics

7.1 General Requirements

All static and dynamic electrical characteristics specified for inspection purposes and the relevant measurement conditions are given below:

- Table 7-1, Table 7-2: Static electrical characteristics for the electrical variants.
- Table 7-3, Table 7-4, Table 7-5: Dynamic electrical characteristics.

For static characteristics (Table 7-1, Table 7-2), test methods refer to IEC 748-2 method number, where existing.

For dynamic characteristics (Table 7-3, Table 7-4, Table 7-5), test methods refer to clause 5.5 of this specification.

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Table 7-1. DC Electrical Characteristics
With -55°C ≤ T_{CASE} ≤ +125°C or -40° ≤ T_{CASE} ≤ +85°C; V_{CC} = 5V ± 10%.

Symbol	Parameter		Min	Max	Unit
V_{IH}	Input High Voltage		2.25	V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		-0.5	0.8	V
V_{OH}	Output High Voltage (except $\overline{IRQRX}$, $\overline{IRQTX}$, $\overline{DTACK}$: open drain outputs)		2.7		V
V_{OL}	Output Low Voltage			0.5	V
I_{OH}	Output Source Current (except $\overline{IRQRX}$, $\overline{IRQTX}$, $\overline{DTACK}$: open drain outputs)	(V_{OUT} = 2.7V)		-8	mA
I_{OL}	Output Sink Current	(V_{OUT} = 0.5V)		8	mA
	DTACK Output Sink Current	(V_{OUT} = 0.5V)		6	mA
I_{LI}	Input Leakage Current	(V_{IN} = 0 to V_{CC})		±20	µA
IDD	Dynamic Current[1]	(T_{CASE} = T_{min} · V_{DD} = V_{max})		65	mA

Note: 1. IDD is measured with all I/O pins at 0V, all input pins at 0V except signals $\overline{CS}$, $\overline{IACKxx}$, $\overline{LDS}$, $\overline{UDS}$ at 5V and CLK-SYS and CLK-ARINC which run at t_{CYC} mini.

Table 7-2. Capacitance (T_A = 25°C)

Symbol	Parameter	Max	Unit
C_{IN}	Input Capacitance	10	pF
C_{OUT}	HI-Z Output Capacitance	20	pF

7.2 Clock Timing

Table 7-3. Clock System (CLK SYS)

Symbol	Parameter	Min	Max	Unit
t_{CYC} S	Clock Period	50	2000	ns
t_{CLS}, t_{CHS}	Clock Pulse Width	20		ns
t_{CRS}, t_{CFS}	Rise and Fall Times		5	ns

Table 7-4. Clock ARINC (CLK ARINC)

Symbol	Parameter	Min	Max	Unit
t_{CYC} A	Cycle Time[1]	200	8000	ns
t_{CLA}, t_{CHA}	Clock Pulse Width	240		ns
t_{CRA}, t_{CFA}	Rise and Fall Times		5	ns

Note: 1. t_{CYC} A ≥ 4 x t_{CYC} S.

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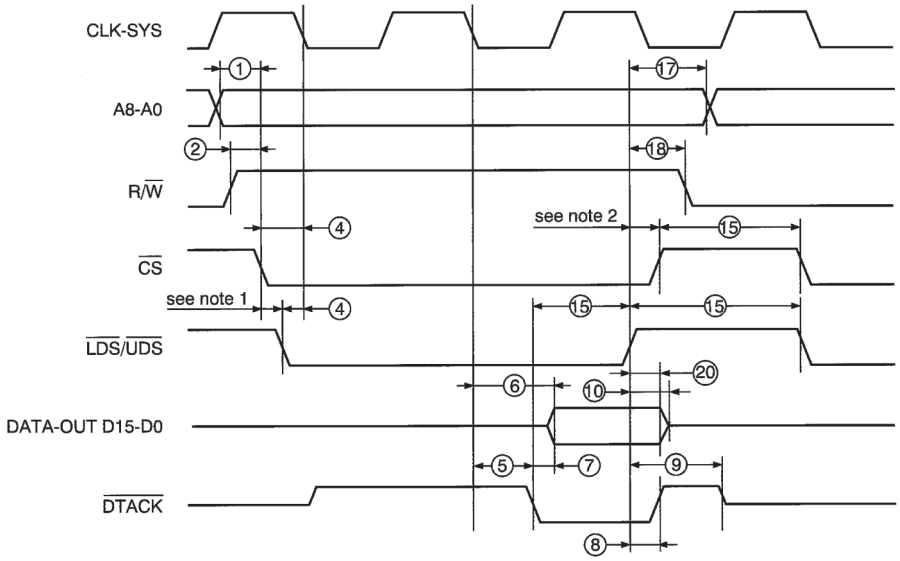
7.3 AC Electrical Characteristics

With V_{CC} = 5 V_{DC} ± 10% V_{SS} = 0 V_{DC}.

$\overline{IEIxx}$, $\overline{IEOxx}$, $\overline{IACKxx}$, must be understood as generic signals (xx = RX and TX).

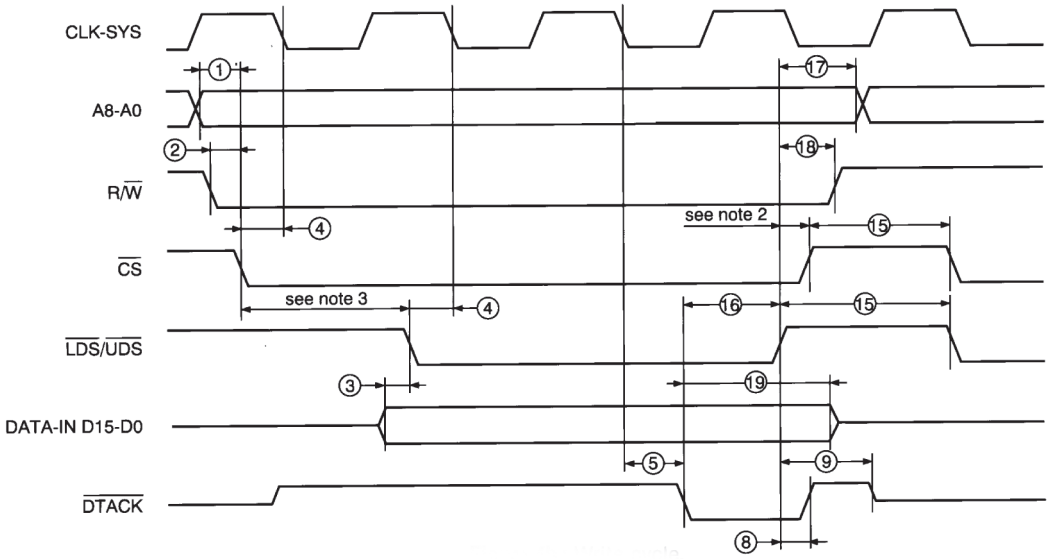
Figure 7-1. Read Cycle



Notes: 1. $\overline{LDS}$/$\overline{UDS}$ can be asserted on the next or previous CLK-SYS period after $\overline{CS}$ goes low but (4) must be met for the next period.

2. The cycle ends when the first of $\overline{CS}$, $\overline{LDS}$/$\overline{UDS}$ goes high.

Figure 7-2. Write Cycle



Note: 1. $\overline{LDS}$/$\overline{UDS}$ can be asserted on the same or previous CLK-SYS period as $\overline{CS}$ but (3) and (4) must be met.

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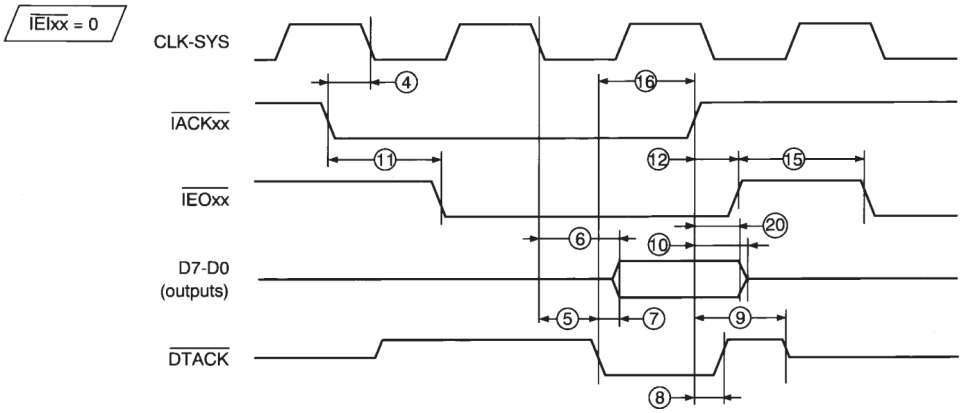
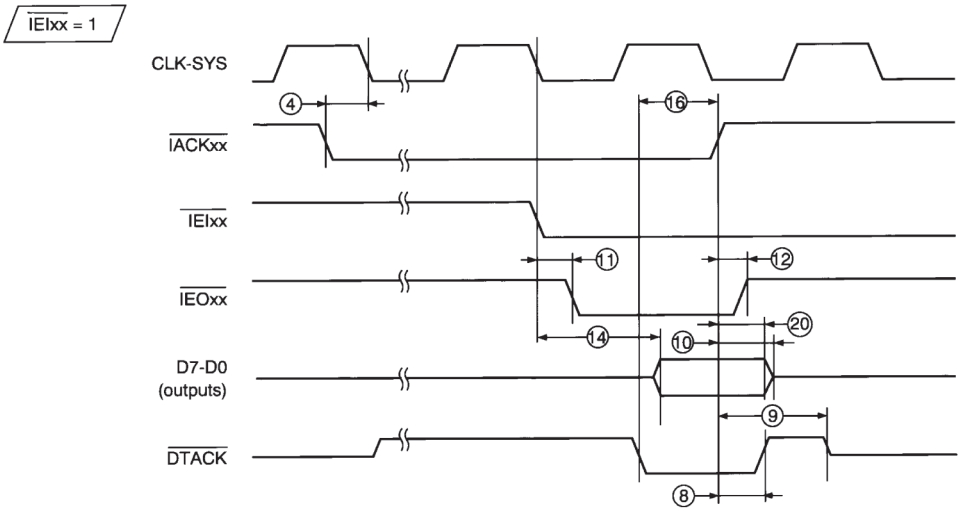
Figure 7-3. Interrupt Cycle (IEIxx = 0)



Notes: 1. If $\overline{UDS}$ = 1, D15-D8 stay hi-z else D15-D8 drive the bus with a stable unknown value.

2. If $\overline{IEOxx}$ goes low, neither vector nor $\overline{DTACK}$ are generated, else $\overline{IEOxx}$ stays inactive and a vector is generated (D7-D0 and $\overline{DTACK}$).

Figure 7-4. Interrupt Cycle (IEIxx = 1)



Notes: 1. If $\overline{UDS}$ = 1, D15-D8 stay hi-z else D15-D8 drive the bus with a stable unknown value.

2. If $\overline{IEOxx}$ goes low, neither vector nor $\overline{DTACK}$ are generated, else $\overline{IEOxx}$ stays inactive and a vector is generated (D7-D0 and $\overline{DTACK}$).

Table 7-5. Timing Characteristic

Number	Symbol	Parameter	Min	Max	T/G[1]	Unit
1	t_{AVCSL}	Address valid to $\overline{CS}$ low	0	-	T	ns
2	t_{RWVCSL}	R/W valid to $\overline{CS}$ low	0	-	T	ns
3	t_{DIVDSL}	Data in valid to $\overline{LDS}$/$\overline{UDS}$ low	0	-	T	ns
4	t_{SVCL}	CS, $\overline{LDS}$/$\overline{UDS}$, $\overline{IACKxx}$ valid to CLK-SYS low	5	-	T	ns

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Table 7-5. Timing Characteristic (Continued)

Number	Symbol	Parameter	Min	Max	T/G[1]	Unit
5	t_{CLDKL}	CLK-SYS low to $\overline{DTACK}$ low	-	45	T	ns
6	t_{CLDOV}	CLK-SYS low to data out valid	-	50	T	ns
7	t_{DKLDOV}	$\overline{DTACK}$ low to data out valid	-	10	G	ns
8	t_{SHDKH}	$\overline{CS}$ or $\overline{LDS}$/$\overline{UDS}$ or $\overline{IACKxx}$ high to $\overline{DTACK}$ high	-	35	G	ns
9	t_{SHDXZ}	$\overline{CS}$ or $\overline{LDS}$/$\overline{UDS}$ or $\overline{IACKxx}$ high to $\overline{DTACK}$ hi-z	-	50	G	ns
10	t_{SHDOZ}	$\overline{CS}$ or $\overline{LDS}$/$\overline{UDS}$ or $\overline{IACKxx}$ high to data out hi-z	-	25	G	ns
11	t_{ILIOL}	$\overline{IEIxx}$ or $\overline{IACKxx}$ low to $\overline{IEOxx}$ low	-	35	T	ns
12	t_{IKHIOH}	$\overline{IACKxx}$ high to IEOxx high	-	40	T	ns
13	t_{IILDKL}	$\overline{IEIxx}$ low to $\overline{DTACK}$ low	-	40	T	ns
14	t_{IILDOV}	$\overline{IEIxx}$ low to data out valid	-	45	T	ns
15	t_{SH}	$\overline{CS}$, $\overline{IACKxx}$, $\overline{LDS}$/$\overline{UDS}$ inactive time	15	-	T	ns
16	t_{DKLSH}	$\overline{DTACK}$ low to $\overline{CS}$ or $\overline{LDS}$/$\overline{UDS}$ or $\overline{IACKxx}$ high	0	-	G	ns
17	t_{SHAH}	$\overline{CS}$ or $\overline{LDS}$/$\overline{UDS}$ high to address hold time	0	-	G	ns
18	t_{SHRWI}	$\overline{CS}$ or $\overline{LDS}$/$\overline{UDS}$ high to R/$\overline{W}$ invalid	0	-	G	ns
19	t_{DKLDIH}	$\overline{DTACK}$ low to data in hold time	0	-	G	ns
20	t_{SHDOH}	$\overline{CS}$ or $\overline{LDS}$/$\overline{UDS}$ or $\overline{IACKxx}$ high data out hold time	0	-	G	ns

Note: 1. T/G = Tested/Guaranteed.

8. Functional Description

8.1 Receiver Channel Unit (RCU)

8.1.1 Overview

The RCU is composed of 8 ARINC receiver channels and has per channel:

- a serial to parallel converter to translate the two serial signals in two 16-bit words.
- a memory to store the authorized labels,
- a control logic to check the validity of the received message.
- a buffer to keep the last valid received message.

8.1.2 Inputs

Each receiver channel has two input lines, receiving line high (RxiH) and receiving line low (RXiL) which are not directly compatible with the bipolar modulated ARINC line. This ARINC three-level state signals (“HIGH”, “NULL”, “LOW”) should be demultiplexed to generate the two RZ lines according to Figure 8-1.

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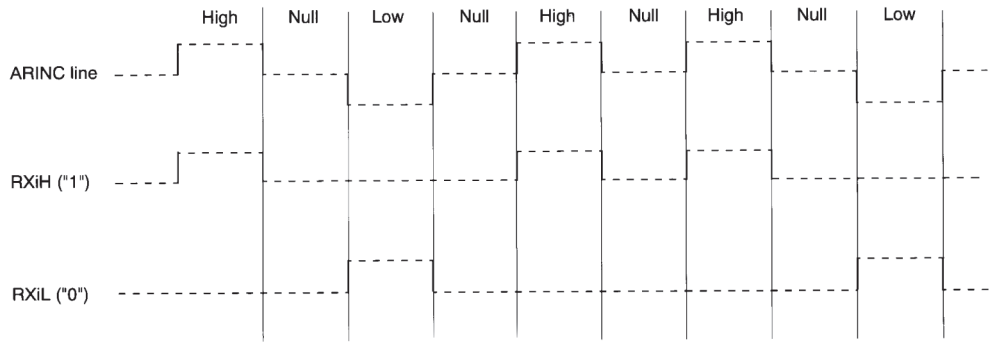
Figure 8-1.



8.1.3 Description

Each channel has a test mode in which the input signals (RXiH, RXiL), are internally connected to the third Transmit Channel Lines. This selection is done by programming the Test bit in the receiver control register (see "Register Description" on page 17) except this difference, the TS68C429A behaves exactly the same manner in the two modes. The receiver channel block diagram is given in Figure 8-2.

ARINC signals being asynchronous, the RCU first rebuilds the received clock in order to transfer the data within the shift-register and when the Gap-controller has detected the end of the message, tests the message validity according to the criteria listed hereafter.

To detect the end of the message, the Gap-Controller waits for a Gap after the last received bit. To do so, at each CLK ARINC cycle, a counter is incremented and compared to the content of the Gap-Register which has the user programmed value. If both values are equal, the counter is stopped and an internal end of message signal is generated. This counter is reseted on the falling edge of the rebuilt clock. Figure 8-2 shows the gap detection principle.

When the end of message is detected, the TS68C429A verifies the following points:

- the number of received bits must be 32,
- if requested the message parity (see "Register Description" on page 17) is compared to the parity bit of the message,
- the message label must be equal to one of the label stored in the Label Control Matrix,
- the Buffer is empty (that is: the last message has been read). The corresponding bit in the Status-register (see logical interface unit), has been cleared,
- when all four conditions are met, the message is transferred from the Shift-register to the Buffer and the corresponding bit is set in the Status-register. If the interrupt mode is enabled (see "General Circuit Control" on page 24) the IRQRX line is activated.

If not, reception of a new message is enabled, see Note.

If only the message parity is incorrect, an interrupt can be generated (see "Register Description" on page 17).

The Buffer is seen as two 16-bit word registers, the Most Significant Word of the message (MSW) is contained in the lower address, the Less Significant Word of the message (LSW) is contained in the upper address. The MSW should be read first because reading the LSW will release the buffer and allow transfer of a new message from the Shift-register.

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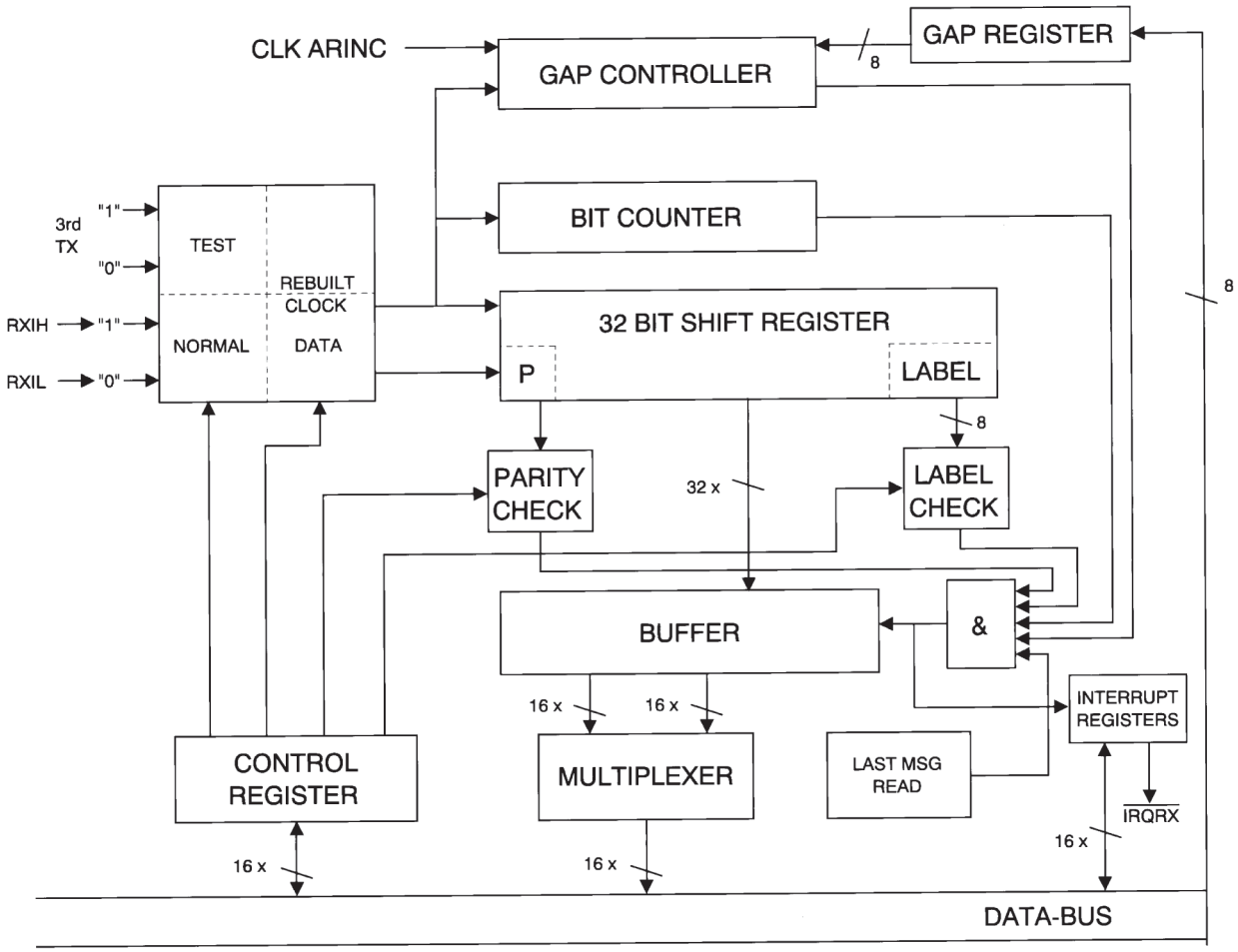
Figure 8-2. Receiver Channel Block Diagram



Note: A valid message is stored in the Shift-Reg. until a new message arrives and so may be transferred to the message buffer as soon as the buffer is “freed”.

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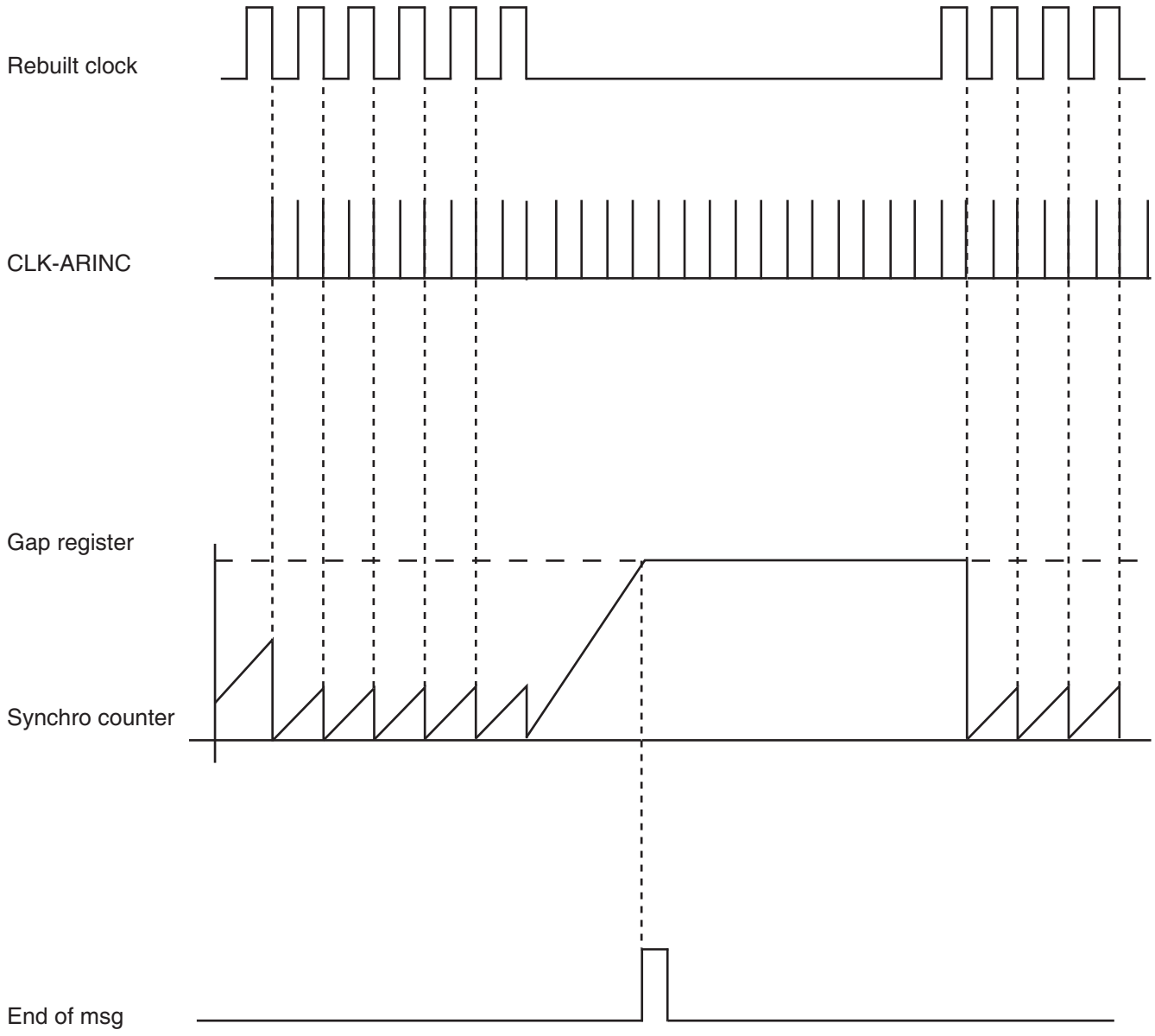
Figure 8-3.



8.1.4 Register Description

Four registers are associated to each receiver channel. These four registers are:

a) receiver control

b) gap register

c) message buffer

d) label control matrix

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- **Register Control Register**

This read/write register controls the function of the related receiver channel:

The lowest value will give the highest priority. If two channels have the same priority, one of them will never be able to send its interrupt vector to the microprocessor. Each channel must have a unique channel priority order.

Figure 8-4.

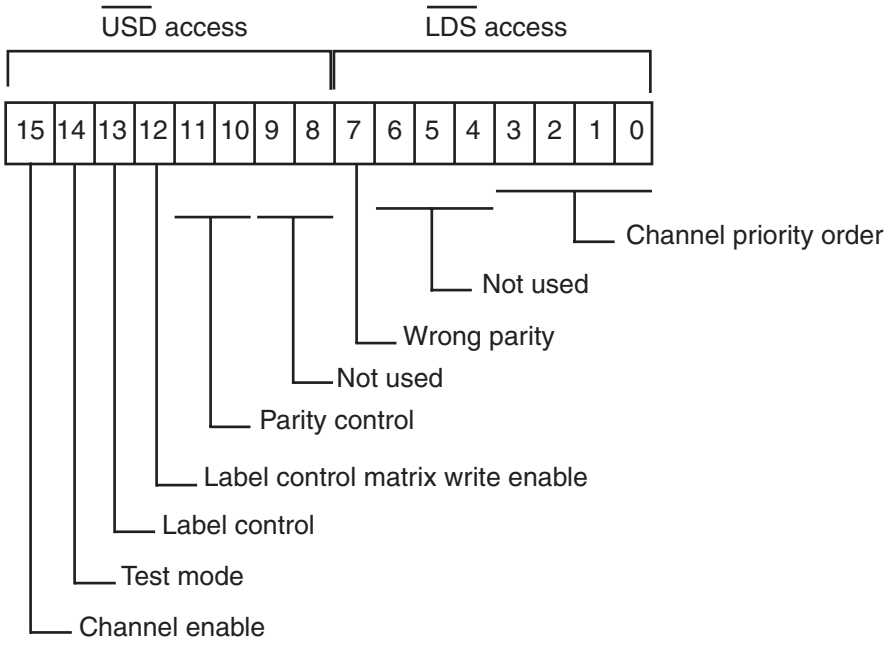

Table 8-1. Register Control Register Description

Bit	Function	Comments
Bit 15	Channel enable	0: channel is out of service 1: channel is in service
Bit 14	Test mode	0: external ARINC lines as input (normal operation) 1: third transmitter lines as input (test mode)
Bit 13	Label control	0: no control, all the labels are accepted 1: automatic check of the label according to the label control matrix
Bit 12	LCMWE label control matrix write enable	0: receiving mode (write to the matrix are disabled) 1: programmation mode for labels control matrix
Bit 11	Parity control	0: even parity check 1: odd parity check
Bit 10	Parity control	0: parity check is disable 1: parity check is enable
Bit 9	Not used	
Bit 8	Not used	

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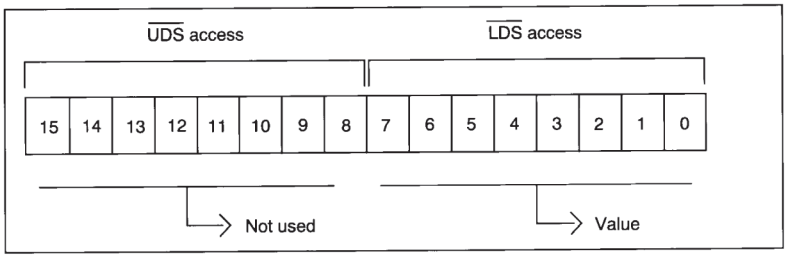
Table 8-1. Register Control Register Description (Continued)

Bit	Function	Comments
Bit 7	Wrong parity: this feature is enabled only if the self-test register bit 0 is set 1	0: received message parity is correct if read, reset wrong parity flag if written. 1: an incorrect received message parity has been detected (the corresponding message is lost) (set by hardware).
Bit 6	Not used	
Bit 5	Not used	
Bit 4	Not used	
Bit 0 to 3	Channel priority: order	The lowest value will give the highest priority. Each channel must have a unique channel priority order. If several messages are pending, the interrupt vector will account for highest priority channel.

- **Gap Register (Figure 8-5)**

The gap register is accessible for writing operations only. It contains the value on which the gap counter will be stopped and will generate the end of the message signal (see "Inputs" on page 14). The value is interpreted as a multiple of the CLK ARINC period.

Figure 8-5. Gap Register Description



The value of the gap register must be chosen so as to generate the end of the message before the minimal gap as defined in the ARINC-429 norm.

- **Message Buffer**

The Buffer is made of two 16-bit registers, the Most Significant Word of the message (MSW) is contained in the lower address register, the Least Significant Word of the message (LSW) is contained in the upper address register. For correct behavior, the MSW must be read before the LSW. They are accessible in read mode only and 16-bit access is mandatory.

- **Label Control Matrix**

The label control matrix is a 256 x 1 bit memory. There is one memory per channel.

The address is driven by the incoming label, the output data is used to validate this incoming message label (see Figure 8-6). To program this matrix, the LCMWE (label control matrix write enable) bit of the receiver-control-register should be set to "1" to allow the access. At this time, the address is driven by the external address bus and the data are written from the data bus D7 to D0 (one per channel according to Figure 8-7). Any write to a matrix on which the LCMWE is not set will not have any effect. The label control matrix can be written or read in byte and word mode. In word mode, the state of D15-D8 is unknown. After complete programming of the matrix, the LCMWE bit should be reset to "0" to allow normal receiving mode. A "1" in the memory means that this label is allowed and a "0" means that this label must be ignored.

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Figure 8-6. Label Control Matrix

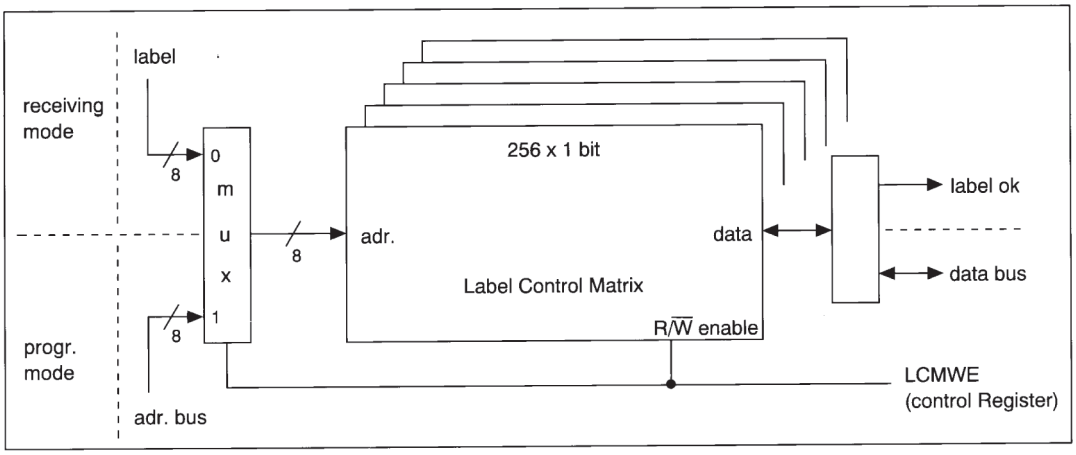
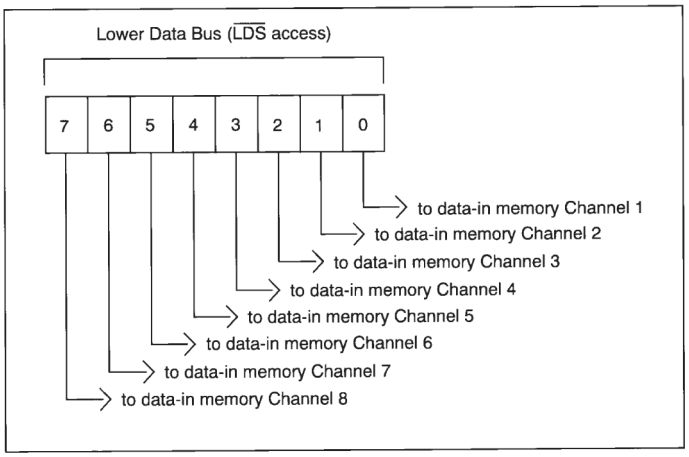


Figure 8-7.



9. Transmitter Channel Unit (TCU)

9.1 Overview

The TCU is composed of three ARINC transmit channels and has per channel:

- a parallel to serial converter to translate the messages into two serial signals,
- a FIFO memory to store eight 32-bit ARINC messages,
- a control logic to synchronize the message transmitter (parity, gap, speed...).

9.2 Outputs

Each transmitter channel has two output lines, Transmit line High (TXiH) and Transmit line Low (TXiL) which are not directly compatible with the bipolar modulated ARINC line. These RZ format lines should be translated by an outside device into ARINC three-level state signal according to Figure 9-1 on page 21.

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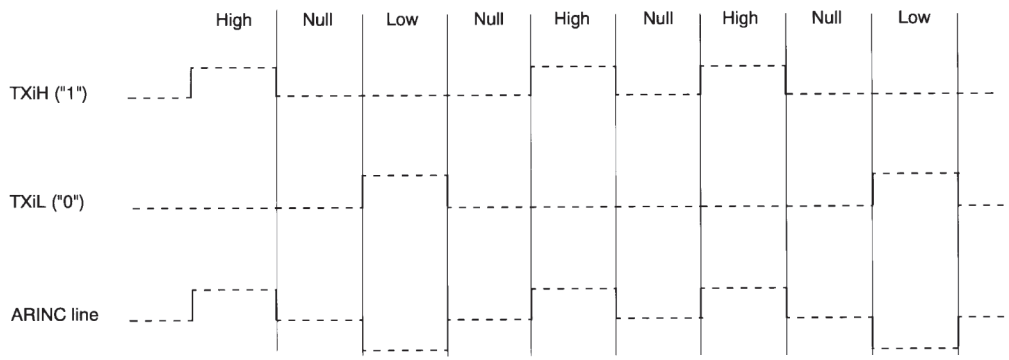
Figure 9-1. Transmitter Channel Unit Outputs



9.2.1 Description

The block diagram of a transmit channel is given is given in Figure 9-2. Only the third channel can be switched to internal lines for test mode, otherwise the channels are identical. The selection of this test mode is done by programming the test bit in the transmitter-control-register (see "Register Description" on page 17). In this test mode the lines TX3H and TX3L are not driven, they are both kept at "0".

The transmit frequency is generated by dividing the ARINC clock signal (CLK ARINC) by the value contained in the frequency register. This divided clock synchronizes the shift register which sends the 32-bit word on the lines TXiH and TXiL.

The parity is computed and if requested (see "Register Description" on page 17) the parity bit (32nd bit of the message) is modified to have an odd number of "1" in the 32-bit message for odd parity or an even number of "1" in the 32-bit message for even parity.

A gap control block generates a gap between the sent messages. The value of this gap is defined by the 5 bits "transmission gap" of the transmitter-control-register, it is given in number of ARINC bit (see "Register Description" on page 17).

A FIFO control block manages the messages to be sent. Up to 8 messages can be written into the FIFO. The FIFO is seen as a two 16-bit memory words, the Most Significant Word of the message (MSW) is written in the lower address, the Least Significant Word of the message (LSW) is written in the upper address. The MSW should be written first. The access to the FIFO is 16 bits mandatory. The number of messages within the FIFO is indicated by a counter that can be read through the transmitter-control-register. This counter is incremented when the LSW is written and decremented when the message is transferred to the shift-register. The "Reset FIFO" bit is used to cancel messages within the FIFO. If a transmission is on going, the entire message will be sent. The "reset FIFO" bit remains active until written at 1 by the microprocessor. When the transmitter is disable during a transmission, the out going message is lost.

When the FIFO is empty, a bit is set in the status-register (see "General Circuit Control" on page 24). If the interrupt mode is enabled (see "General Circuit Control" on page 24) the $\overline{\text{IRQTX}}$ line is activated.

When the transmitter FIFO is empty and when no transmission is on going, the first write access to the FIFO has to be preceded by the following sequence: disable and enable transmission (see Figure 10-9: First FIFO access).

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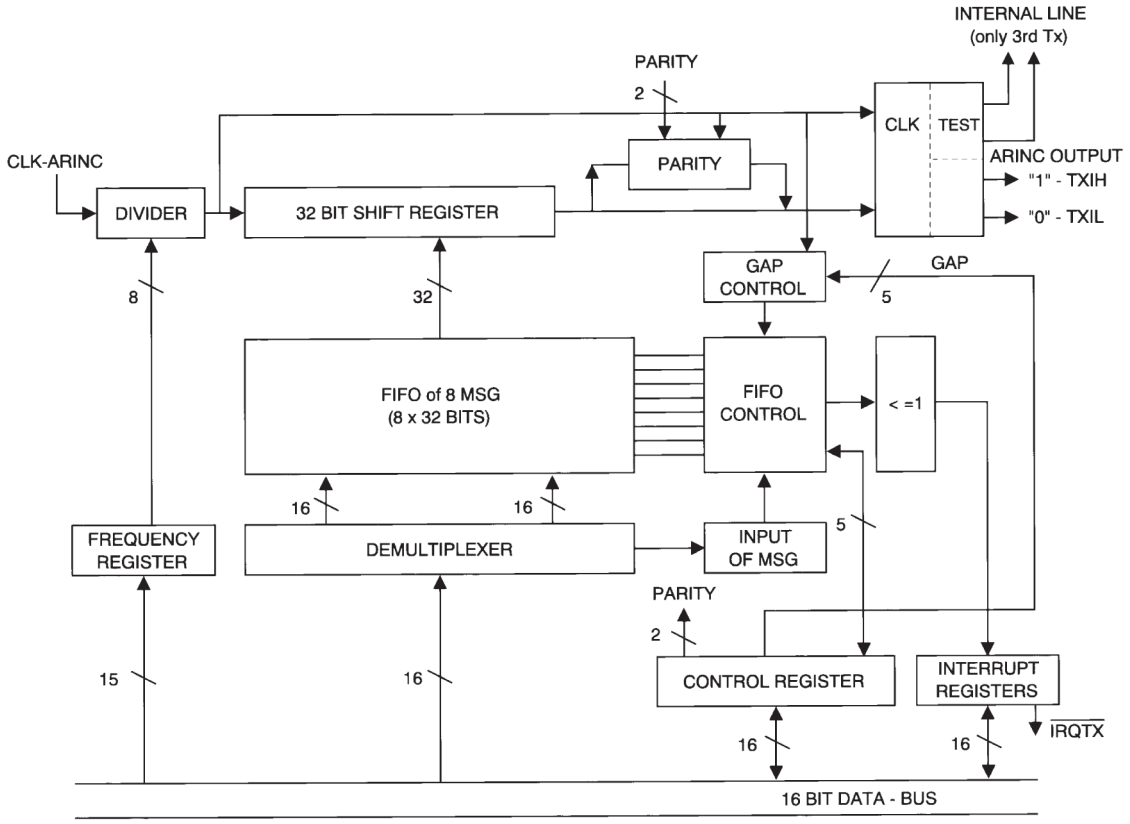
Figure 9-2. Transmitter Channel Block Diagram



9.2.2 Register Description

Three registers are associated to each transmitter channel:

- the frequency register,
- the transmitter control register,
- the FIFO.

- **The Frequency Register**

The frequency register is only accessible for writing operations by the user and contains the frequency divider.

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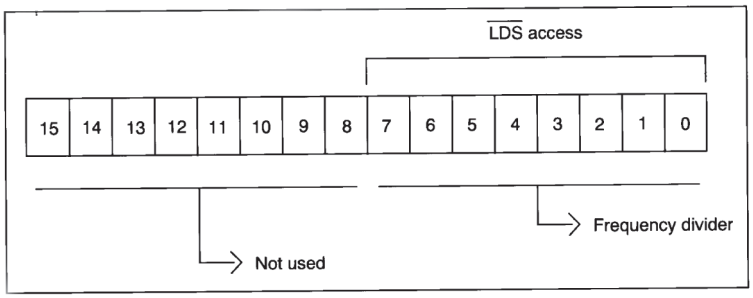
Figure 9-3. Frequency Register



The transmission frequency can be computed by dividing the CLK ARINC frequency by the frequency register value.

The frequency register must be loaded with a value greater or equal to 2.

- **The Transmitter Control Register**

The transmitter control register is accessible for reading and writing operations.

Figure 9-4. Transmitter Control Register

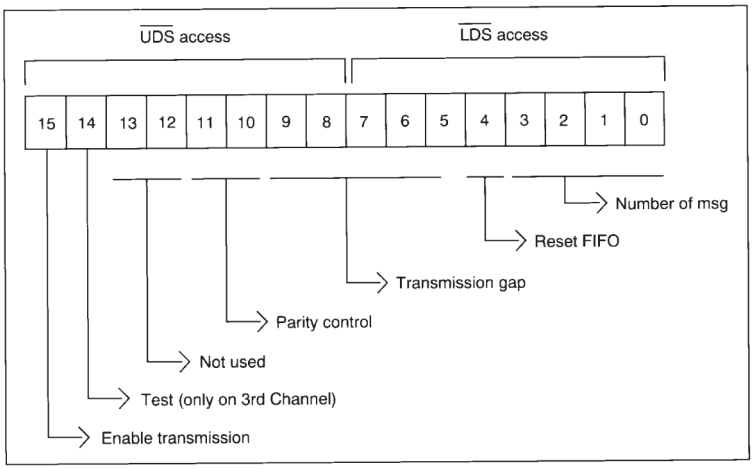


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Table 9-1. Transmission Control Register Description

Bit	Function	Comments
Bit 15	Enable transmission	- 0: channel out of service (stops on going transmission) - 1: channel in service - 1 to 0: transition is not allowed at the same time as an 1 to 0 transition of the bit 4 - when the transmitter FIFO is empty and when no transmission is on going, the first write access to the FIFO has to be preceded by the following sequence: reset to 0 and then set to 1
Bit 14	Test (only 3rd channel)	0: normal operating 1: test, output are only driven on internal lines for input testing
Bit 13 to 12	Not used	
Bus 11	Parity control	0: even parity calculation 1: odd parity calculation
Bit 10	Parity control	0: parity disable, Bit 32 of the message stays unchanged 1: parity enable. Bit 32 of the message will be forced by parity control
Bit 9 to 5	Transmission gap	“transmission gap” which is the delay between two 32-bit ARINC messages (in ARINC bit)
Bit 4	Reset FIFO	- write a 0 in this bit reset the FIFO counter - this bit must be set to 1 before any write in the transmit buffer. - 1 to 0: transition is not allowed at the same time as an 1 to 0 transition of the bit 15
Bit 3 to 0	Number of msg	these four bits indicate the available space within the FIFO

- **FIFO**

The FIFO is seen as two 16-bit words. The Most Significant Word (MSW) must be written first. The Least Significant Word (LSW) write increments the FIFO counter.

Before any write, the user should verify that the FIFO is not full. If the FIFO is full, any write to the FIFO will be lost.

9.3 General Circuit Control

9.3.1 Logical Control Unit (LCU)

The LCU mainly distributes the clocks and reset within the MRT. The reset signal, active low is an asynchronous signal. When it occurs, all registers are reset to zero except the Label-Control-Matrix which is not initialized and the Status-Register which is set to FC00 (hex). Reset duration must be greater than 4 clk-cyc periods.

The LCU contains the Status-register. This read/write register indicates the state of the internal operations. It is also the image of the pending interrupts if they are not masked. Clearing a bit “RX-Channel-i” will cancel the received message and release the Message-buffer for reception of a new message. The “End of TX on channel-i” Is set only when the involved channel FIFO is empty. The format of the Status-Register is given below.

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Figure 9-5. Status Register

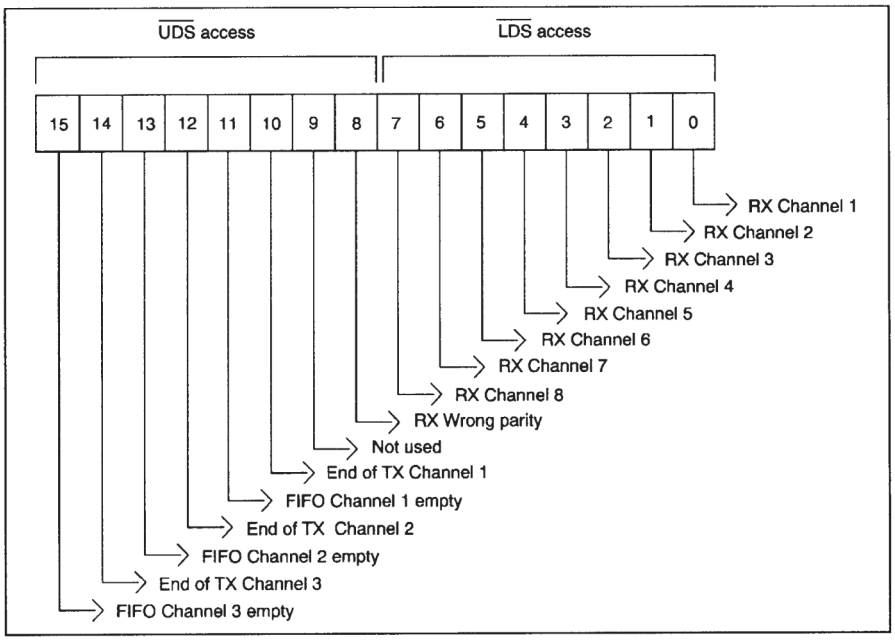

Table 9-2. Description of LCU Status Register

Bit	Function	Comments
Bit 15, 13, 11	FIFO channel 3, 2, 1 empty	0: FIFO not empty 1: FIFO empty
Bit 14, 12, 10	End of transmission on channel 3, 2, 1	0: Transmission occurs 1: No transmission actually
Bit 8	RX wrong parity. This feature is available only if self-test register bit 0 is set to 1. This bit must be reset to 0 by user when needed.	0: No wrong parity received 1: At least one receiver has received a message with wrong parity (set by hardware).
Bit 7, 6, 5, 4, 3, 2, 1, 0	Receiving channel 8, 7, 6, 5, 4, 3, 2, 1	0: Waiting for message 1: Received correct message

9.3.2 Microprocessor Interface Unit (MIU)

This interface which is directly compatible with the e2v TS68K family is based on an asynchronous data transfer.

The data exchange is mandatory on 16 bits for access to the FIFO messages (transmitter) and to the message buffer (receiver). For other access it can be on byte on D0-D7 with LDS assertion or an D8-D15 with UDS assertion.

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Figure 9-6 and Figure 9-7 on page 27 show the read and write flow chart.

Figure 9-6. Read Cycle Flow Chart

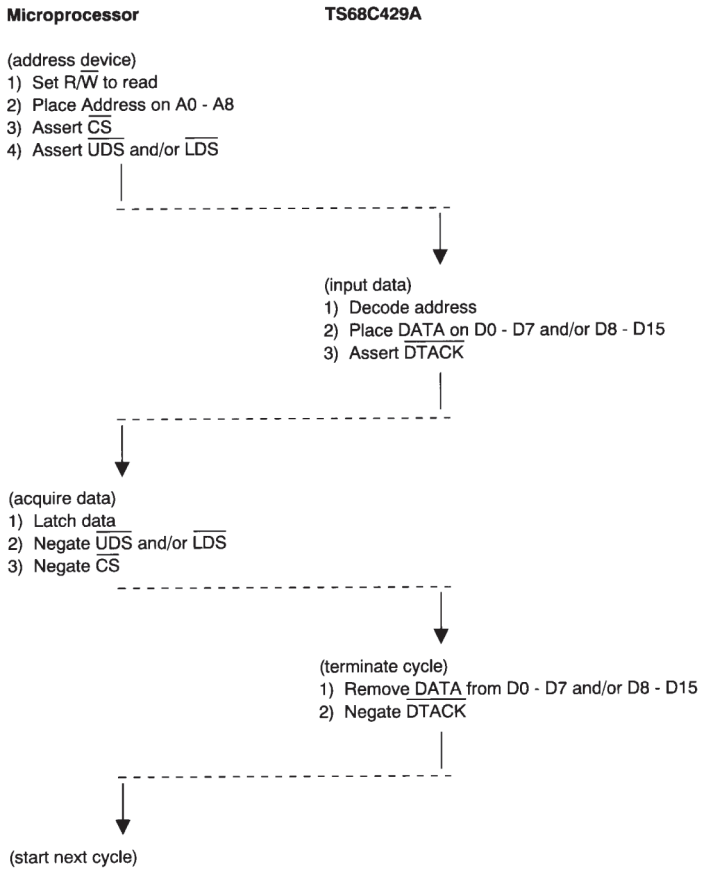
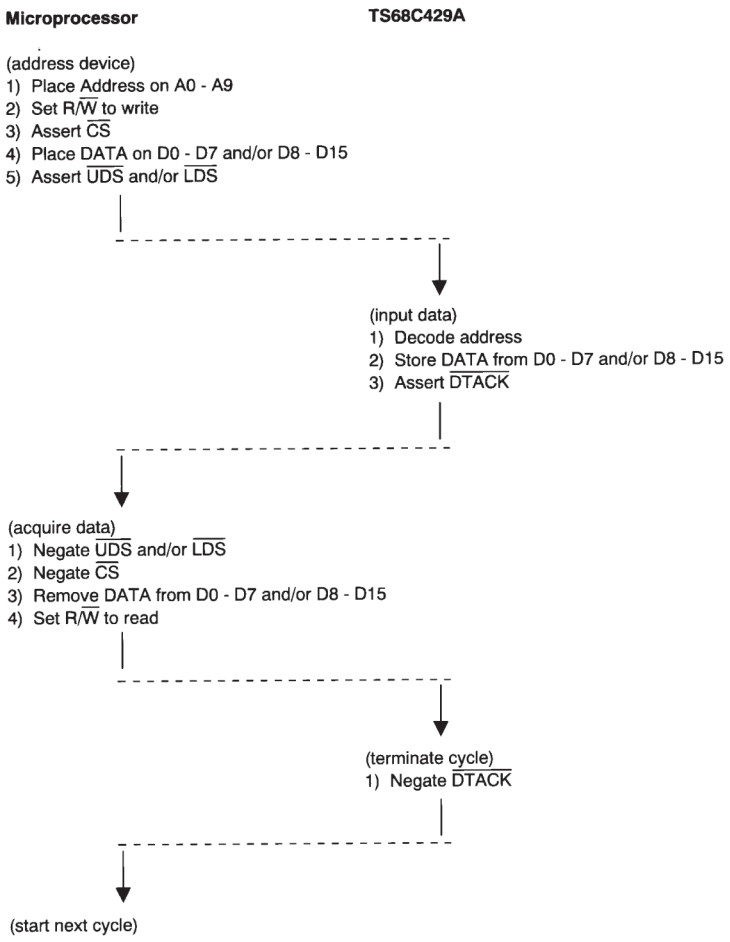


Figure 9-7. Write Cycle Flow Chart



9.3.3 Interrupt Control Unit (ICU)

- **Daisy Chain**

The ICU is composed of 2 interrupt blocks with a daisy chain capability (transmitter and receiver blocks). The daisy chain allows more than one circuit to be connected on the same interrupt line. Figure 9-8 shows the use of a daisy chain. IRQxx, IACKxx, IEIxx, IEOxx must be understood as generic signals. They are IRQTX, IACKTX, IEITX, IEOTX for the transmitter block and IRQRX, IACKRX, IEIRX, IEORX for the receiver block.

If IEIxx = 0, no higher device have an interrupt pending on the same line so the interrupt is requested and the IEOxx is forced high to disable lowest devices to generate interrupt. If IEIxx = 1, it waits for the condition IEIxx = 0. When IEIxx is tied high, IEOxx is forced high.

The daisy chains can be used to program a priority between receivers and transmitters interrupts when only one interrupt level is needed. An example is given in “Microprocessor Interface” on page 35.

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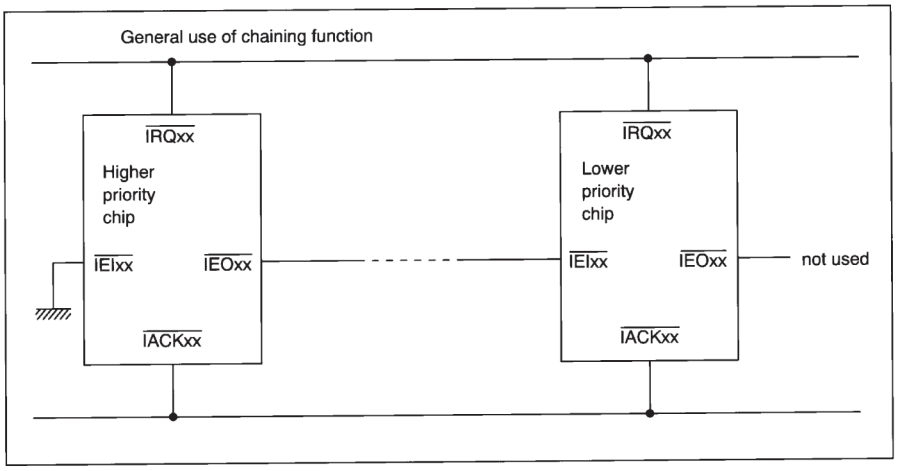
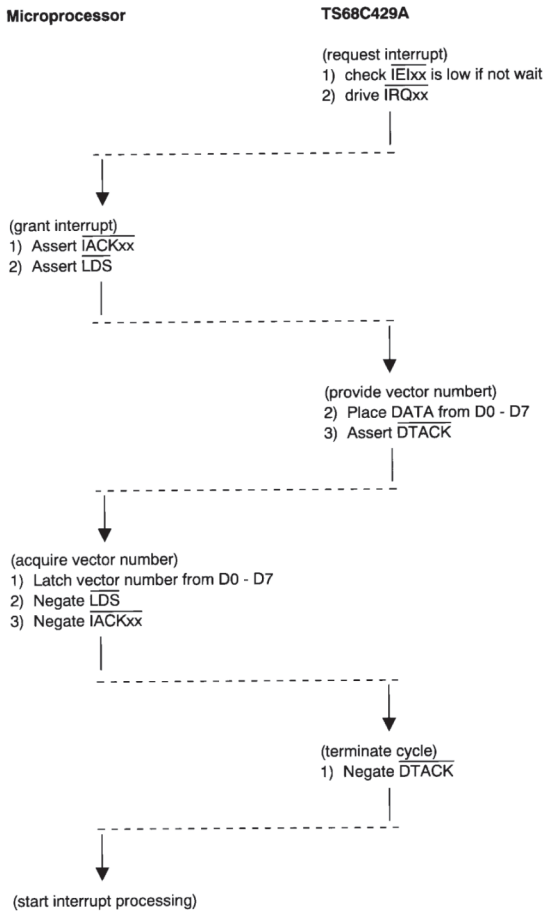
Figure 9-8. Interrupt Control Unit Daisy Chain Use



- **Vectored Interrupt**

They are 15 possibilities to generate an interrupt and two lines to handle them. To be more efficient, a unique vector number for each cause is given to the microprocessor as an answer to an IRQ. Figure 9-9 shows the interrupt acknowledge sequence flow chart.

Figure 9-9. Interrupt Acknowledge Sequence Flow Chart



- **Register Description**

Any internal status change that induces a bit to be set in the status-register will generate an interrupt if this cause is enabled by the Mask-register and if no highest priority cause is already activated or pending.

For the receiver blocks, the priority is programmable (see interrupt vector number description). For the transmitter block, the End-of-transmission has higher priority than FIFO-empty and channel 1 has higher priority than channel 2 that has higher priority than channel 3.

The RX wrong parity bit can be set only if self-test register bit 0 is set to 1.

The user has to check which receiver has it receiver control register bit 7 set to 1.

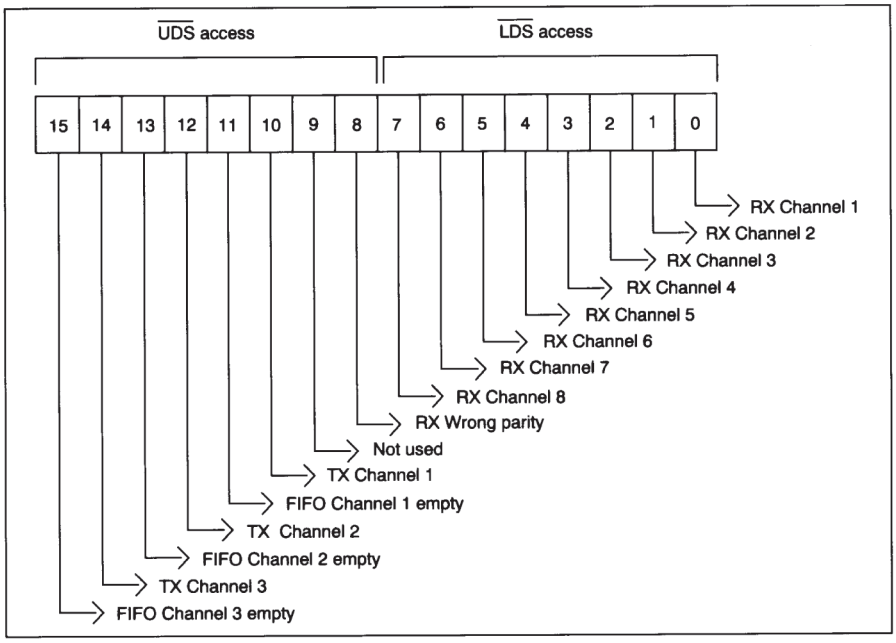
At the end of the interrupt procedure, the user must reset RX wrong parity bit to 0.

RX wrong parity is the highest interrupt priority source for the receiver part of the MRT.

- **The Mask Register**

The mask register is accessible for reading and writing operations. The mask register is used to disable interrupt source. The bit order is the same as in the status register. A “0” indicates that this source is disable, a “1” enables an interrupt for this source.

Figure 9-10. Mask Register



- **The Base Register**

The base register is only accessible for writing operations by the user. The base register must be programmed at the initialization phase. It contains the base for the vector generation during an interrupt acknowledge. This allows the use of several peripherals. If not programmed interrupt vector is set to $OF.

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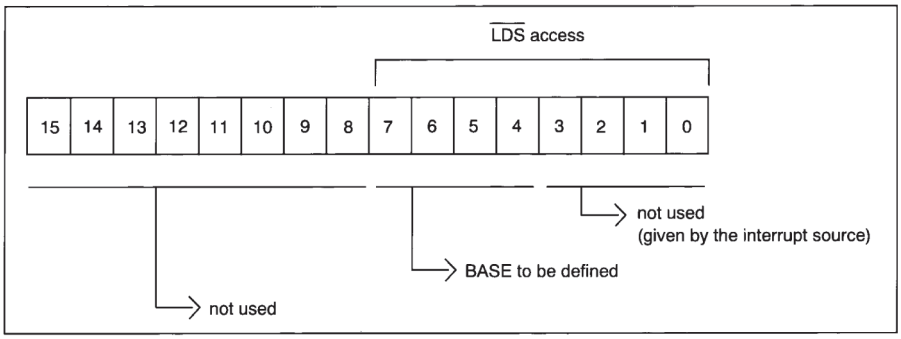
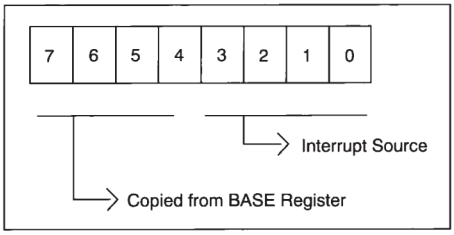
Figure 9-11. Base Register



- **The Interrupt Vector Number**

During an interrupt acknowledge cycle, an 8-bit vector number is presented to the microprocessor on D0-D7 lines. This vector number corresponds to the interrupt source requesting service. The format of this number is given below.

Figure 9-12.



Bit 3 to 0 : Interrupt source :

0000 : Msg on receiving channel 1
0001 : Msg on receiving channel 2
0010 : Msg on receiving channel 3
0011 : Msg on receiving channel 4
0100 : Msg on receiving channel 5
0101 : Msg on receiving channel 6
0110 : Msg on receiving channel 7
0111 : Msg on receiving channel 8
1000 : RX wrong parity
1001 : Not used
1010 : End of transmission on channel 1
1011 : FIFO of channel 1 empty
1100 : End of transmission on channel 2
1101 : FIFO of channel 2 empty
1110 : End of transmission on channel 3
1111 : FIFO of channel 3 empty

9.4 Self-test Description

A self-test has been implemented for the receiver control label matrix RAM and the transmitter FIFO. This test can be used to guarantee the good behavior of the different MRT's memories.

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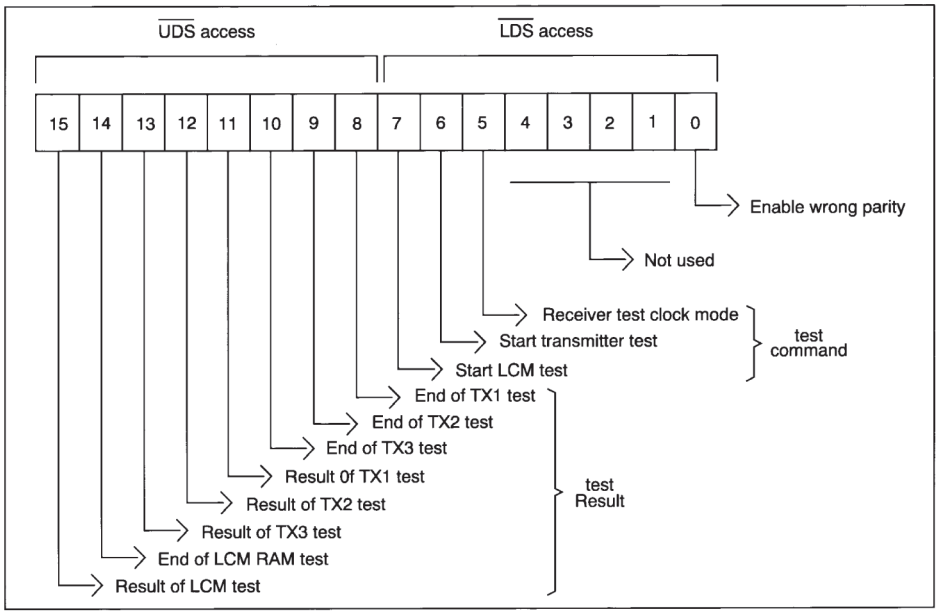
9.4.1 Register Description

Figure 9-13. Self-test Register



The self-test register can be split in three parts:

1. bit 0: Used to enable receiver wrong parity detection. This bit has been implemented to guarantee compatibility with previous designs:

   0: Receiver wrong parity detection disable,

   1: Receiver wrong parity detection enable.

2. Self-test command:

   bit 5: Receiver test clock mode:

   0: If CLK-SYS is less or equal to 10 MHz,

   1: If CLK-SYS is higher than 10 MHz.

   bit 6: Start transmitter self-test if a 0 to 1 transition is programmed (before a new self-test, the user must reprogram this bit to 0).

   bit 7: Start receiver Label Control Matrix self-test if a 0 to 1 transition is programmed (before a new self-test, the user must reprogram this bit to 0).

3. Self-test result:

   bit 8: 0: Transmitter 1 self-test is running,

   1: End of Transmitter 1 self-test.

   bit 9: 0: Transmitter 2 self-test is running,

   1: End of Transmitter 2 self-test.

   bit 10: 0: Transmitter 3 self-test is running,

   1: End of Transmitter 3 self-test.

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bit 11: Result of Transmitter 1 self-test:

0: (if bit 8 is set to 1) self-test pass,

1: Self-test fail.

bit 12: Request of Transmitter 2 self-test:

0: (if bit 9 is set to 1) self-test pass,

1: Self-test fail.

bit 13: Result of Transmitter 3 self-test:

0: (if bit 10 is set to 1) self-test pass,

1: Self-test fail.

bit 14: 0: Receiver Label Control Matrix self-test is running,

1: End of receiver Label Control Matrix self-test.

bit 15: Result of receiver LCM self-test:

0: (if bit 14 is set to 1) self-test pass,

1: Self-test fail.

9.4.2 Self-test Use

The self-test destroys the content of the tested memory. So, it could be used after system reset, during system initialization. Only one self-test (transmitters and receivers) can be performed after a reset. If the self-test must be restarted, the reset must be activated (then released) before the new self-test start.

To program the self-test:

1. If the receiver self-test will be used:
   set to 1 LCMWE bits (for all receivers).
2. If receiver self-test will be used and CLK-SYS is > 10 MHz:
   set to self-test register bit 5.
3. Start self-test:
   set to 1 self-test register bit 6 for Transmitter test,

   set to 1 self-test register bit 7 for Receiver RAM test.

   At this point, self-test is running. The test duration is:

   710 CLK-SYS periods for Transmitter self-test,

   2820 CLK-SYS periods for Receiver RAM test if self-test register bit 5 is 0,

   5640 CLK-SYS periods for Receiver RAM test if self-test register bit 5 is 1.

To read the self-test result, the user must:

1. poll the self-test register and wait for an end of test set to 1 (bits 8 to 10, bit 14) then,
2. read the self-test register again to have a valid result on bits 11, 12, 13, 15 according to the tests which end at point 1.

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Table 9-3. Memory MAP

Address	Access	Register	
0H	R/W	Receiver-control-register	Receiving channel 1
1H	W	Gap-register	
2H	R	Message-buffer MSW	
3H	R	Message-buffer LSW	
4H	R/W	Receiver-control-register	Receiving channel 2
5H	W	Gap-register	
6H	R	Message-buffer MSW	
7H	R	Message-buffer LSW	
8H	R/W	Receiver-control-register	Receiving channel 3
9H	W	Gap-register	
AH	R	Message-buffer MSW	
BH	R	Message-buffer LSW	
CH	R/W	Receiver-control-register	Receiving channel 4
DH	W	Gap-register	
EH	R	Message-buffer MSW	
FH	R	Message-buffer LSW	
10H	R/W	Receiver-control-register	Receiving channel 5
11H	W	Gap-register	
12H	R	Message-buffer MSW	
13H	R	Message-buffer LSW	
14H	R/W	Receiver-control-register	Receiving channel 6
15H	W	Gap-register	
16H	R	Message-buffer MSW	
17H	R	Message-buffer LSW	
18H	R/W	Receiver-control-register	Receiving channel 7
19H	W	Gap-register	
1AH	R	Message-buffer MSW	
1BH	R	Message-buffer LSW	
1CH	R/W	Receiver-control-register	Receiving channel 8
1DH	W	Gap-register	
1EH	R	Message-buffer MSW	
1FH	R	Message-buffer LSW	
20H	R/W	Transmit-control-register	Transmission channel 1
21H	W	Frequency-register	
22H	W	Message-FIFO MSW	
23H	W	Message-FIFO LSW	
24H	R/W	Transmit-control-register	Transmission channel 2
25H	W	Frequency-register	
26H	W	Message-FIFO MSW	
27H	W	Message-FIFO LSW	

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Table 9-3. Memory MAP (Continued)

Address	Access	Register	
28H 29H 2AH 2BH	R/W W W W	Transmit-control-register Frequency-register Message-FIFO MSW Message-FIFO LSW	Transmission channel 3
40H	R/W	Status-register	
41H 42H 43H	R/W W R/W	Mask-register Base-register Self-test register	
100H to 1FFH	R/W	Label-control-matrix	Receiving channels 1-8

MRT address 2CH to 3FH and 44H to FFH do not generate $\overline{\text{DTACK}}$ signal (illegal address).

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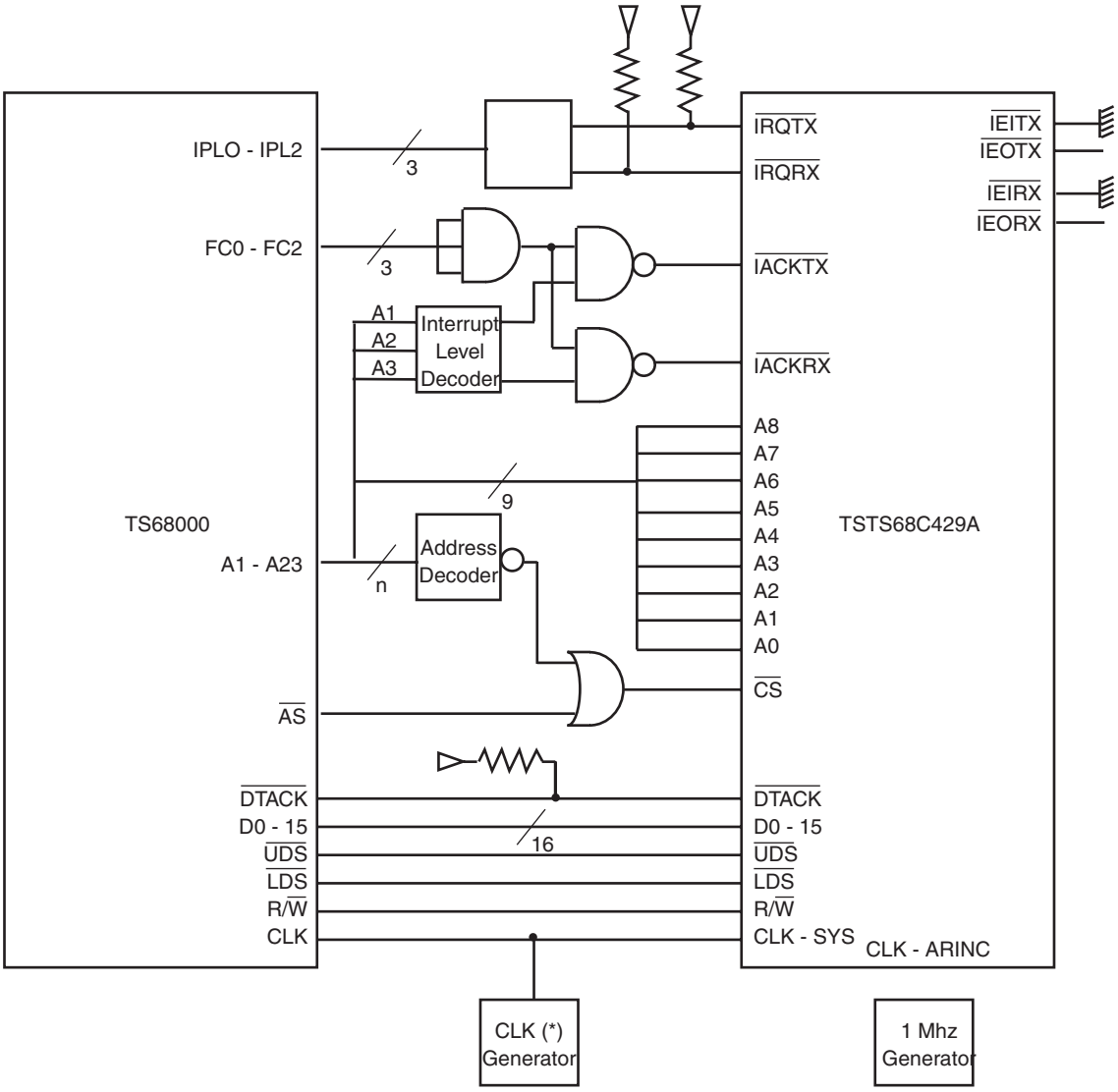
10. Application Notes

(for additional details order the AN 68C429A)

10.1 Microprocessor Interface

Figure 10-1. Typical Interface with TS68000



(*) This kind of application can also work with an independant clk

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Figure 10-2. Typical Interface with 68020/CPU 32 Core Microcontrollers

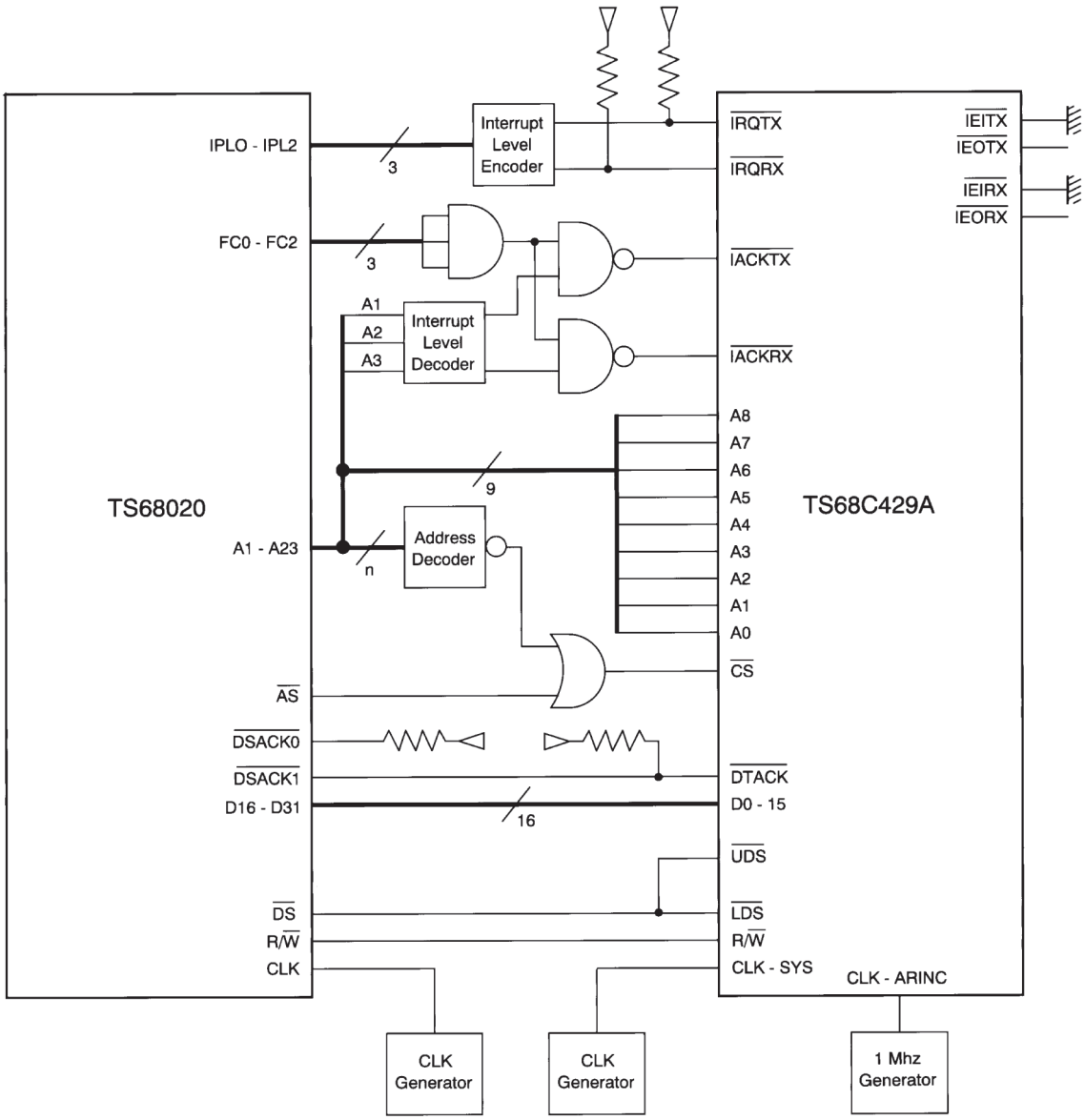

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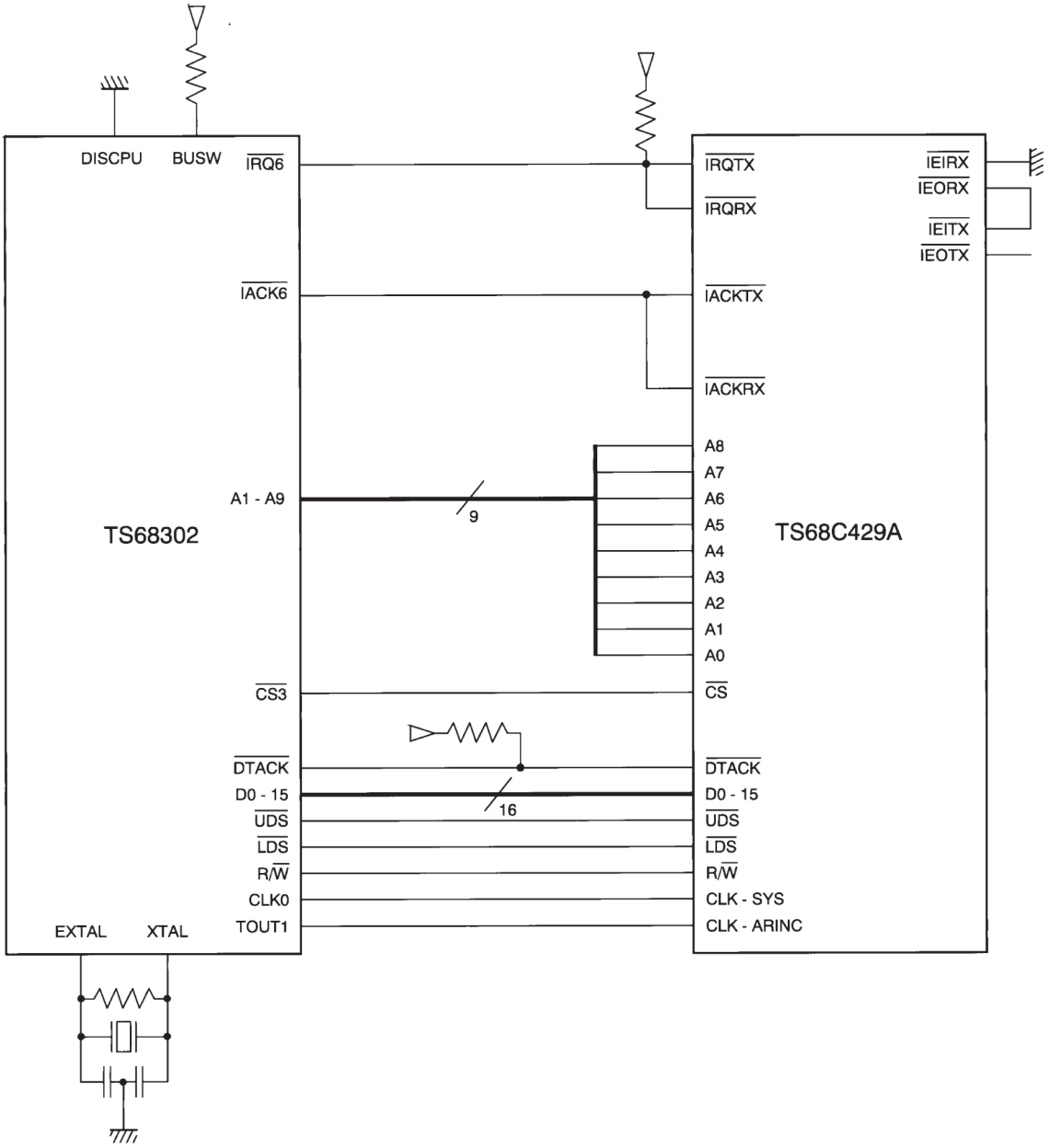
Figure 10-3. Typical Interface with 68302



In this example, receiver interrupts have a higher priority than transmitter interrupts.

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10.2 Programs Flow-chart

Figure 10-4. Initialization after Reset Flow-chart

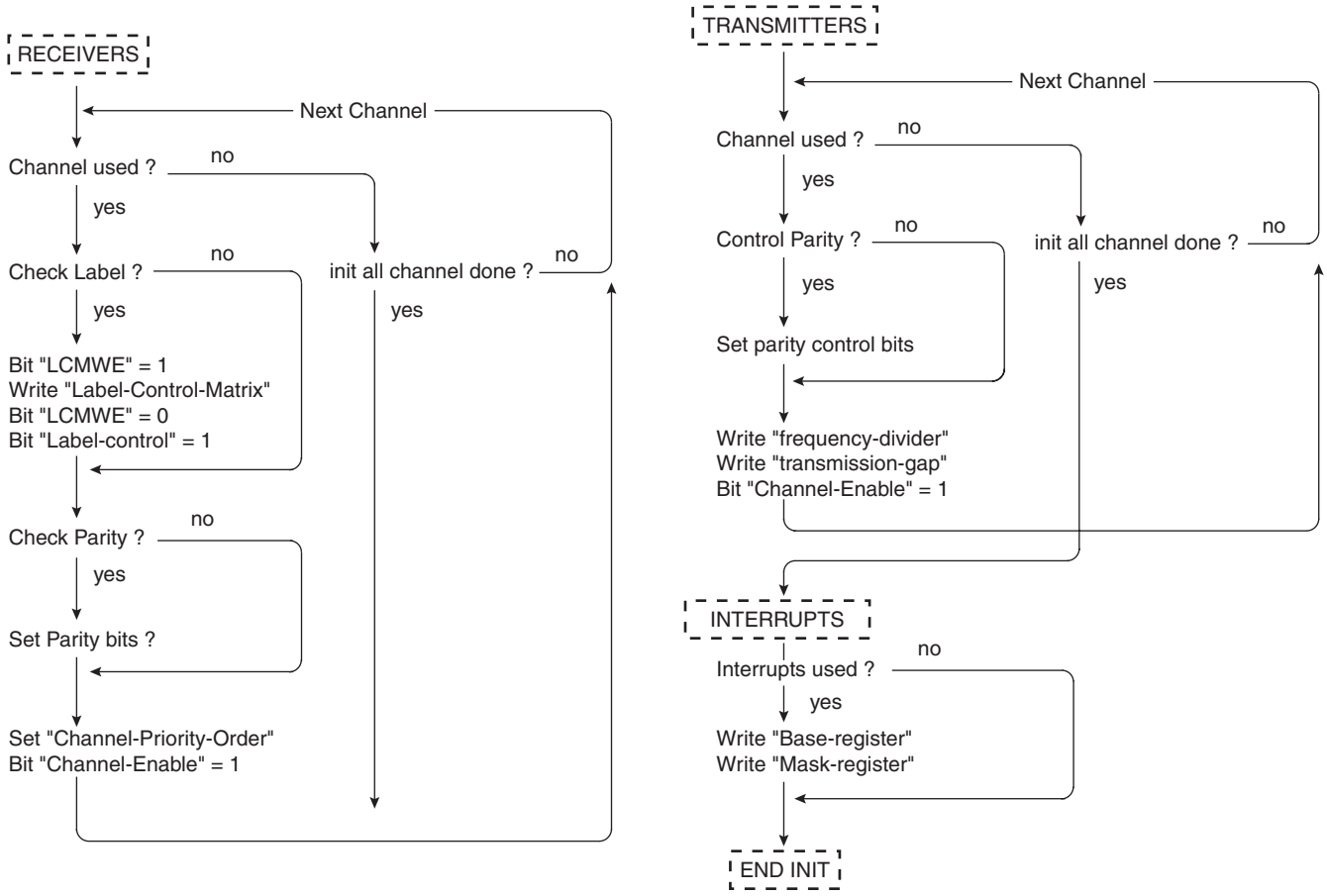

Figure 10-5. Receiver without Interrupt Flow-chart

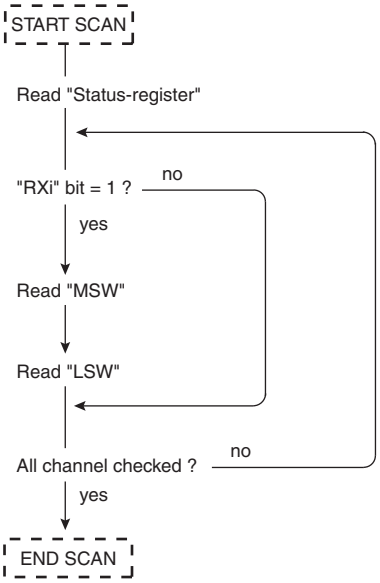

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Figure 10-6. Receiver with Interrupt Flow-chart

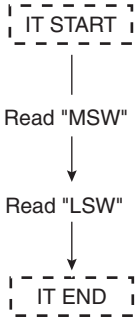

Figure 10-7. Transmitter without Interrupt Flow-chart

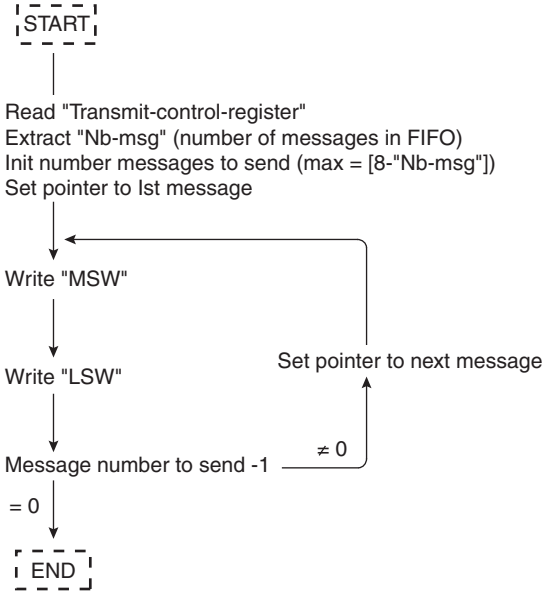

Figure 10-8. Transmitter with Interrupt Flow-chart

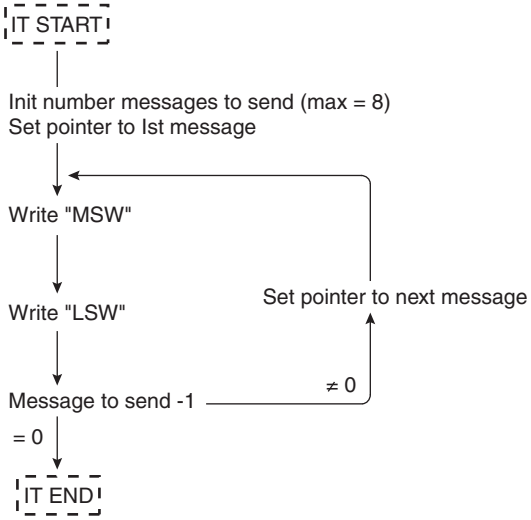

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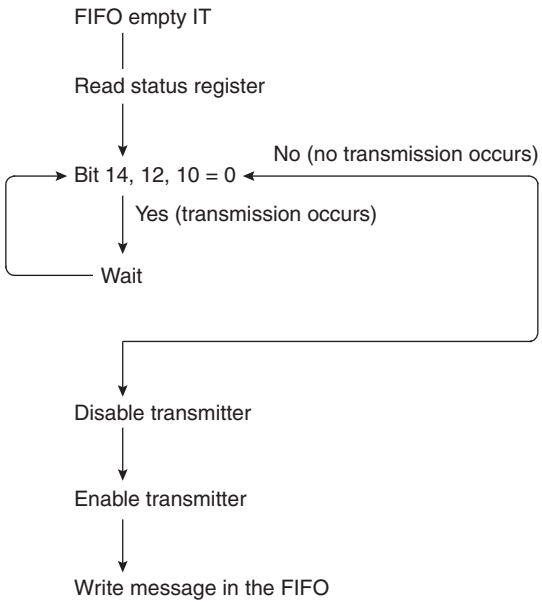
Figure 10-9. First FIFO Access



11. Preparation for Delivery

11.1 Packaging

Microcircuits are prepared for delivery in accordance with MIL-I-38535 or DESC.

11.2 Certificate of Compliance

e2v offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or DESC and guaranteeing the parameters not tested at temperature extremes for the entire temperature range.

12. Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

- Devices should be handled on benches with conductive and grounded surfaces.
- Ground test equipment, tools and operator.
- Do not handle devices by the leads.
- Store devices in conductive foam or carriers.
- Avoid use of plastic, rubber, or silk in MOS areas.
- Maintain relative humidity above 50 percent if practical.

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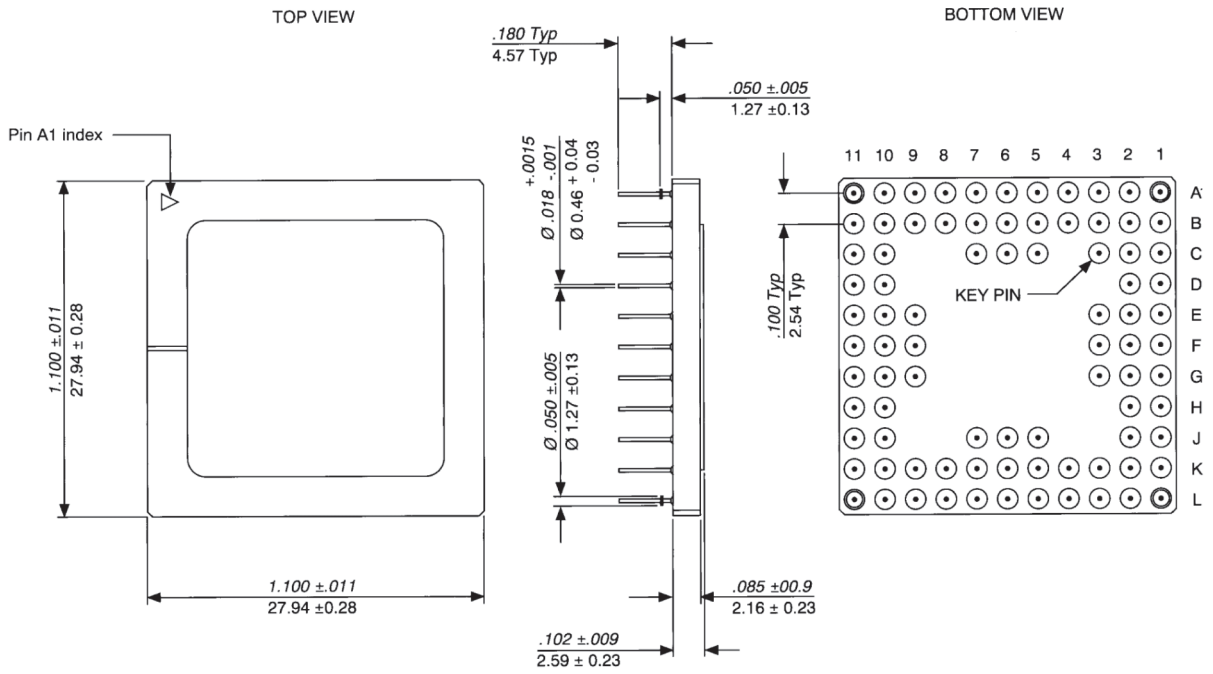
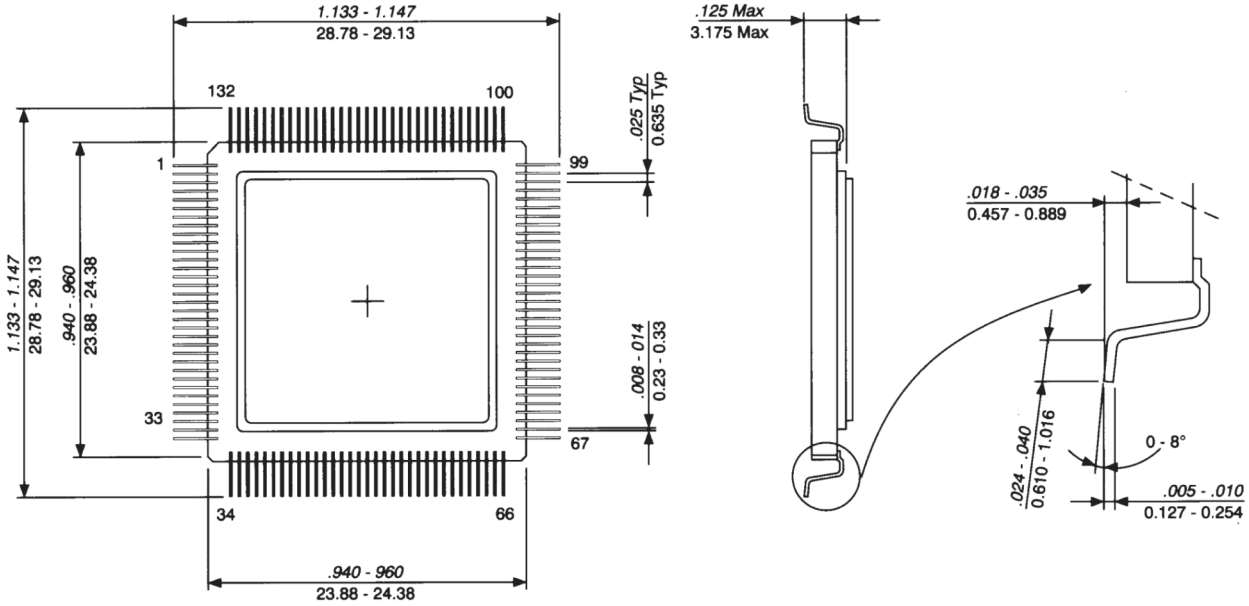
13. Package Mechanical Data

13.1 PGA 84



13.2 CQFP 132



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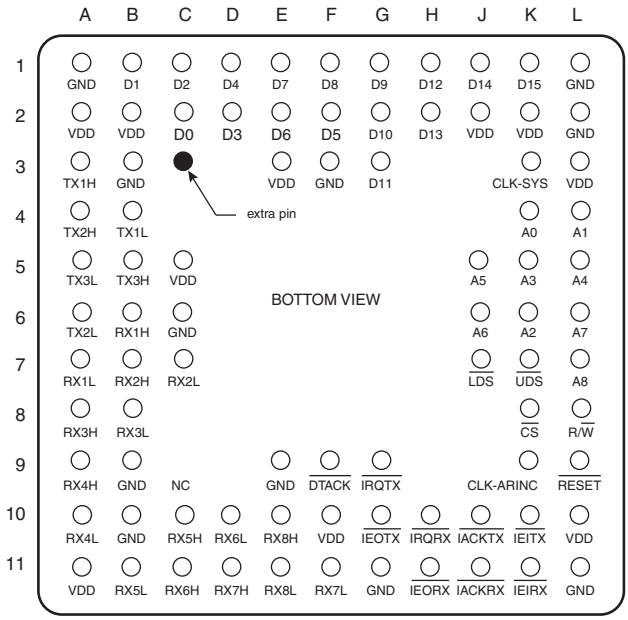
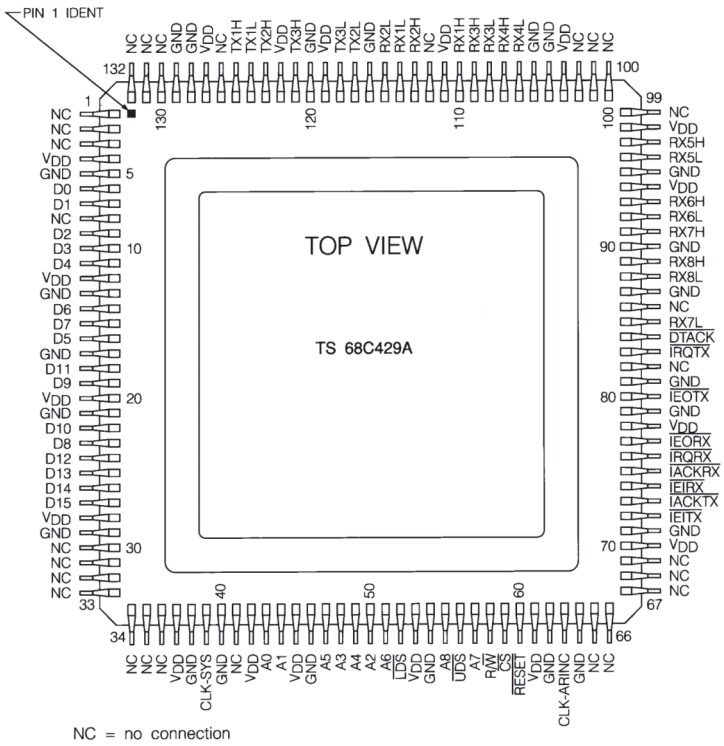
14. Terminal Connections

14.1 84-lead PGA Assignment



14.2 132-lead CQFP Assignment



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15. Ordering Information

15.1 Standard Product

e2v Part Number	Norms	Package	Temperature Range Tc (°C)	Detailed Qualification
TS68C429AMRA	e2v Standard	84-lead PGA	-55/+125	e2v internal
TS68C429AMFA	e2v Standard	132-lead CQFP	-55/+125	e2v internal
TS68C429AVRA	e2v Standard	84-lead PGA	-40/+85	e2v internal
TS68C429AVFA	e2v Standard	132-lead CQFP	-40/+85	e2v internal

15.2 HI-REL Products

e2v Part Number	Norms	Package	Temperature Range Tc (°C)	Detailed Qualification
TS68C429AMRBCA	MIL-STD-883	84-lead PGA	-55/+125	e2v internal
TS68C429AMFBCA	MIL-STD-883	132-lead CQFP	-55/+125	e2v internal

TS	68C429A	x	y	z	BC	A
Product Code (1)	Part Identifier	Temperature Range Tj (1)	Package (1)	Lead finish	Screening Level	Revision Level (1)
TS(X)(2)	68C429A	M: -55˚C, +125˚C V: -40˚C, +85˚C	R = PGA 84 F = CQFP132	1: Hot solder dip blank: Gold	BC = QML Class Q blank: standard	A

Notes: 1. For availability of the different versions, contact your local e2v sales office.

2. The letter X in the part number designates a "Prototype" product that has not been qualified by e2v. Reliability of a PCX part-number is not guaranteed and such part-number shall not be used in Flight Hardware. Product changes may still occur while shipping prototypes.

16. Document Revision History

Table 16-1 provides a revision history for this hardware specification.

Table 16-1. Document Revision History

Revision Number	Date	Substantive Change(s)
E	02/08	Table 7-1 on page 11: Removed I_{OH} of DTACK. Added DTACK in except pin
D	06/07	Added IOL IOH spec for DTACK signal
C	03/07	Name change from Atmel to e2v
B	07/06	Revised part-numbering consecutive to the change of wafer fab (see PCN #GC061204)
A	09/02	Initial revision

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