Description

The F2977 is a 50Ω single-pole double-throw (SP2T) reflective RF switch featuring high linearity and wide bandwidth. This device is optimized from 30MHz to 6GHz to support a multitude of wireless RF applications. The F2977 uses a single positive supply voltage of either +3.3V or +5.0V and is compatible with either 1.8V or 3.3V control logic.

Competitive Advantage

The F2977 provides extremely low insertion loss across the entire bandwidth while providing superb distortion performance.

- Low insertion loss
- High isolation
- Low distortion
- Fast switching
- No external matching required

Typical Applications

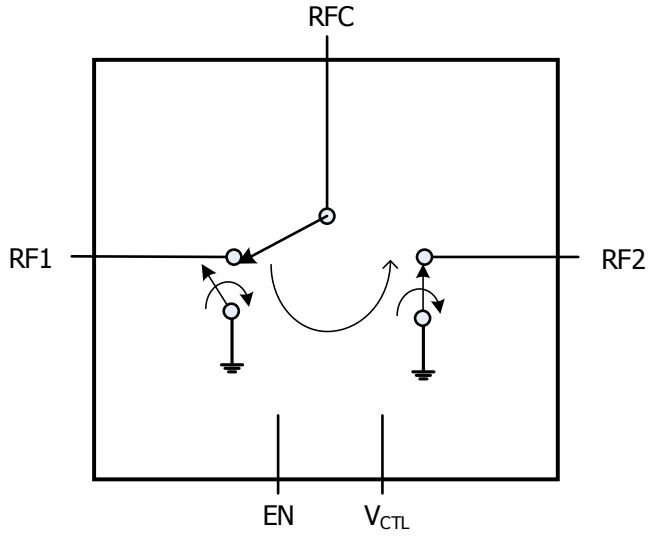
- Cellular BTS
- Cellular BTS small cell
- Transmit / Receive switching
- Post PA switching
- General purpose

Features

- Low insertion loss:
  - 0.38dB at 2.4GHz
  - 0.45dB at 6GHz
- High Isolation:
  - 39dB at 2.4GHz
- High Linearity:
  - IIP2 +125dBm at 2.4GHz
  - IIP3 +77dBm at 2.4GHz
- P0.1dB compression of +40dBm at 2.4GHz
- Second Harmonic: -95dBc at 900MHz
- Third Harmonic: -90dBc at 900MHz
- Supply voltage: +2.7V to +5.25V
- 1.8V and 3.3V compatible control logic
- -40°C to +105°C operating temperature range
- 2mm x 2mm, 12-pin VFQFP-N package

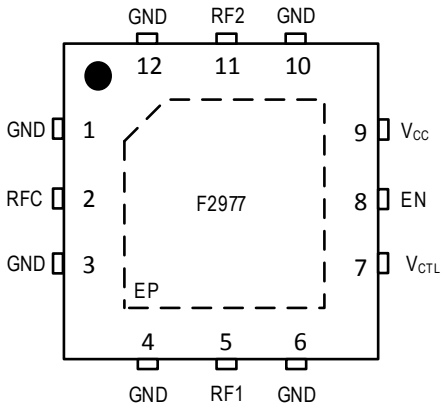
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 2mm x 2mm x 0.5mm 12-pin VFQFP-N, NEG12 – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
2	RFC	RF Common Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
3	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
4	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
5	RF1	RF1 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
6	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
7	V_{CTL}	Logic control pin.
8	EN	Active HIGH enable pin. If LOW, neither RF1 nor RF2 are connected to RFC. Pin is internally pulled up to 2.5V through a 500kΩ resistor.
9	V_{CC}	Power supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
10	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
11	RF2	RF2 Port. If this pin is not 0V DC, then an external coupling capacitor must be used.
12	GND	Internally grounded. Connect pin directly to paddle ground or as close as possible to pin with thru vias.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

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Absolute Maximum Ratings

Stresses beyond those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter		Symbol	Minimum	Maximum	Units
V_{CC} to GND		V_{CC}	-0.3	+5.5	V
V_{CTL}, EN		V_{LOGIC}	-0.3	Lower of (V_{CC} + 0.3, 3.9)	V
RF1, RF2, RFC		V_{RF}	-0.3	+0.3	V
Maximum Input CW Power, 50Ω, T_{EP} = 25°C, V_{CC} = 5.25V (any port, insertion loss state) [a]	30MHz ≤ f_{RF} ≤ 200MHz	P_{ABSCW1}		33	dBm
	200MHz < f_{RF} ≤ 6000MHz	P_{ABSCW2}		34	
Maximum Peak Power, 50Ω, T_{EP} = 25°C, V_{CC} = 5.25V (any port, insertion loss state) [a, b]	30MHz ≤ f_{RF} ≤ 200MHz	P_{ABSPK1}		38	dBm
	200MHz < f_{RF} ≤ 6000MHz	P_{ABSPK2}		39	
Maximum Junction Temperature		T_{JMAX}		+140	°C
Storage Temperature Range		T_{ST}	-65	+150	°C
Lead Temperature (soldering, 10s)		T_{LEAD}		+260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)		V_{ESDHBM}		2500 (Class 2)	V
Electrostatic Discharge – CDM (JEDEC 22-C101F)		V_{ESDCDM}		1000 (Class C3)	V

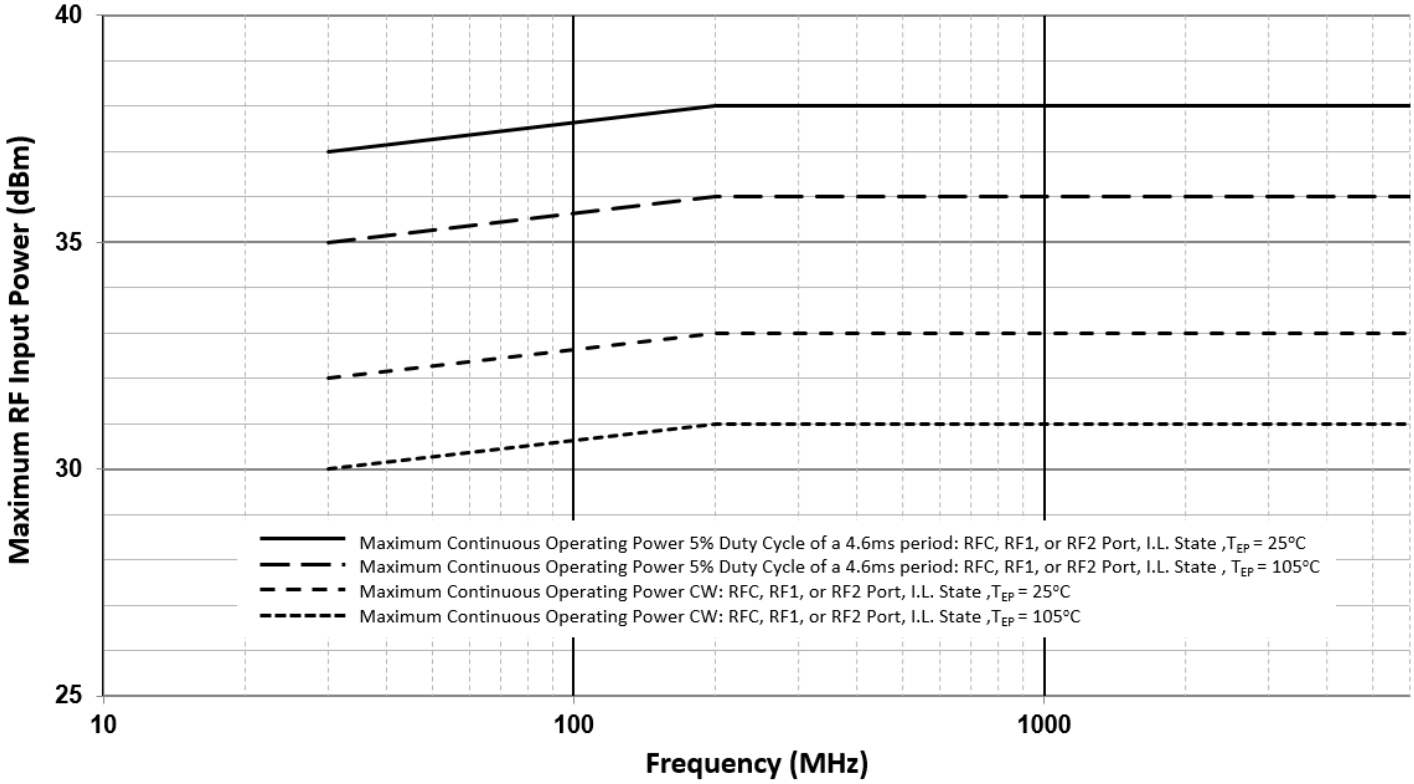
a. T_{EP} = Temperature of the exposed paddle.
b. 5% duty cycle of a 4.6ms period.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage	V_{CC}		2.7	3.3	5.25	V
Operating Temperature Range	T_{EP}	Exposed Paddle	-40		+105	°C
RF Frequency Range	f_{RF}		0.030		6	GHz
Maximum Operating Input Power	P_{MAX}	Insertion Loss State $Z_S = Z_L = 50\Omega$			See Figure 3	dBm
Port Impedance (RFC, RF1, RF2)	Z_{RF}	Insertion Loss State		50		Ω

Figure 3. Maximum Operating RF Input Power ($Z_S = Z_L = 50\Omega$)



General Specifications

Table 4. General Specifications

See F2977 Typical Application Circuit. Specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, EN = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, unless otherwise noted.

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Logic Input HIGH Threshold	V_{IH}	V_{CTL}, EN pins		1.17 [b]		Lower of (V_{CC}, 3.6)	V
Logic Input LOW Threshold	V_{IL}	V_{CTL}, EN pins		-0.3		0.6	V
Logic Current	I_{IH}, I_{IL}	V_{CTL}, EN pins (each pin)		***-10*** [a]		***+10***	µA
DC Current (V_{CC})	I_{CC}	Normal Operation			80	***150***	µA
		Standby (EN = LOW)			20	***35***	
Switching Rate	SW_{RATE}					25	kHz
Startup Time	T_{STRTUP}	From Standby State, 50% EN to 90% RF	No Change in RF Path		1.0		µs
			Change in RF Path		1.6		
Maximum Video Feed-Through, RFC Port	VID_{FT}	Peak transient during switching. $Z_S = Z_L = 50\Omega$. Measured with 20ns rise time, 0V to 3.3V (3.3V to 0V) control pulse applied to V_{CTL}.			12		mVp-p
Switching Time [c]	SW_{TIME}	50% V_{CTL} to 90% or 10% RF			1.5	3	µs

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. Measured at f_{RF} = 1GHz.

Electrical Characteristics

Table 5. Electrical Characteristics

See F2977 Typical Application Circuit. Specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, Z_S = Z_L = 50Ω, EN = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Insertion Loss (RFC to RF1, RF2)	IL	30MHz < f_{RF} ≤ 1GHz		0.33	0.53 [b]	dB
		1GHz < f_{RF} ≤ 2GHz [c]		0.36	***0.56*** [a]	
		2GHz < f_{RF} ≤ 3GHz		0.40		
		3GHz < f_{RF} ≤ 6GHz		0.45		
Isolation (RFC to RF1, RF2)	ISO1	30MHz < f_{RF} ≤ 1GHz	43	48		dB
		1GHz < f_{RF} ≤ 2GHz	36	42		
		2GHz < f_{RF} ≤ 3GHz	31	37		
		3GHz < f_{RF} ≤ 6GHz		27		
Isolation (RF1 to RF2, RF2 to RF1)	ISO2	30MHz < f_{RF} ≤ 1GHz	40	45		dB
		1GHz < f_{RF} ≤ 2GHz	33	38		
		2GHz < f_{RF} ≤ 3GHz	29	34		
		3GHz < f_{RF} ≤ 6GHz		26		
Return Loss (RFC, RF1, RF2) (Insertion loss states)	RL	30MHz < f_{RF} ≤ 1GHz		28		dB
		1GHz < f_{RF} ≤ 2GHz		26		
		2GHz < f_{RF} ≤ 3GHz		26		
		3GHz < f_{RF} ≤ 6GHz		25		

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. Minimum or maximum specification guaranteed by test at 2GHz and by design characterization over the whole frequency range.

Electrical Characteristics

Table 6. Electrical Characteristics

See F2977 Application Circuit. Specifications apply when operated with V_{CC} = +3.3V, T_{EP} = +25°C, Z_S = Z_L = 50Ω, EN = HIGH, single tone signal applied at RF1 or RF2 and measured at RFC, EVKit trace and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Input 0.1dB Compression [c]	P0.1dB	f_{RF} = 30MHz		40		dBm
		f_{RF} = 2.4GHz		40		
		f_{RF} = 6.0GHz		40		
Input IP3 (RF1, RF2 to RFC)	IIP3	f_{RF} = 2.4GHz P_{IN} = +24dBm/tone 100MHz spacing		77		dBm
Input IP2 (RF1, RF2 to RFC)	IIP2	f_1 = 700MHz f_2 = 1.7GHz P_{IN} = +24dBm/tone Measure 2.4GHz product		125		dBm
		f_1 = 2.4GHz f_2 = 3.5GHz P_{IN} = +24dBm/tone Measure 5.9GHz product		120		
Second Harmonic (RF1, RF2 to RFC)	H2	f_{IN} = 900MHz, P_{IN} = +35dBm		-95	-85 [b]	dBc
		f_{IN} = 1.8GHz, P_{IN} = +33dBm		-86	-76	
Third Harmonic (RF1, RF2 to RFC)	H3	f_{IN} = 900MHz, P_{IN} = +35dBm		-90	-75	dBc
		f_{IN} = 1.8GHz, P_{IN} = +33dBm		-89	-74	
Spurious Output (No RF Applied)	P_{SPUR1}	f_{OUT} ≥ 5MHz All unused ports terminated		-133		dBm
	P_{SPUR2}	f_{OUT} < 5MHz All unused ports terminated		-120		

a. Items in min/max columns in ***bold italics*** are guaranteed by test.
b. Items in min/max columns that are not bold italics are guaranteed by design characterization.
c. The input 0.1dB compression point is a linearity figure of merit. Refer to Figure 3 for the maximum RF operating input power levels.

Thermal Characteristics

Table 7. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	102	°C/W
Junction to Case Thermal Resistance (Case is defined as the exposed paddle)	θ_{JC_BOT}	56	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOCs)

Unless otherwise noted:

- V_{CC} = +3.3V
- T_{EP} = 25°C
- EN = HIGH
- $Z_S = Z_L = 50\Omega$
- All temperatures are referenced to the exposed paddle
- Evaluation Kit traces and connector losses are de-embedded

Typical Performance Characteristics [1]

Figure 4. RF1 to RFC Insertion Loss

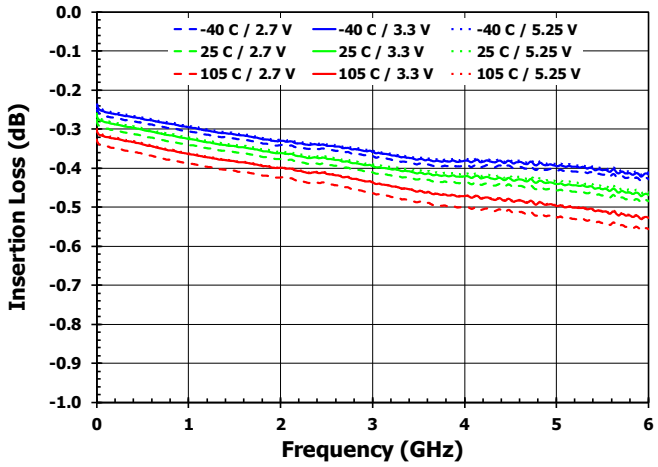


Figure 5. RF2 to RFC Insertion Loss

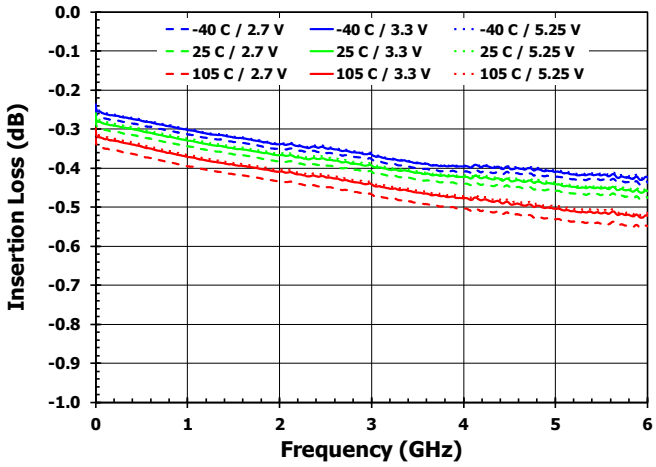


Figure 6. RF1 to RFC Isolation [RF2 On State]

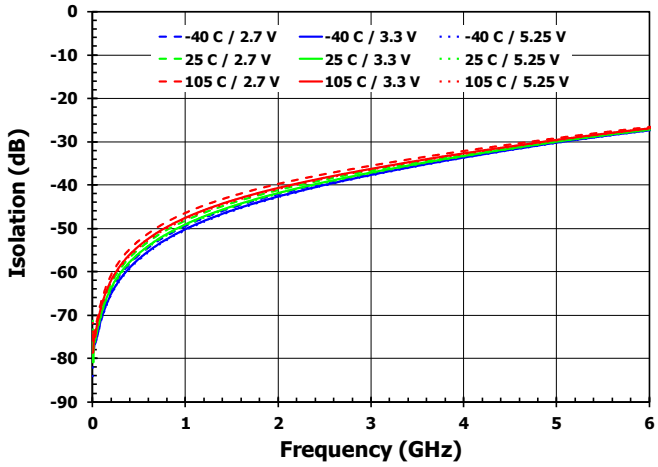


Figure 7. RF2 to RFC Isolation [RF1 On State]

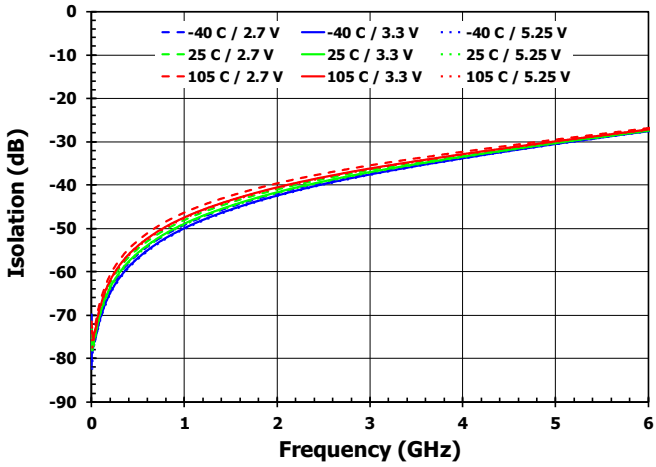


Figure 8. RF1 to RF2 Isolation [RF1 On State]

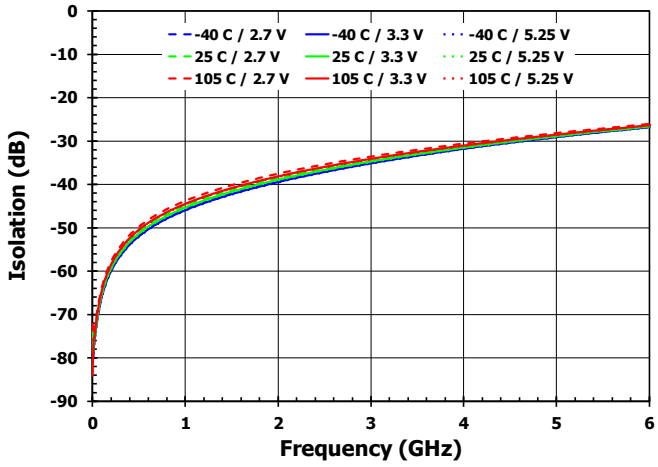
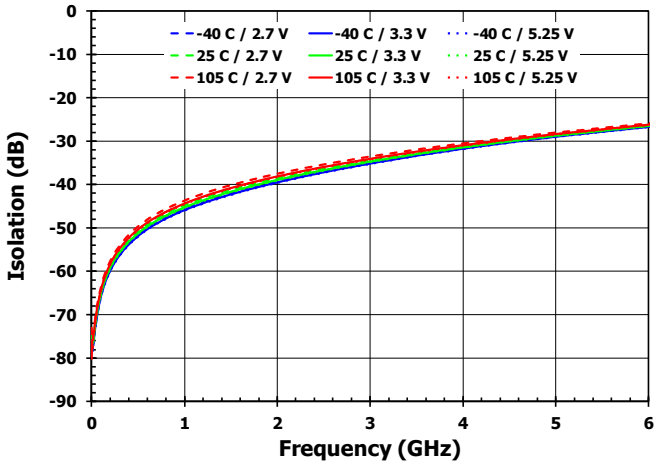


Figure 9. RF2 to RF1 Isolation [RF2 On State]



Typical Performance Characteristics [2]

Figure 10. RFC Return Loss [RF1 On State]

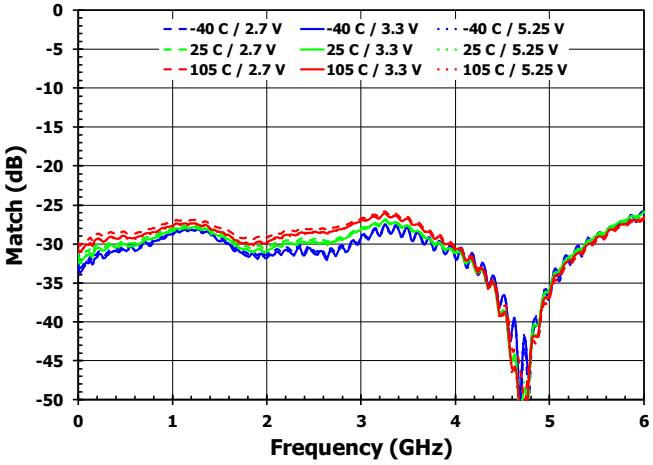


Figure 11. RFC Return Loss [RF2 On State]

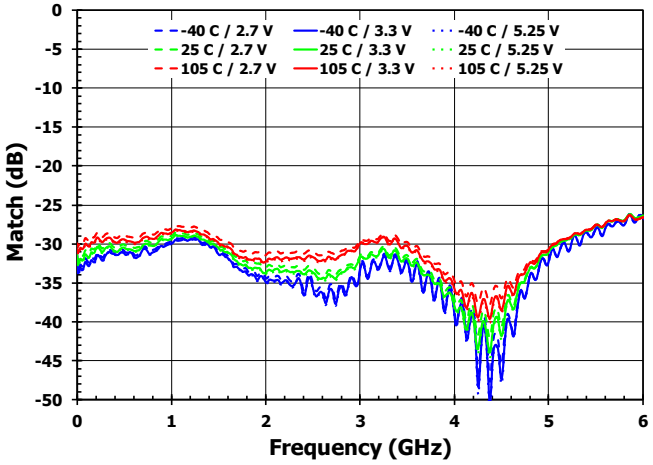


Figure 12. RF1 Return Loss [RF1 On State]

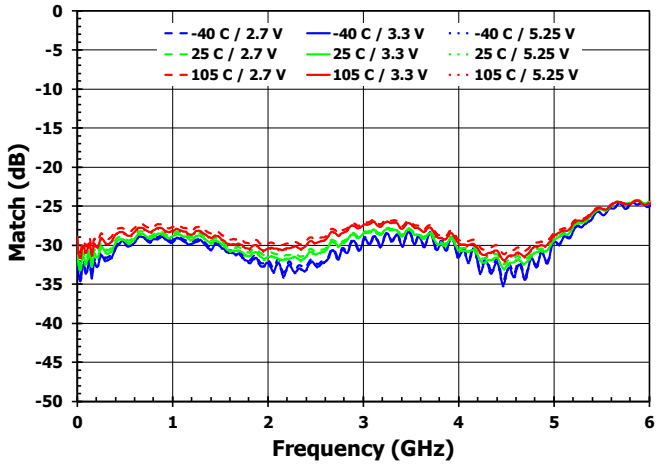


Figure 13. RF2 Return Loss [RF2 On State]

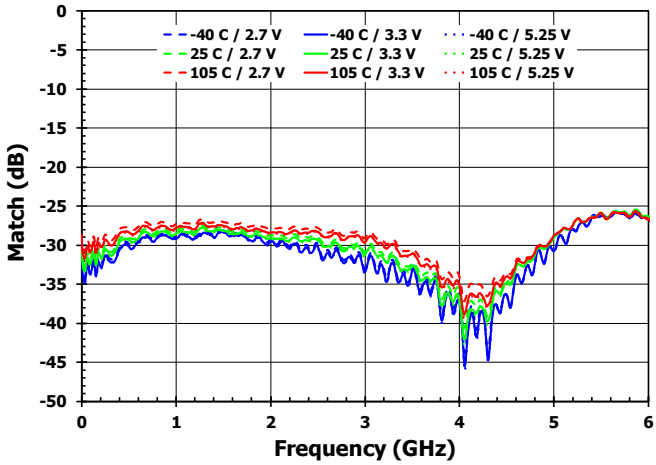


Figure 14. Switching Time [Isolation to Insertion Loss State]

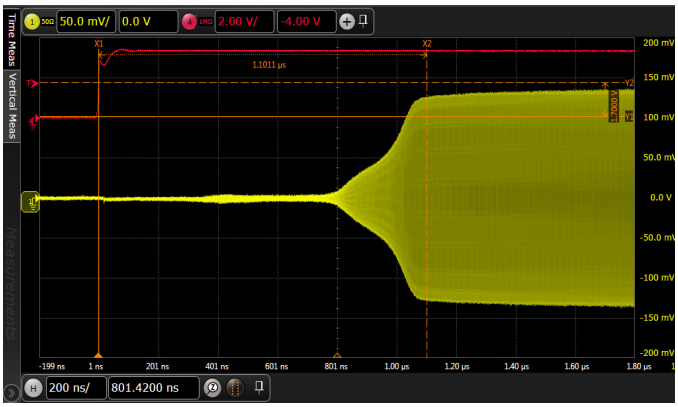


Figure 15. Switching Time [Insertion Loss to Isolation State]

Control Mode

Table 8. Switch Control Truth Table

V_{CTL} (pin 7)	EN (pin 8)	Switch State
LOW	HIGH	RFC to RF1 Insertion Loss State
HIGH	HIGH	RFC to RF2 Insertion Loss State
Don't Care	LOW	Standby

Application Information

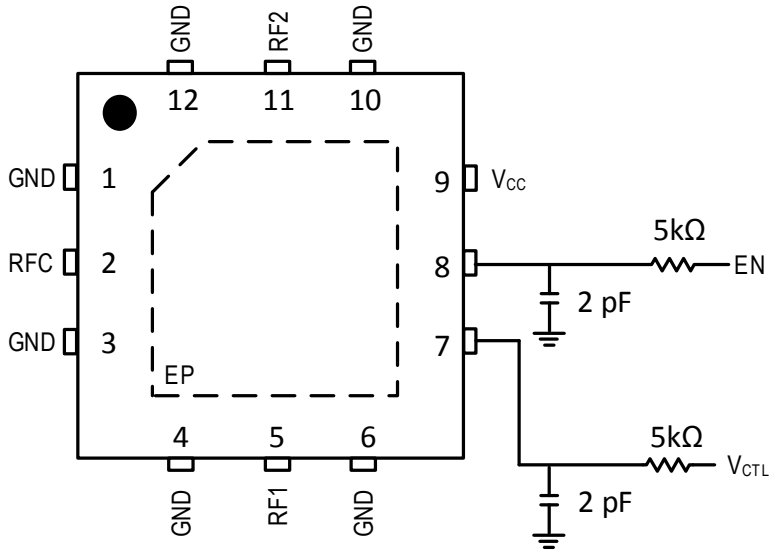
Power Supplies

A common V_{CC} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V / 20µs. In addition, all control pins should remain at 0V (+/- 0.3V) while the supply voltage ramps up or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 7 and 8 as shown below.

Figure 16. Control Pin Interface Schematic



Evaluation Kit Picture

Figure 17. Top View

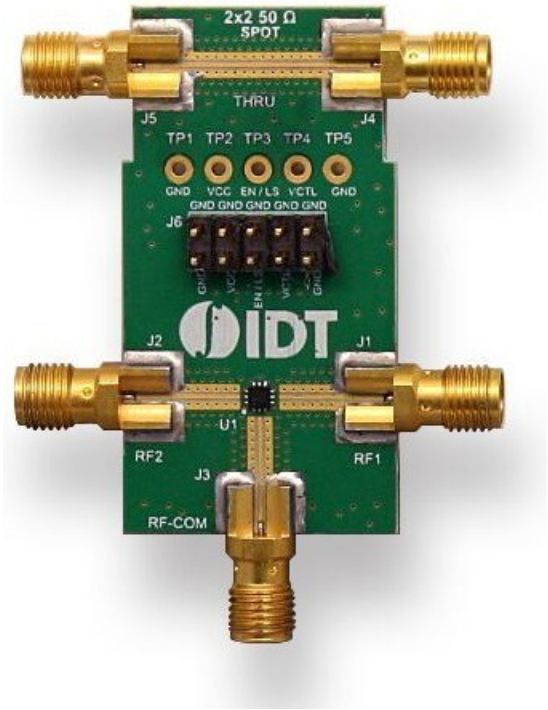


Figure 18. Bottom View

Evaluation Kit / Applications Circuit

Figure 19. Electrical Schematic

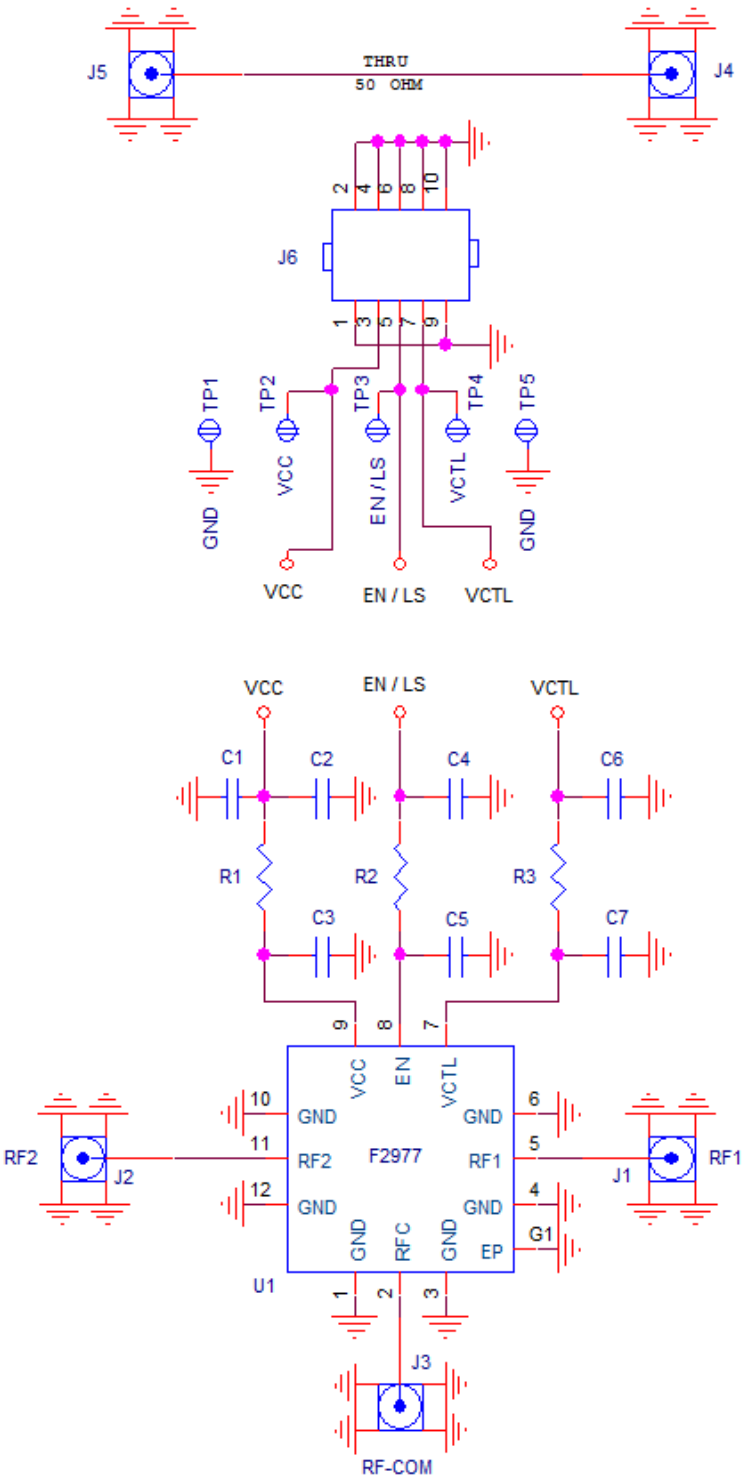


Table 9. Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1 – C7	0	Not Installed (0402)		
R1 – R3	3	0Ω 1/10W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
J1 – J5	5	SMA Edge Mount	142-0761-881	Cinch Connectivity
J6	1	Conn Header 10 Pos 0.100” Str 15 Au	68602-210HLF	Amphenol FCI
TP1, TP2, TP3, TP4, TP5	0	Not Installed Test Point Loop		
U1	1	SP2T Switch 2mm x 2mm 12-pin TQFN	F2977NEGK	IDT
	1	Printed Circuit Board	F2972 50Ω PCB	IDT

Evaluation Kit (EVKit) Operation

External Supply Setup

Set up a V_{CC} power supply in the voltage range of +2.7V to +5.25V with the power supply output disabled.

Connect the disabled V_{CC} supply connection to J6 pin 3 and GND to J6 pin 1, 2, 4, 6, 8, 9, or 10.

Logic Control Setup

With the logic control lines disabled, set the HIGH and LOW logic levels to satisfy the levels stated in the electrical specifications table.

Connect the disabled logic control lines to J6 EN / LS (pin 5) and V_{CTL} (pin 7).

See Table 8 for the logic truth table.

Turn On Procedure

Setup the supplies and EVKit as noted in the External Supply Setup and Logic Control Setup sections above.

Enable the V_{CC} supply.

Enable the logic control signals.

Set the logic setting to achieve the desired Table 8 configuration. Note that external control logic should not be applied without V_{CC} being present.

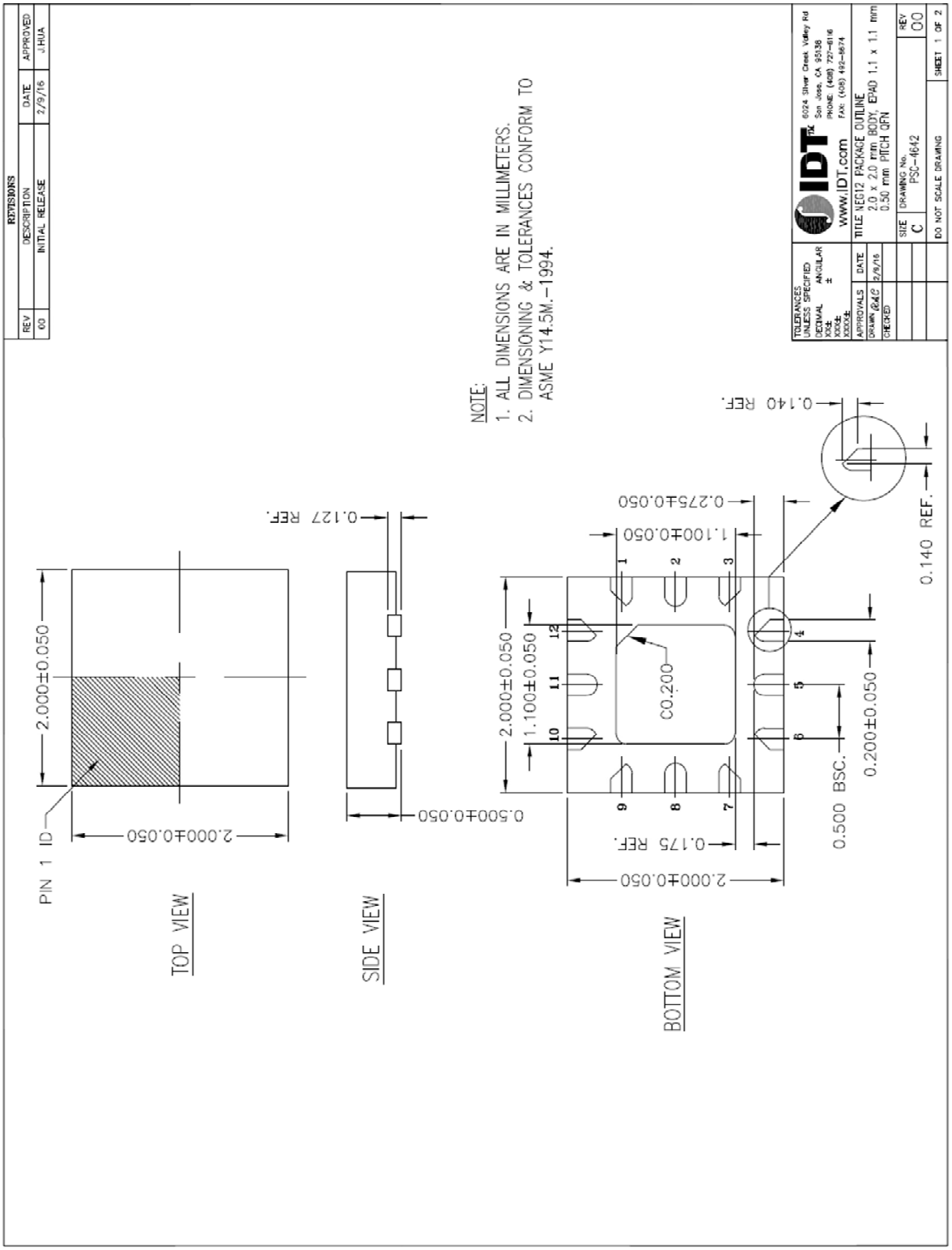
Turn Off Procedure

Set the logic control pins to a logic LOW.

Disable the V_{CC} supply.

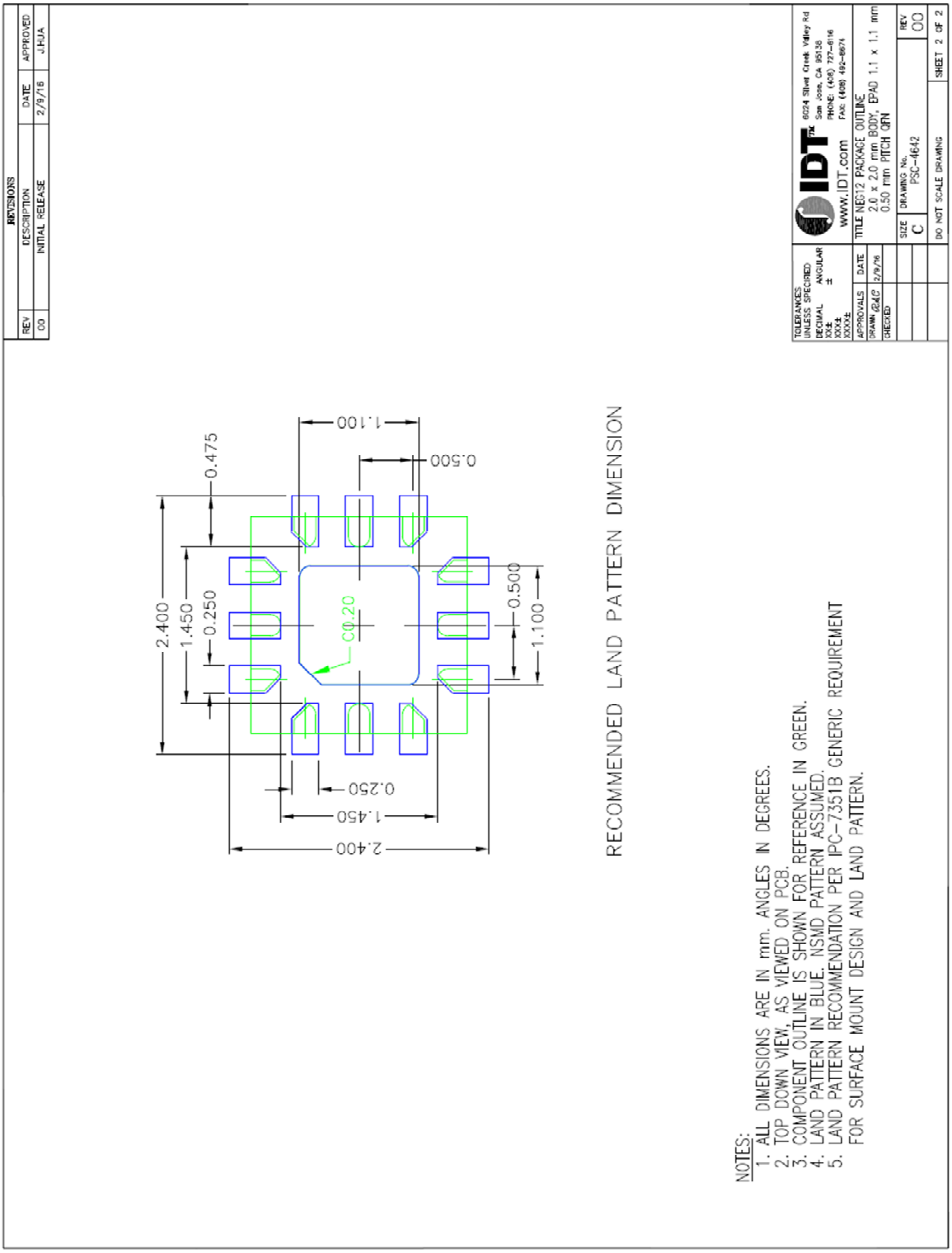
Package Drawings

Figure 20. Package Outline Drawing NEG12 PSC-4642

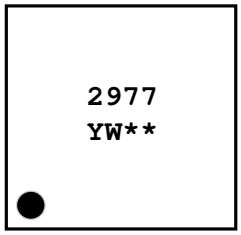


Recommended Land Pattern

Figure 21. Recommended Land Pattern NEG12 PSC-4642



Marking Diagram



Line 1 - 2977 = Abbreviated part number.
Line 2 - Y = Year code.
Line 2 - W = Work week code.
Line 2 - ** = Sequential alpha for lot traceability.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2977NEGK	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Cut Reel	-40°C to +105°C
F2977NEGK8	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Tape and Reel	-40°C to +105°C
F2977EVBI	Evaluation Board			

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Revision History

Revision	Revision Date	Description of Change
Rev O	2017-May-19	Initial Release

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