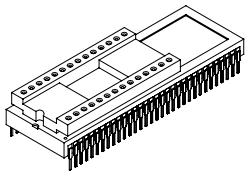
SONY

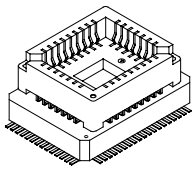
CXP85200A/85290A

CMOS 8-bit 1-chip Microcomputer

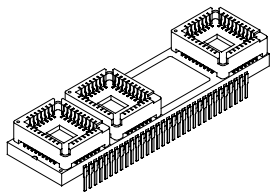
Piggyback/ evaluator type

64 pin PSDIP (Ceramic) 64 pin PQFP (Ceramic)





64 pin PSDIP (Ceramic)



Description

The CXP85200A/85290A are CMOS 8-bit 1-chip microcomputers that serve as both piggyback and evaluator. The CXP85200A/85290A is developed for evaluating the function of the CXP85112B/85116B/85220A/85224A/85228A/85232A.

Note that CXP85200A corresponds to the fixed font, and CXP85290A corresponds to the custom font respectively.

Features

- Instruction set which supports a wide array of data types
  - 213 types of instructions which include 16-bit calculations, multiplication and division arithmetic, and boolean bit operations.
- Minimum instruction cycle 1µs/4MHz
- EPROM 27C256
  LCC type 27C256
- Incorporated RAM capacity 448 bytes
- EPROM for custom font (CXP85290A only)
  LCC type 27C256
  (used volume is 4K bytes)
- Peripheral functions
  - On-screen display function 12 × 16 dots, 128 types, 8 colors, 21 characters × 4 lines
    (More than 5 lines possible)
    Double scanning mode, jitter elimination circuit
  - I^2C bus interface
  - PWM output 14 bits, 1 channel
    6 bits, 8 channels
  - Remote control receiving circuit 8-bit pulse measurement counter, 6-stage FIFO
  - A/D converter 4 bits, 4 channels, successive approximation system
    (conversion time of 40µs/4MHz)
  - HSYNC counter
  - Power supply frequency counter
  - Watchdog timer
  - Serial I/O 8-bit clock synchronized
  - Timers 8-bit timer, 8-bit timer/counter, 19-bit time-base timer
- Interrupts 14 factors, 14 vectors multi-interruption possible
- Standby mode Sleep
- Package 64-pin ceramic SDIP/QFP

Structure

Silicon gate CMOS IC

Note) Optional mask depends on the type of the CXP85200A/85290A. Refer to the product list for details.

Purchase of Sony's I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specifications as defined by Philips.

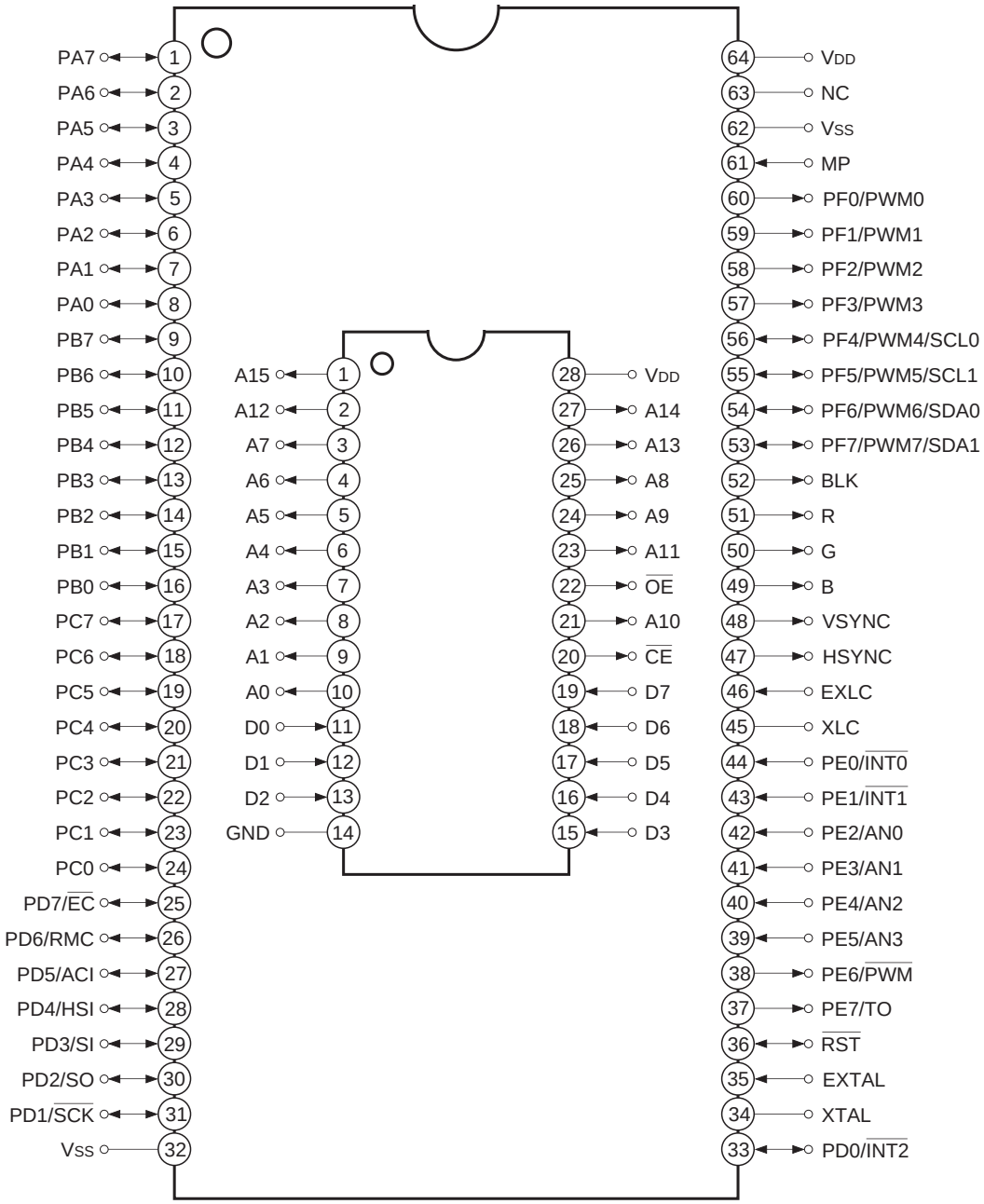
Sony reserves the right to change products and specifications without prior notice. This information does not convey any license by any implication or otherwise under any patents or other right. Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits.

E94333A7Y-PS

CXP85200A

Pin Assignment: Piggyback mode 1

(Top View) 64 pin PSDIP Package

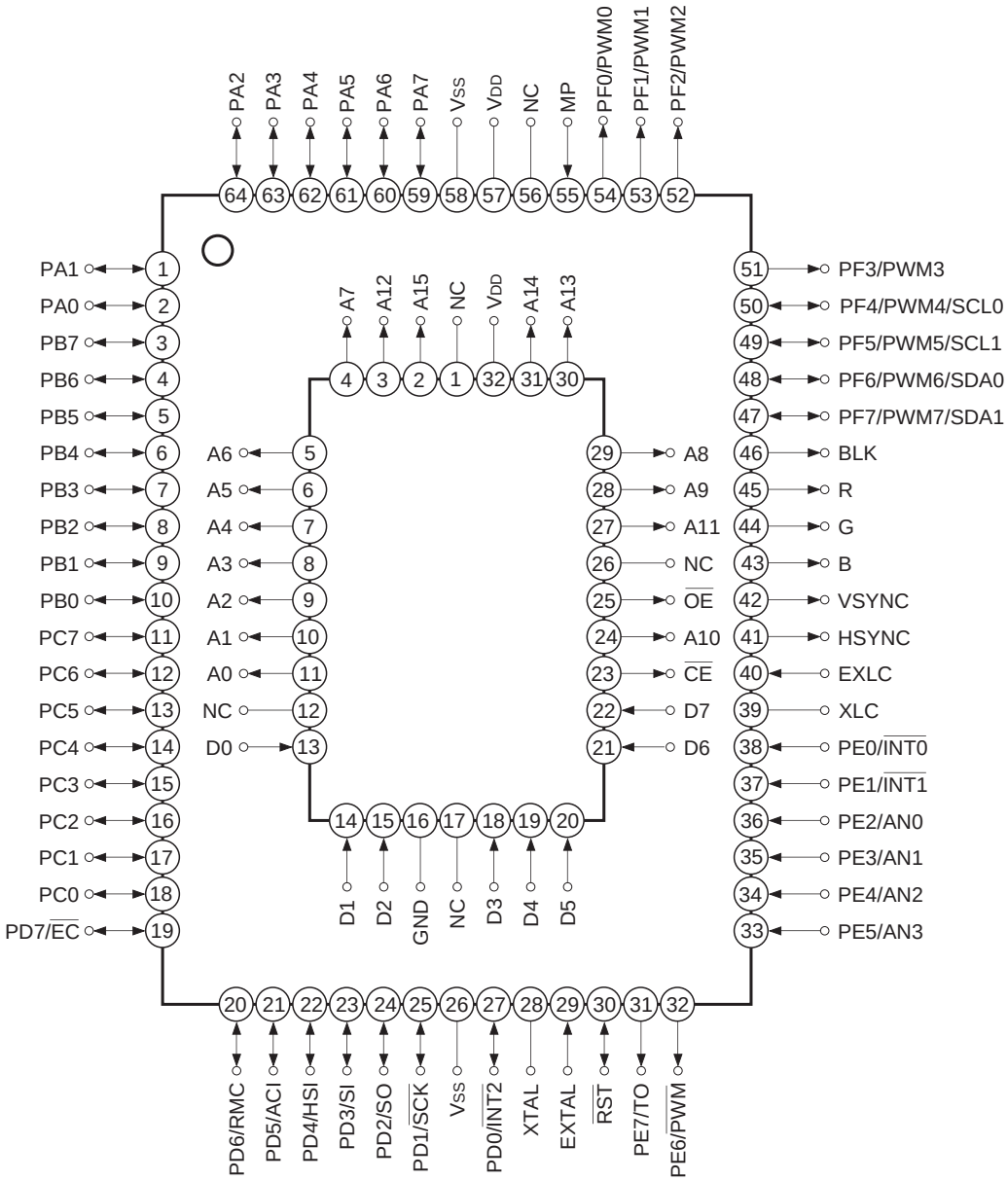


Note) 1. NC (Pin 63) is always connected to V_{DD}.
2. Vss (Pins 32 and 62) are always connected to GND.
3. MP (Pin 61) is always connected to GND.

CXP85200A

Pin Assignment: Piggyback mode 2

(Top View) 64 pin PQFP Package

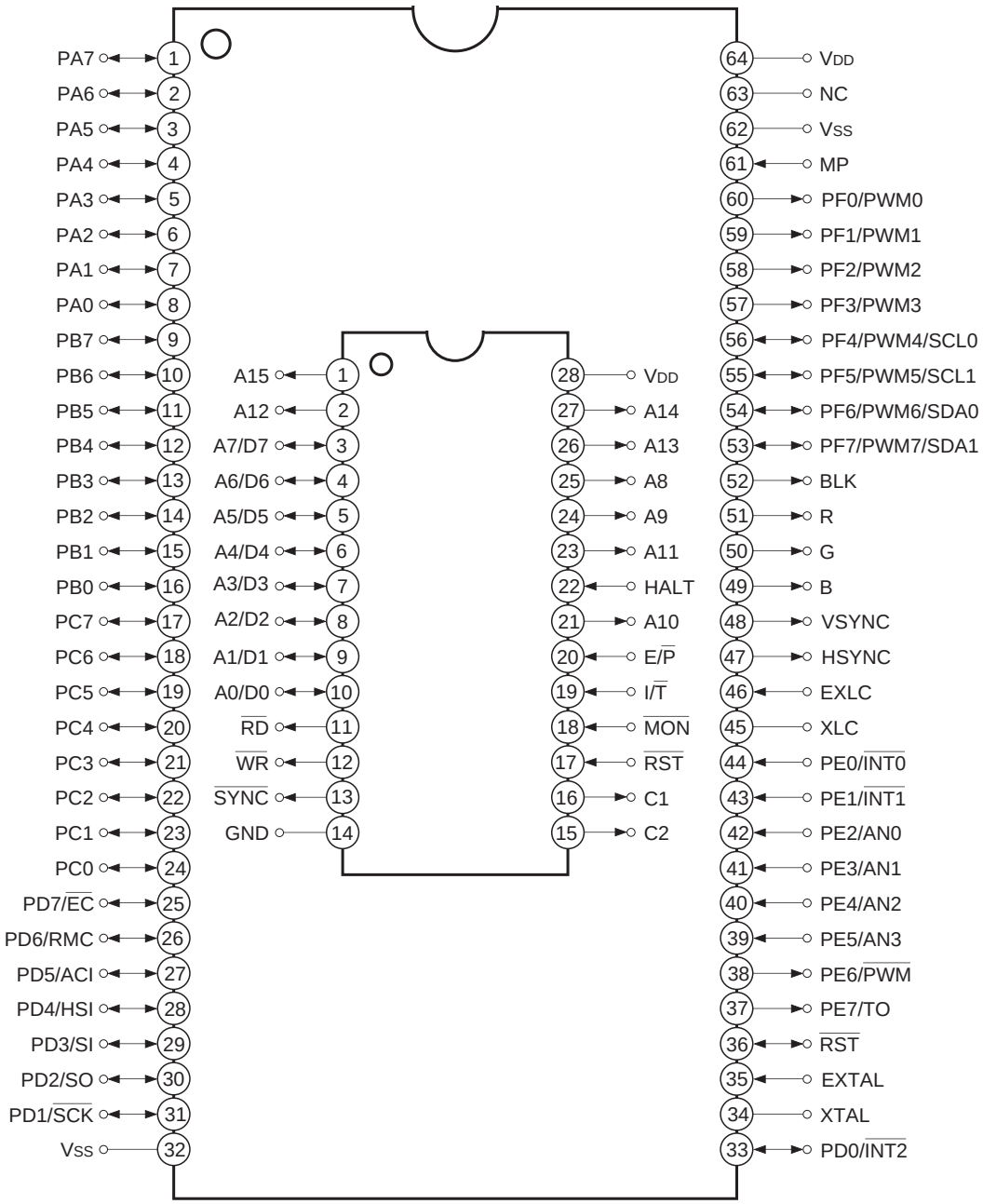


Note) 1. NC (Pin 56) is always connected to V_{DD}.
2. Vss (Pins 26 and 58) are always connected to GND.
3. MP (Pin 55) is always connected to GND.

CXP85200A

Pin Assignment: Evaluator Mode 1

(Top View) 64 pin PSDIP Package

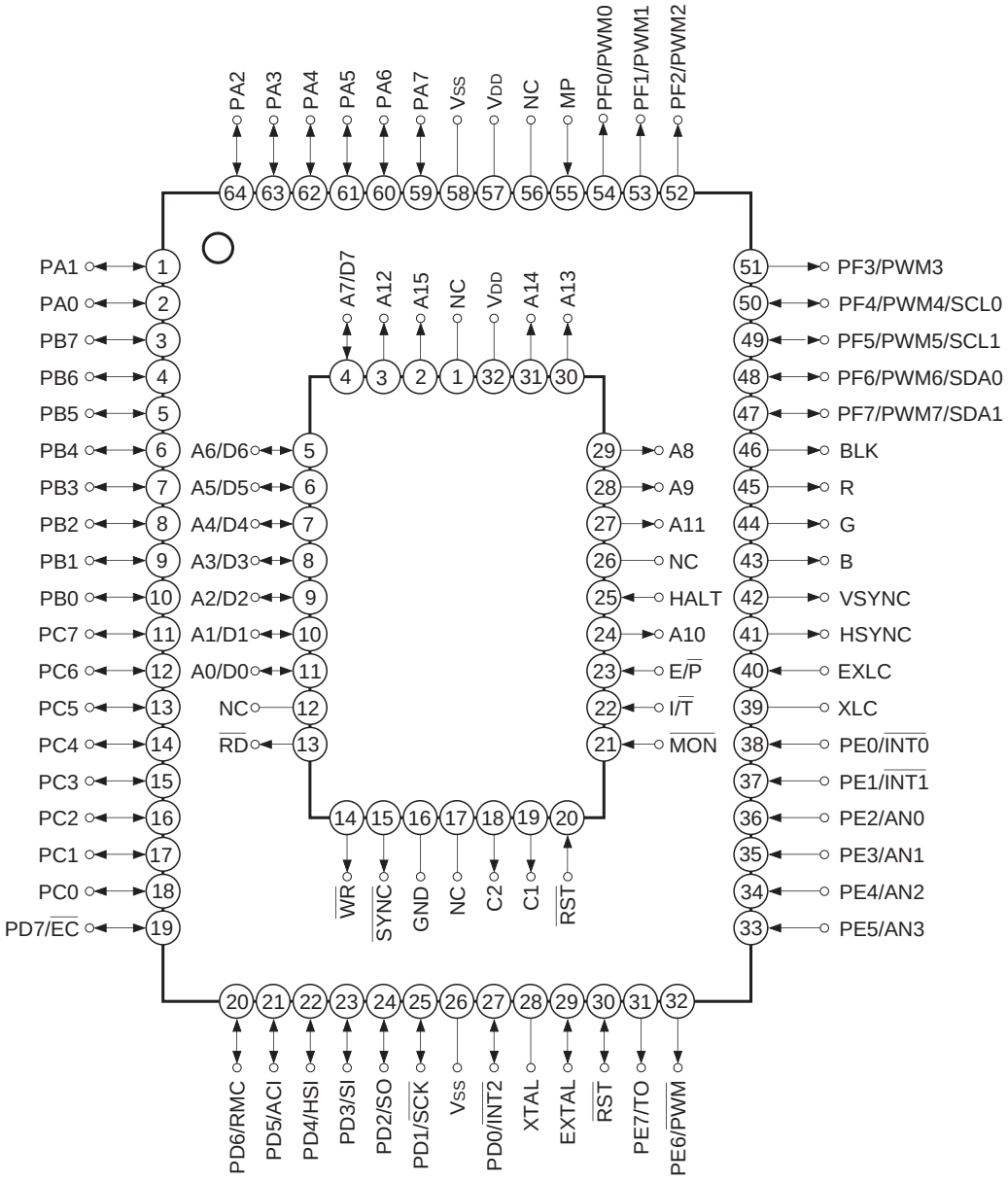


Note) 1. NC (Pin 63) is always connected to V_{DD}.
2. Vss (Pins 32 and 62) are always connected to GND.
3. MP (Pin 61) is always connected to GND.

CXP85200A

Pin Assignment: Evaluator Mode 2

(Top View) 64 pin PQFP Package

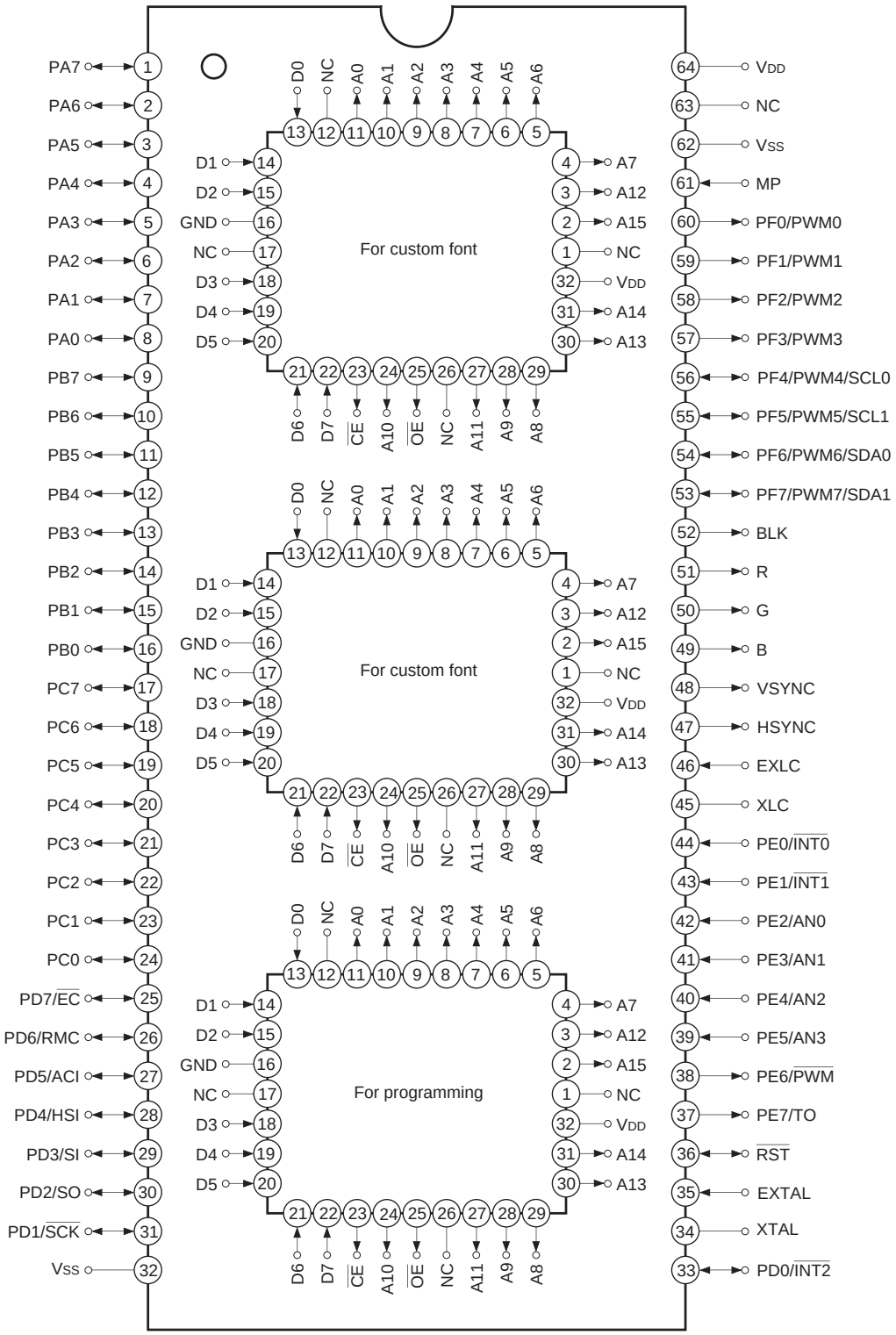


Note) 1. NC (Pin 56) is always connected to V_{DD}.
2. Vss (Pins 26 and 58) are always connected to GND.
3. MP (Pin 55) is always connected to GND.

CXP85290A

Pin Assignment: Piggyback Mode

(Top View) 64 pin PSDIP Package



Note) 1. NC (Pin 63) is always connected to V_{DD}.

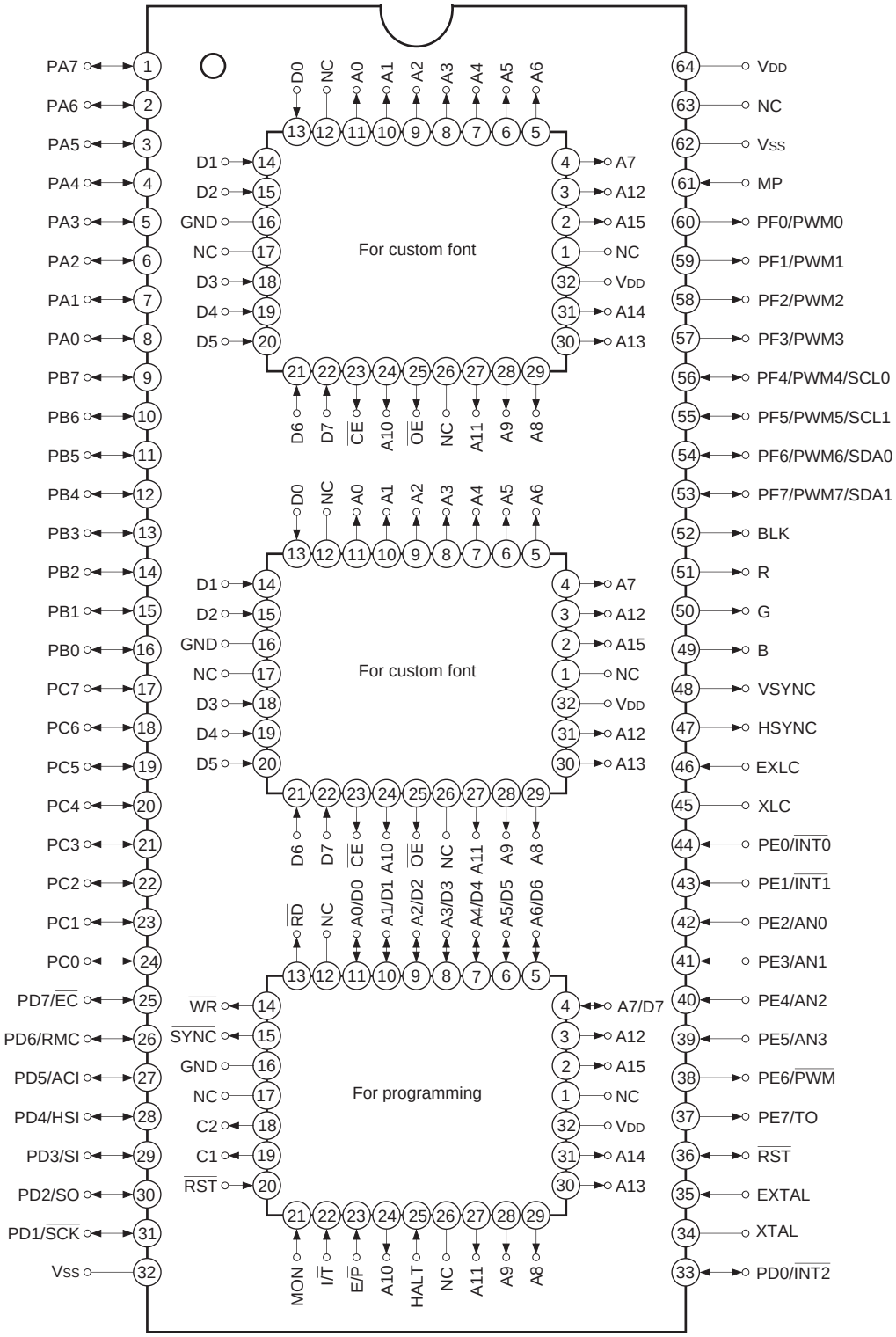
2. Vss (Pins 32 and 62) are always connected to GND.

3. MP (Pin 61) is always connected to GND.

CXP85290A

Pin Assignment: Evaluator Mode

(Top View) 64 pin PSDIP Package



Note) 1. NC (Pin 63) is always connected to V_{DD}.

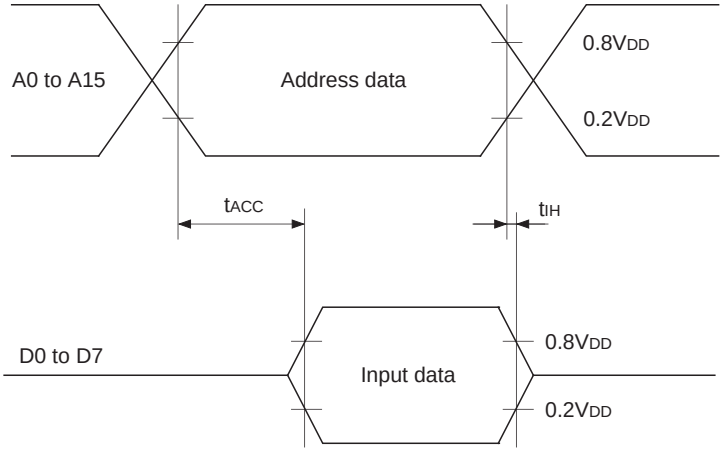
2. Vss (Pins 32 and 62) are always connected to GND.

3. MP (Pin 61) is always connected to GND.

EPROM Read Timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		250	ns
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

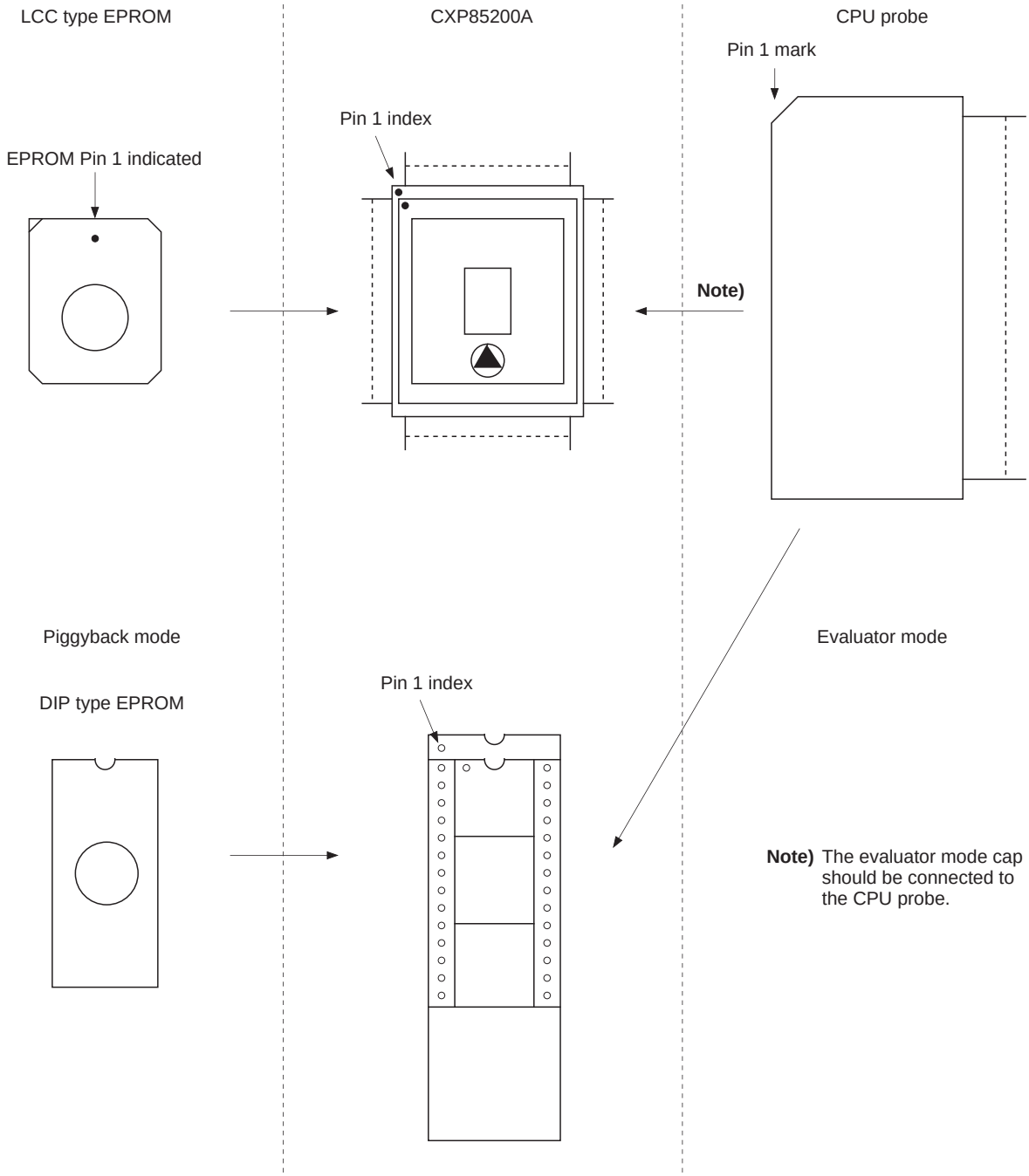


Product List

Optional item	Product								
	Mask						Piggyback/evaluator		
	CXP85112B	CXP85116B	CXP85220A	CXP85224A	CXP85228A	CXP85232A	CXP85200A-U01S CXP85200A-U01Q	CXP85200A-U03S CXP85200A-U03Q	CXP85290A-U01S
Package	64 pin plastic SDIP/QFP						64 pin ceramic PSDIP/PQFP		64 pin ceramic PSDIP
ROM capacity	12K bytes	16K bytes	20K bytes	24K bytes	28K bytes	32K bytes	EPROM 32K bytes		
RAM capacity	352 bytes		448 bytes				448 bytes		
Reset pin pull-up resistor	Existent/non existent						Existent		
Power-on reset circuit	Existent/non existent						Existent		
Font data	User data						Fixed	Fixed (European Font)	EPROM 4K bytes

CXP85200A

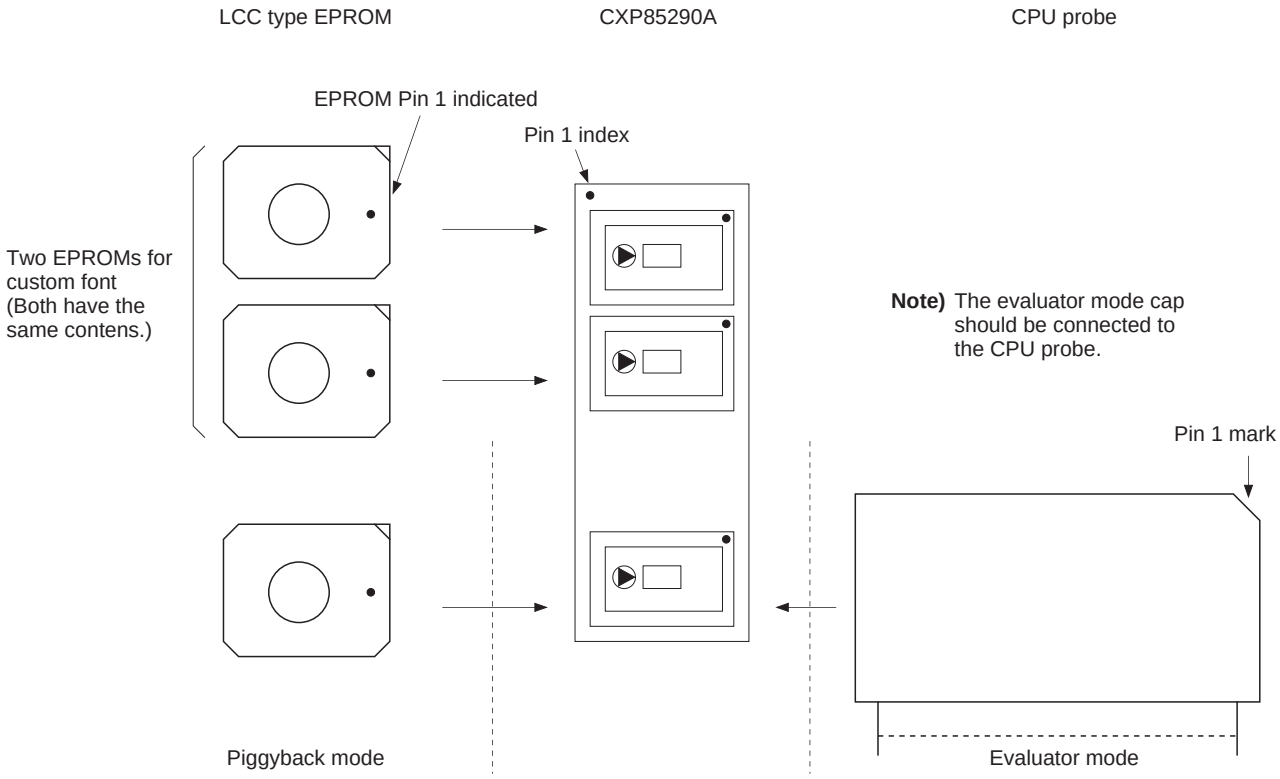
Piggyback mode/evaluator mode switching process is as follows.



Note) The evaluator mode cap should be connected to the CPU probe.

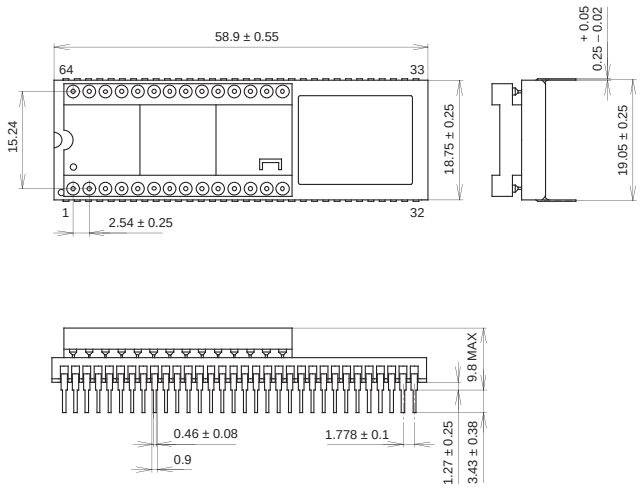
CXP85290A

Piggyback mode/evaluator mode switching process is as follows.



Package Outline Unit: mm

64PIN PSDIP (CERAMIC) 750mil

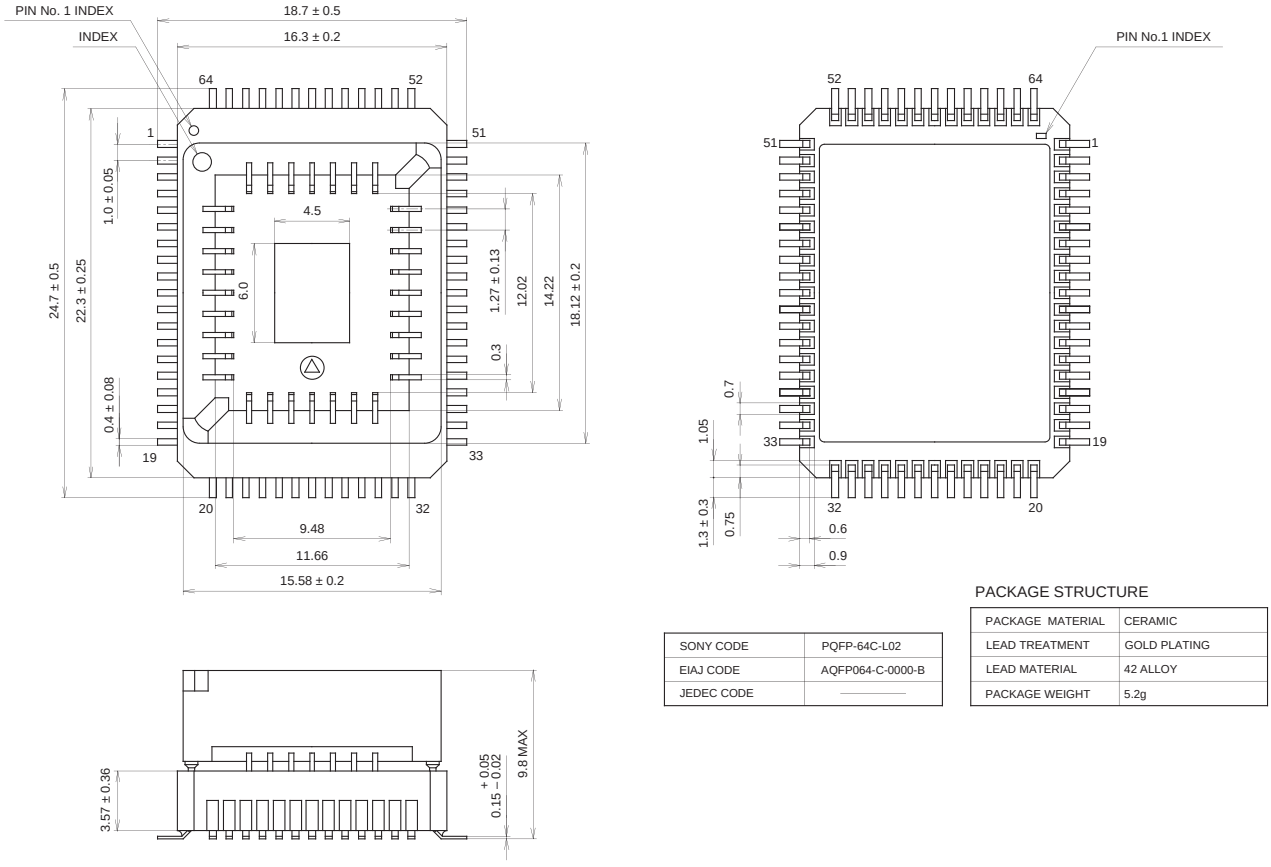


SONY CODE	PSDIP-64C-01
EIAJ CODE	ADIP064-C-0750-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	16.0g

64PIN PQFP (CERAMIC)

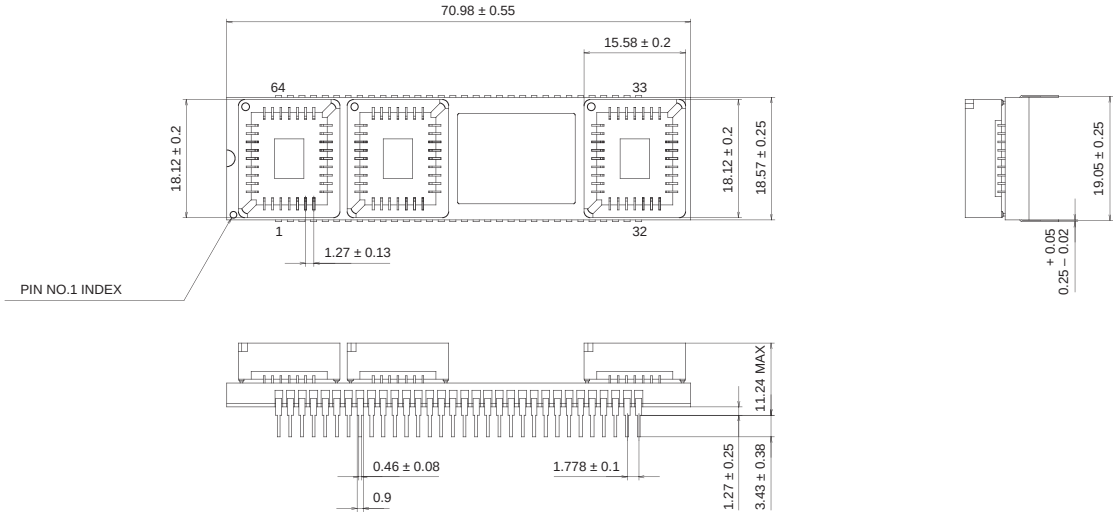


SONY CODE	PQFP-64C-L02
EIAJ CODE	AQFP064-C-0000-B
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.2g

64PIN PSDIP (CERAMIC)



PACKAGE STRUCTURE

SONY CODE	PSDIP-64C-02
EIAJ CODE	ADIP064-C-0750-B
JEDEC CODE	

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	22.8g