KL5KUSB121

USB to 10/100 Ethernet Controller

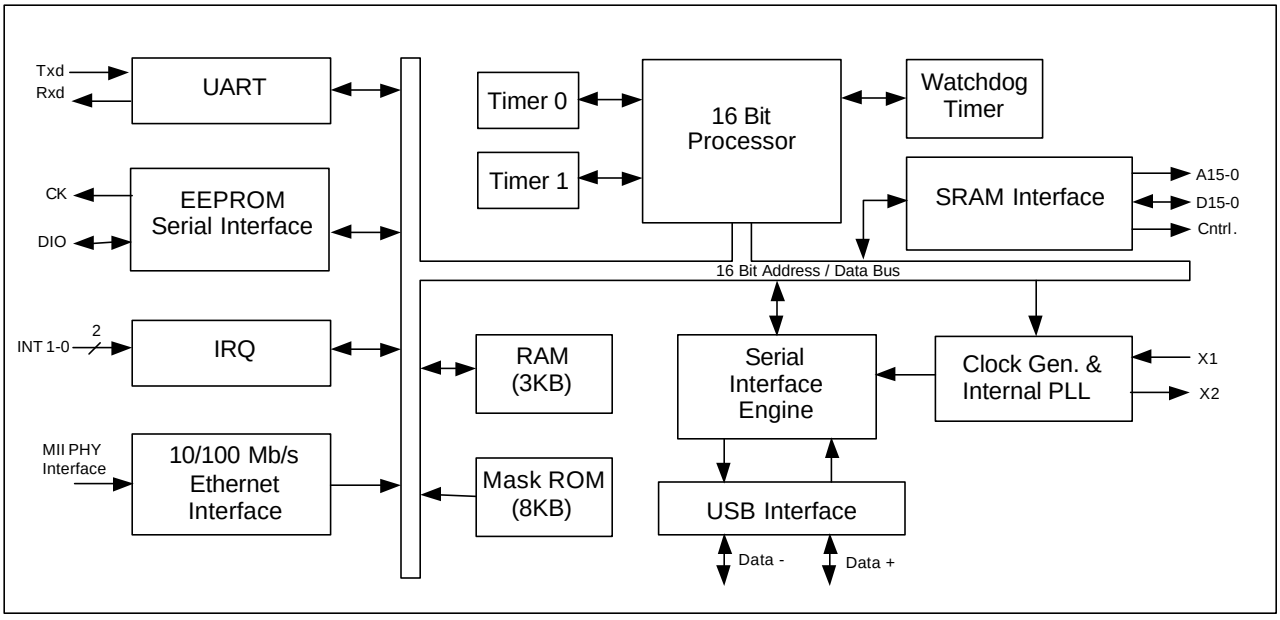
General Description

The Kawasaki KL5KUSB121 Controller is a unique single chip solution to interface peripheral devices to the Universal Serial Bus (USB) and Ethernet. The KL5KUSB121 has been specifically designed to provide a simple solution to communicate with Ethernet applications as well as other USB peripheral devices. This has been accomplished by its highly integrated functionality. The USB controller consists of a central 16-bit processor, mask ROM, RAM buffer, clock generator, Ethernet interface, UART, IRQ, Watchdog Timer, Serial interface, External Memory Interface and SPORT Interface. The SIE (Serial Interface Engine) is fully compatible with the USB specification. Our powerful internal processor enables Remote NDIS (Network Drive) which gives compatibility with next generation operating systems and faster data transfer. This USB to Ethernet controller is ideal for LAN (Local Area Network), HAN (Home Area Network), Cable Modem, Set Top Boxes, or Mobile Networking applications.

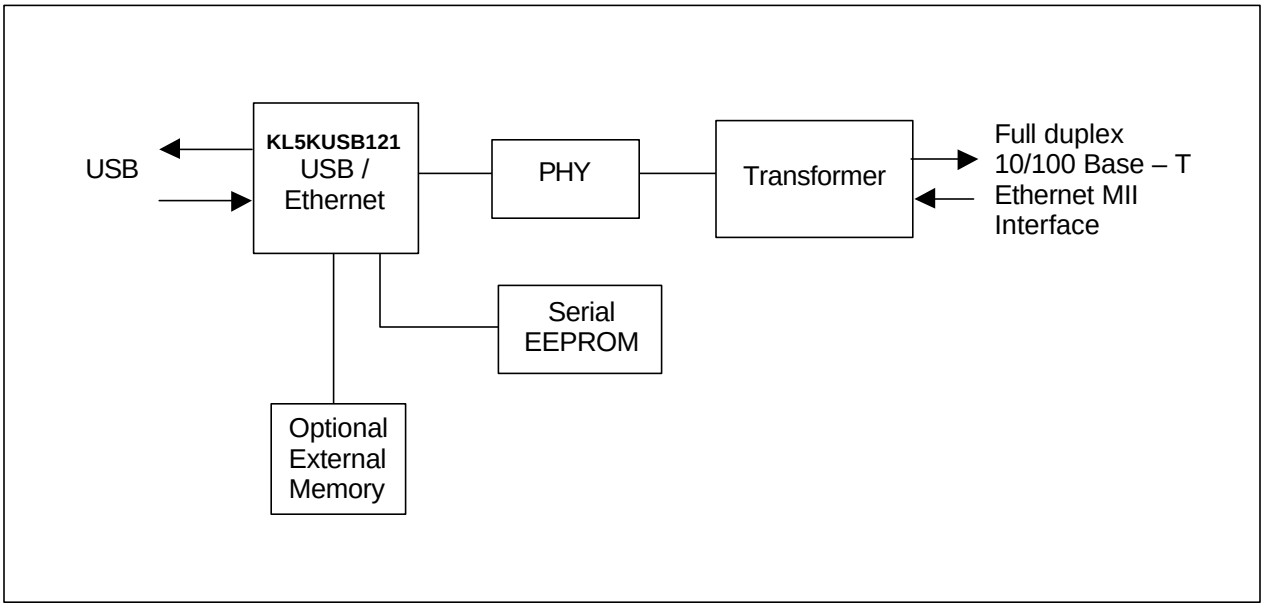
Features

- Advanced 16 Bit processor for USB transaction processing and control data processing
- 10/100Base-T compatibility
- USB interface ver. 1.0/1.1 compliant
- Transceivers and SIE (Serial Interface Engine)
- Internal Clock Generation - Utilizes low cost external 12MHz crystal circuitry
- MII Physical Layer interface
- 1.5K x 16 Internal RAM buffer
- Remote NDIS for faster data transfer.
- Fully IEEE 802.3 compliant 10 Mbit/sec Ethernet MAC Layer. Interfaces serially of an external ENDEC PHY.
- UART
- External memory interface
- LQFP package
- Serial Interface for external EEPROM

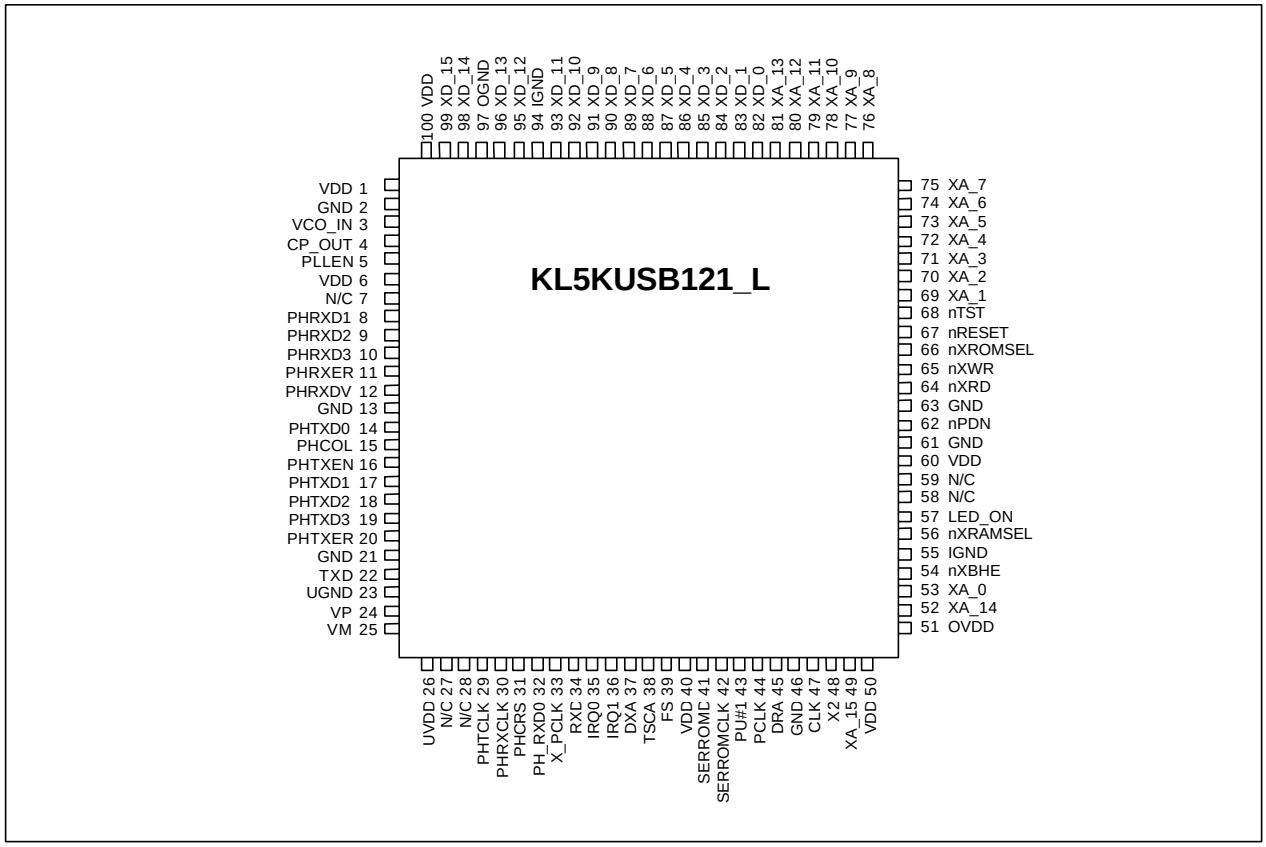
Block Diagram



KL5KUSB121 Application Block Diagram



Pin Diagram 100LQFP



Pin Description

Pin # LQFP	I/O	Pin Name	Description
1	IN	VDD	VDD
2	GND	GND	PLL GND
3	IN	VCO_IN	PLL VCO IN
4	OUT	CP_OUT	PLL VCO OUT
5	IN	PLLEN	PLL Enable
6	IN	VDD	PLL VDD
7	N/C	N/C	*Open connection*
8	IN	PHRXD1	PHY Receive Data 1
9	IN	PHRXD2	PHY Receive Data 2
10	IN	PHRXD3	PHY Receive Data 3
11	IN	PHRXER	Receive Data Error from PHY
12	IN	PHRXDV	Receive Data Valid from PHY
13	IN	GND	Ground
14	OUT	PHTXD0	Transmit data to PHY
15	IN	PHCOL	Collision input from PHY
16	OUT	PHTXEN	Transmit Enable to PHY
17	OUT	PHTXD1	Transmit Data 1 to PHY
18	OUT	PHTXD2	Transmit Data 2 to PHY
19	OUT	PHTXD3	Transmit Data 3 to PHY
20	OUT	PHTXER	Transmit Error to PHY
21	IN	GND	Ground
22	IN/OUT	TXD	UART TXD
23	IN	UGND	USB GND
24	IN/OUT	VP	USB + Pin
25	IN/OUT	VM	USB – Pin
26	IN	UVDD	USB VDD
27	NC	NC	*Open connection*
28	NC	NC	*Open connection*
29	IN	PHTXCLK	PHY Transmit Clock
30	IN	PHRXCLK	PHY Receive Clock
31	IN	PHCRS	PHY Carrier Sense
32	IN	PH_RXD0	PHY Serial Receive Data
33	IN/OUT	X_PCLK	External PCLK
34	IN/OUT	RXD	UART RXD
35	IN	IRQ0	Edge sens. Interrupt
36	IN	IRQ1	Edge sens. Interrupt
37	OUT	DXA	Sport Mode or GPIO7
38	IN	TSCA	Sport Mode or GPIO8
39	IN/OUT	FS	Sport Mode or GPIO9
40	IN	VDD	*Open connection*
41	IN/OUT	SERROMD	Serial ROM Data
42	OUT	SERROMCLK	Serial ROM Clock
43	IN/OUT	PU#1	Pull up to USB + Pin for High Speed
44	IN	PCLK	Sport Mode or GPIO5
45	IN	DRA	Sport Mode or GPIO6
46	IN	OGND	GND
47	IN	CLK	12MHz Clock/Crystal Input

Pin # LQFP	I/O	Pin Name	Description
48	OUT	X2	12MHz Crystal Output
49	OUT	XA_15	External Address Pin
50	IN	VDD	VDD
51	IN	OVDD	VDD
52	OUT	XA_14	External Address Pin
53	OUT	XA_0	External Address Pin
54	OUT	nXBHE	SRAM Byte High Enable
55	IN	IGND	GND
56	OUT	nXRAMSEL	SRAM Byte Low Enable
57	OUT	LED_ON	Turns on 3.3V to TX LED
58	N/C	N/C	*Open connection*
59	N/C	N/C	*Open connection*
60	IN	VDD	VDD
61	IN	GND	Ground
62	IN/OUT	nPDN	Active low Powerdown mode signal to Phy
63	IN	GND	GND
64	OUT	nXRD	External Memory Read (Active low)
65	OUT	nXWR	External Memory Write (Active low)
66	N/C	nXROMSEL	External ROM CS, active LO
67	IN	nRESET	Reset Pin
68	IN	nTST	Test Pin, *Disconnect for Normal Operation*
69	OUT	XA_1	External Address Pins
70	OUT	XA_2	External Address Pins
71	OUT	XA_3	External Address Pins
72	OUT	XA_4	External Address Pins
73	OUT	XA_5	External Address Pins
74	OUT	XA_6	External Address Pins
75	OUT	XA_7	External Address Pins
76	OUT	XA_8	External Address Pins
77	OUT	XA_9	External Address Pins
78	OUT	XA_10	External Address Pins
79	OUT	XA_11	External Address Pins
80	OUT	XA_12	External Address Pins
81	OUT	XA_13	External Address Pins
82	IN/OUT	XD_0	External Data Pins
83	IN/OUT	XD_1	External Data Pins
84	IN/OUT	XD_2	External Data Pins
85	IN/OUT	XD_3	External Data Pins
86	IN/OUT	XD_4	External Data Pins
87	IN/OUT	XD_5	External Data Pins
88	IN/OUT	XD_6	External Data Pins
89	IN/OUT	XD_7	External Data Pins
90	IN/OUT	XD_8	External Data Pins
91	IN/OUT	XD_9	External Data Pins
92	IN/OUT	XD_10	External Data Pins
93	IN/OUT	XD_11	External Data Pins
94	IN	IGND	GND
95	IN/OUT	XD_12	External Data Pins
96	IN/OUT	XD_13	External Data Pins
97	IN	OGND	GND

Pin # LQFP	I/O	Pin Name	Description
98	IN/OUT	XD_14	External Data Pins
99	IN/OUT	XD_15	External Data Pins
100	IN	VDD	VDD

Function Description

16 Bit Processor

The integrated 16 bit processor serves as a micro controller for USB peripherals. The processor can execute approximately five million instructions per second. With this processing power it allows the design of intelligent peripherals that can process data prior to passing it on to the host PC, thus improving overall performance of the system. The masked ROM (4K X 16) in the KL5KUSB121 or external memory contains a specialized instruction set that has been designed for highly efficient coding of processing algorithms and USB transaction processing.

The 16-bit processor is designed for efficient data execution by having direct access to the RAM Buffer, external memory, I/O interfaces, and all the control and status registers. The divide/multiply feature expands the capability of USB peripherals.

The processor supports prioritized vectored hardware interrupts. In addition, as many as 240 software interrupt vectors are available.

The processor provides six addressing modes, supporting memory-to-memory, memory-to-register, register-to-register, immediate-to-register or immediate-to-memory operations. Register, direct, immediate, indirect, and indirect indexed addressing modes are supported. In addition, there is an auto-increment mode in which a register, used as an address pointer is automatically incremented after each use, making repetitive operations more efficient both from a programming and a performance standpoint.

The processor features a full set of program control, logical, and integer arithmetic instructions. All instructions are sixteen bits wide, although some instructions require operands, which may occupy another one or two words. Several special " short immediate" instructions are available, so that certain frequently used operations with small constant operand will fit into a 16-bit instruction.

RAM Buffer

The USB controller contains a 3K byte (1.5K X 16) internal buffer memory. The memory is used to buffer data and USB packets and accessed by the 16 Bit processor and the SIE. USB transactions are automatically routed to the memory buffer. The 16-bit processor has the ability to set up pointers and block sizes in buffer memory for USB transactions. Data is read from the interface and is processed and packetized by the 16-bit I/O processor.

PLL Clock Generator

The PLL circuitry is provided to generate the internal 48MHz clock requirements. This circuitry is designed to allow use of a low cost 12 MHz external crystal which is connected to the USB3 pins X1 and X2. If an external 12 MHz clock is available in the application, it may be used in lieu of the crystal circuit and connected directly to the X1 input pin.

USB Interface

The USB controller meets the Universal Serial Bus (USB) specification ver 1.0. The transceiver is capable of transmitting and receiving serial data at the USB's full speed, 12 Mbits/sec data rate. The driver portion of the transceiver is differential, while the receive section is comprised of a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the SIE logic. Externally, the transceiver connects to the physical layer of the USB.

10Mb, 100Mb/sec Ethernet Interface

The KL5KUSB121 Controller has a built in the Ethernet MAC (Media Access Controller) which is fully compliant with the IEEE 802.3 Ethernet standard. The KL5KUSB121 connects externally to a 10 Base -T and/or 100 Base-T ENDEC PHY. The KL5KUSB121 Controller 16-bit processor has direct access to the registers of the MAC.

UART Interface

Supports a transfer rate of 900 to 115.2K baud.

Serial EEPROM Support

The USB Controller serial interface is used to provide access to external EEPROM's. The interface can support a variety of serial EEPROM formats.

SRAM Interface

An address port and 16-bit data port has been provided to interface to an external SRAM.

DC CHARACTERISTICS

U2E is implemented with Kawasaki's 0.5um CMOS CBA and Embedded Memory KZ300EM Technology. The followings are the description of chip electric characteristics.

1. Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	Vdd	–0.3 ~ 4.0	V
Input Voltage	Vin	–0.3 ~ 7.3	V
DC Output Current	Iout	±15	mA
Storage Temperature	Tstg	–55 ~ 125	°C

2. Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating supply voltage	Vdd	3.0	–	3.6	V
Operating ambient temperature	Ta	0	–	70	°C

3. I/O Electrical DC Characteristics (Over Recommended Range)

Table 3.1 DC Characteristics (over recommended range)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input low voltage	VIL	–	–	0.8	V	
Input high voltage	VIH	2.0	–	–	V	
Input low current	IIL	–10	–	10	uA	VIN = Gnd
Input high current	IIH	–10	–	10	uA	VIN = Vdd
Output low voltage	VOL	–	–	0.4	V	IOL = 4mA
Output high voltage	VOH	2.4	–	–	V	IOH = –4mA
3-state leak current	IOZ	–10	–	10	uA	VOH = Gnd or VOL = Vdd
Active pull-up current	IPU	–25	–66	–160	uA	VIN = Gnd or VOH = Gnd
Standby current	IDDS	–	80	100	uA	VIN = Gnd or Vdd No inputs are cycling. Outputs open.
Suspend current	ISUSP	–	350	450	uA	Same conditions as IDDS except for CLKI input buffer 48MHz toggling.
dynamic operating current	IDDOP1 (in busy)	–	80	100	mA	Outputs open. Vdd = Max. FCLKI = FMAX (48MHz)
	IDDOP2 (in idle)	–	40	50	mA	
Input capacitance	CIN	–	–	15	pF	Fpin=1MHz, VIN = Gnd. Vin = 100 mVrms
Output capacitance	COUT	–	–	15	pF	

AC CHARACTERISTICS

U2E chip has 4 types of interfaces – USB port, Ethernet PHY port, SRAM port and Serial EEPROM port. AC timing of these interfaces are described below along with appropriate timing charts. Chip also requires the AC timing of system clock input CLKI and system reset RESETN.

1. CLKI and RESETN Signal

Figure 1.1 CLKI and RESETN AC Timing

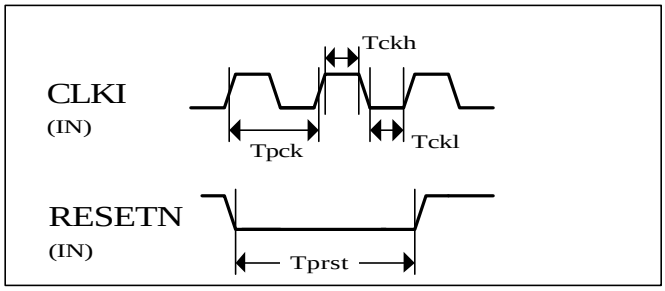


Table 1.1 CLKI AC Characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Tpck	CLKI one cycle time	–	20.83	–	ns	1
Fck	CLKI frequency	–	48	–	MHz	1
Tckh	CLKI high time	10	–	–	ns	1
Tckl	CLKI low time	10	–	–	ns	1

Note: 1) The clock is used as an USB sampling clock and to generate the internal 32MHz clock pulse.

Table 1.2 RESETN AC characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Tprst	RESETN low pulse width	10	–	–	Tpck	2

Note: 2) RESETN is an asynchronous, low assert, reset signal. Minimum assertion is 10 times of Tpck (210 ns).

2. USB Interface

The USB signals – VP and VM are the pair signals of the differential output driver and receiver. The USB to Ethernet operates under USB Full speed (12Mb/s).
USB signals are fully compatible with USB spec rev 1.1.

3. PHY Interface

USB to Ethernet exchanges the serial bit data and messages to the external PHY chip.

3.1 U2E to PHY transmit

Figure 3.1.1 USB to Ethernet to PHY Transmit AC Timing

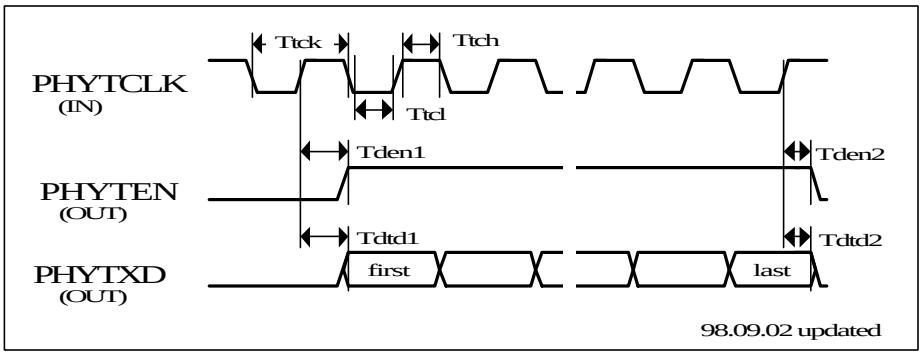


Table 3.1.1 PHY Transmit AC Characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Ttck	PHYTCLK period	–	100	–	ns	1
Ftck	PHYTCLK frequency	–	10	–	MHz	1
Ttch	PHYTCLK high width	–	50	–	ns	–
Ttcl	PHYTCLK low width	–	50	–	ns	–
Tden1	PHYTEN assert delay from PHYTCLK rise	–	–	30	ns	2
Tden2	PHYTEN negate delay from PHYTCLK fall	0	–	–	ns	2
Tdtd1	PHYTXD valid delay from PHYTCLK rise	–	–	28	ns	2
Tdtd2	PHYTEN valid delay from PHYTCLK fall	0	–	–	ns	2

Note: 1) PHY generates the 10MHz clock.
2) 30pF capacitor external load is assumed.

Figure 3.1.2 PHY SQE function AC Timing at Transmit

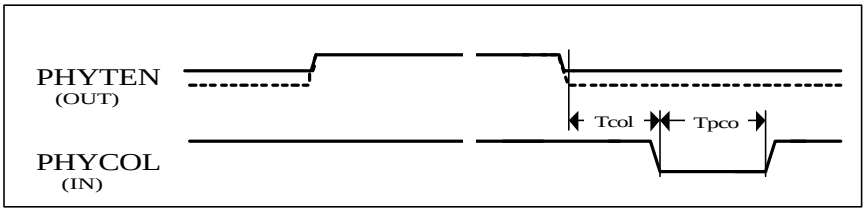


Table 3.1.2 PHY SQE Transmit AC Characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Tcol	PHYCOL assert delay from PHYTEN fall	–	–	1.6	us	–
Tpco	PHYCOL low width	0.5	–	–	us	–

3.2 U2E to PHY receive

Figure 3.2.1 U2E from PHY Receive AC Timing

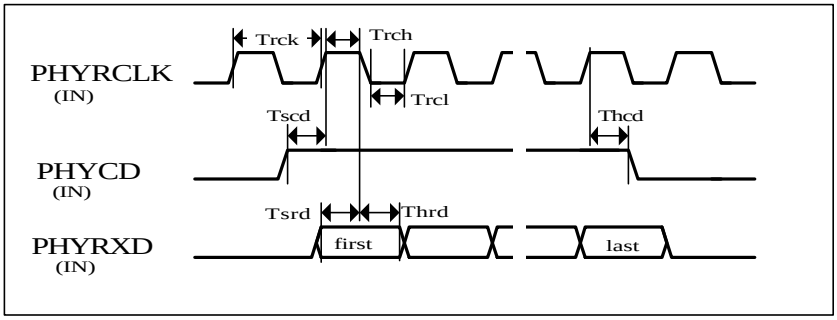


Table 3.2.1 Receive from PHY AC Characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Trck	PHYRCLK period	–	100	–	ns	1
Frck	PHYRCLK frequency	–	10	–	MHz	1
Trch	PHYRCLK high width	–	50	–	ns	–
Trcl	PHYRCLK low width	–	50	–	ns	–
Tscd	PHYCD setup time to PHYRCLK rise	20	–	–	ns	–
Thcd	PHYCD hold time from PHYTCLK rise	10	–	–	ns	–
Tsrd	PHYRXD setup time to PHYRCLK fall	20	–	–	ns	–
Thrd	PHYRXD hold time from PHYRCLK fall	10	–	–	ns	–

Note: 1) PHY generates the 10MHz clock.

4. SRAM Interface

4.1 SRAM Read Access

Figure 4.1.1 SRAM Read AC Timing

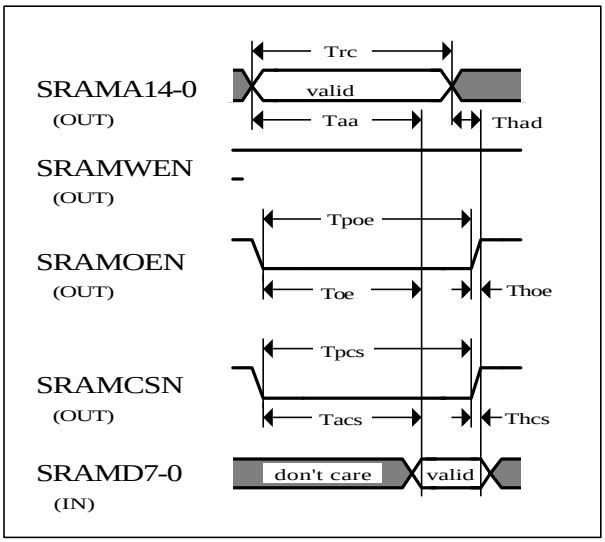


Table 4.1.1 SRAM Read AC Characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Trc	SRAM read cycle	31.25	–	–	ns	1,2
Frc	SRAM read frequency	–	–	32	MHz	1,2
Taa	SRAMA valid to SRAMD delay (address access)	–	–	17	ns	2
Thad	SRAMD hold time from SRAMD invalid	2	–	–	ns	2
Tpoe	SRAMOEN low width	31.25	–	–	ns	2
Toe	SRAMOEN assert to SRAMD delay	–	–	10	ns	2
Thoe	SRAMD hold time from SRAMOEN rise	0	–	–	ns	2
Tpcs	SRAMCSN low width	31.25	–	–	ns	1,2
Tacs	SRAMCSN assert to SRAMD delay	–	–	17	ns	2
Thcs	SRAMD hold time from SRAMCSN rise	0	–	–	ns	2

Note: 1) Same as the USB to Ethernet internal clock cycle time 1T (31.25 ns).
2) Outputs are assumed to have 30pF external capacitive load.

4.2 SRAM Write Access

Figure 4.2.1 SRAM Write AC Timing

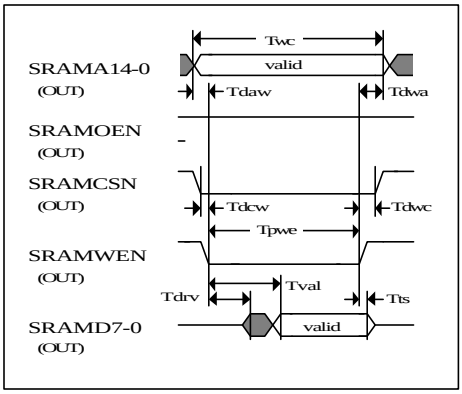


Table 4.2.1 SRAM Write AC Characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Twc	SRAM write cycle	31.25	–	–	ns	1,2
Fwc	SRAM write frequency	–	–	32	MHz	1,2
Tdaw	SRAMWEN assert delay from SRAMA valid	0	–	–	ns	2
Tdwa	SRAMA invalid delay from SRAMWEN negate	0	–	–	ns	2
Tdcw	SRAMWEN assert delay from SRAMCSN assert	0	–	–	ns	2
Tdwc	SRAMCSN negate delay from SRAMWEN negate	0	–	–	ns	2
Tpwe	SRAMWEN low width	25	–	–	ns	2
Tdrv	SRAMD drive delay from SRAMWEN assert	0	–	–	ns	2
Tval	SRAMD valid from SRAMWEN assert	–	–	15	ns	2
Tts	SRAMD hold time from SRAMWEN rise	0	–	–	ns	2

Note: 1) Same as the USB to Ethernet internal clock cycle time 1T (31.25 ns).
2) Outputs are assumed to have 30pF external capacitive load.

5. Serial EEPROM interface

The USB to Ethernet device communicates with the Serial EEPROM (SEP) through I²C™ bus.

5.1 Serial EEPROM Access Start

Figure 5.1.1 SEP Access Start AC Timing

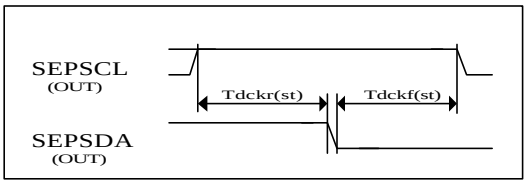


Table 5.1.1 SEP Access Start AC Characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Tdckr(st)	SEPSDA fall delay from SEPSCL rise	4.7	–	–	us	1
Tdckf(st)	SEPSCL fall delay from SEPSDA fall	4.0	–	–	us	1

Note: 1) 30pF external capacitive load is assumed.

5.2 Serial EEPROM Access Stop

Figure 5.2.1 SEP Access Stop AC Timing

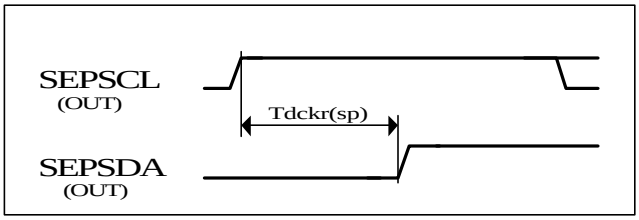


Table 5.2.1 SEP access stop AC characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Tdckr(sp)	SEPSDA rise delay from SEPSCL rise	4.0	–	–	us	1

Note: 1) 30pF external capacitive load is assumed.

5.3 Serial EEPROM Read Access

Figure 5.3.1 SEP Read Access AC Timing

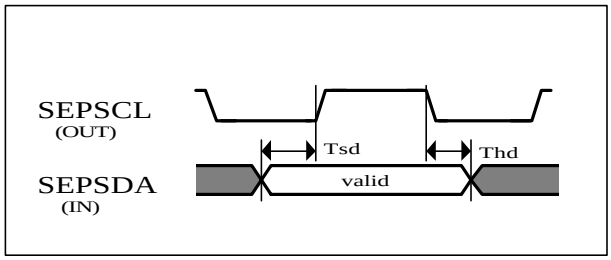


Table 5.3.1 SEP read access AC characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Tsd	SEPSDA setup time from SEPSCL rise	20	–	–	ns	1
Thd	SEPSDA hold time from SEPSCL fall	0	–	–	ns	1

Note: 1) 30pF external capacitive load is assumed.

5.4 Serial EEPROM Write Access

Figure 5.4.1 SEP Write Access AC Timing

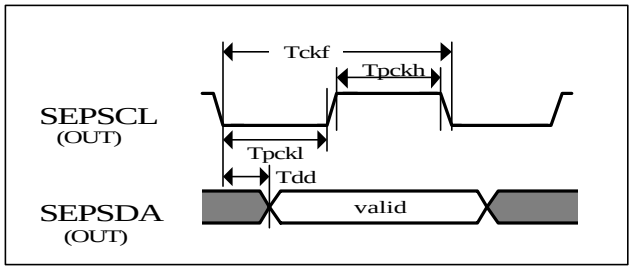


Table 5.4.1 SEP Write Access AC Characteristics (over recommended range)

Symbol	Parameter	Min	Typ	Max	Unit	Note
Tsck	SEPSCL clock period	10	–	–	us	1
Fsck	SEPSCL frequency	–	–	100	kHz	1
Tpckl	SEPSCL low width	4.7	–	–	us	1
Tpckh	SEPSCL high width	4.0	–	–	us	1
Tdd	SEPSDA valid delay from SEPSCL fall	2	–	20	ns	1

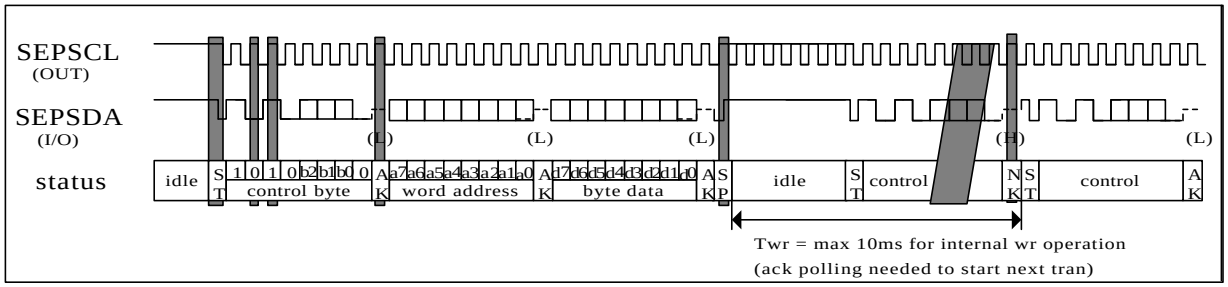
Note: 1) 30pF external capacitive load is assumed.

6. Serial EEPROM Access Timing

Serial EEPROM Byte Write, Page Write, Current Address Read, Random Read and Sequential Read Timings are shown below. Please refer to Serial EEPROM datasheet ([12] 3-b) for more detail.

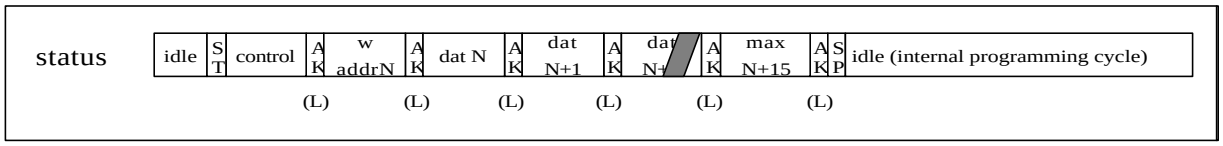
6.1 Serial EEPROM Byte Write

Figure 6.1.1 SEP Byte Write Timings



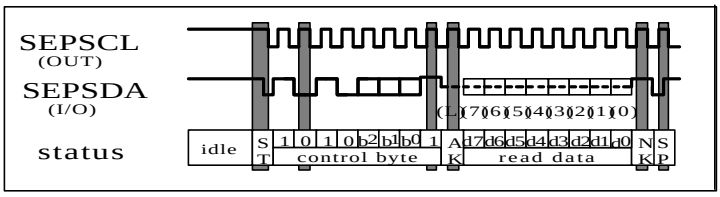
6.2 Serial EEPROM Page Write (up to 16 bytes)

Figure 6.2.1 SEP Page Write Timings



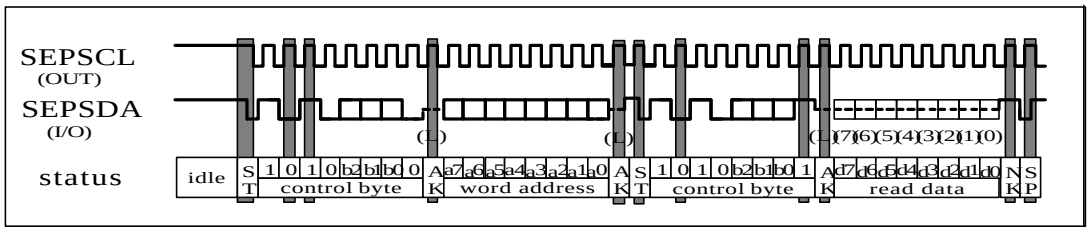
6.3 Serial EEPROM Byte Read from current address

Figure 6.3.1 SEP Byte Read Timings



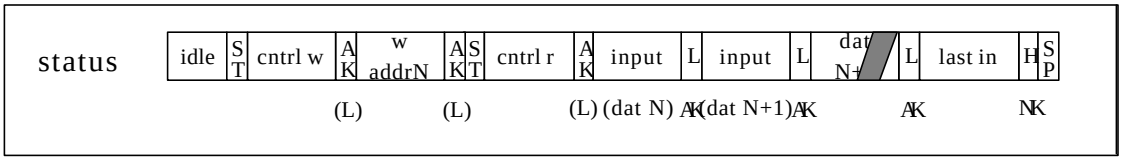
6.4 Serial EEPROM Byte Random Read

Figure 6.4.1 SEP Byte Random Read Timings



6.5 Serial EEPROM Sequential Read (up to final address)

Figure 6.5.1 SEP Sequential Read Timings



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