May 11, 2009

National Semiconductor

LM57

Resistor-Programmable Temperature Switch and Analog Temperature Sensor

General Description

The LM57 is a precision, dual-output, temperature switch with integrated analog temperature sensor. The trip temperature (T_{TRIP}) is programmable by using two external 1% resistors. Using extremely small packaged resistors (0.5 mm x 1 mm), the LM57 can be programmed to any of 256 trip temperatures while consuming very little board space. The V_{TEMP} output delivers an analog output voltage which is inversely proportional to the measured temperature.

Built-in temperature hysteresis (T_{HYST}) keeps the output stable in an environment of thermal oscillation. The digital temperature switch outputs will go active when the die temperature exceeds T_{TRIP} and will release when the temperature falls below a temperature equal to T_{TRIP} minus T_{HYST}. One of the digital outputs, T_{OVER}, is active-high with a push-pull structure. The other digital output, $\overline{T_{OVER}}$, is active-low with an open-drain structure.

Driving the TRIP-TEST input high will make the digital outputs active. A processor can read the logic level of the temperature switch outputs, confirming that they changed to their active state. This allows for in-situ verification that the comparator and output circuitry are functional after system assembly. When the TRIP-TEST pin is high, the trip-level reference voltage appears at the Vtemp pin. The system could then use this voltage to calibrate the sensor for even tighter accuracy. Tying T_{OVER} to TRIP-TEST will latch the output after it trips. It can be cleared by forcing TRIP-TEST low or powering off the LM57.

As it draws only 28µA max from its supply, it has very low self-heating, about 0.02°C in still air.

Applications

- Cell phones
- Wireless transceivers
- Digital cameras
- Personal digital assistants (PDA's)
- Battery management
- Automotive
- Disk drives
- Games
- Appliances

Features

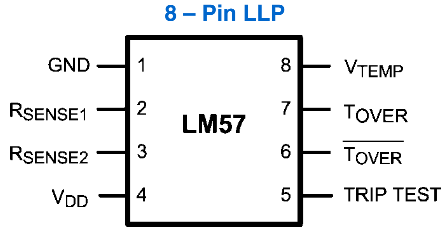
- Trip temperature set by external resistors
- External resistor tolerance contributes zero error
- Push-pull and open-drain temperature switch outputs
- Wide operating temperature and trip-temperature range of –50°C to 150°C
- Very linear analog V_{TEMP} temperature sensor output
- Analog and digital outputs are short-circuit protected
- TRIP-TEST pin allows in-system testing
- Latching function for the digital outputs
- Very small 2.5 mm by 2.5 mm 8-Pin LLP package

Key Specifications

Supply voltage	2.4V to 5.5V
Supply current	24 µA (typ)
Temperature switch accuracy	±1.5°C
Analog (V_{TEMP}) Accuracy	±0.7°C
Operating temperature	–50°C to 150°C
Hysteresis magnitude	5°C, 10°C

Connection Diagram

8 – Pin LLP



Top View

Typical Application

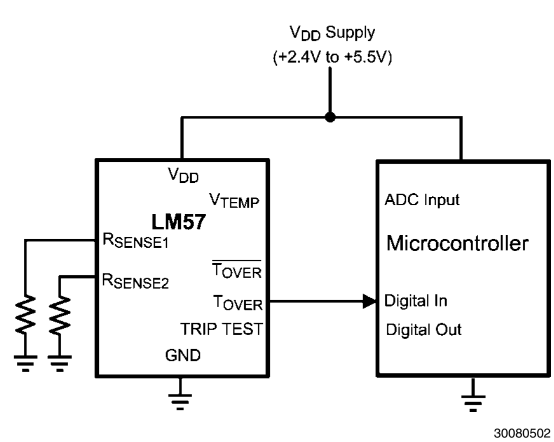
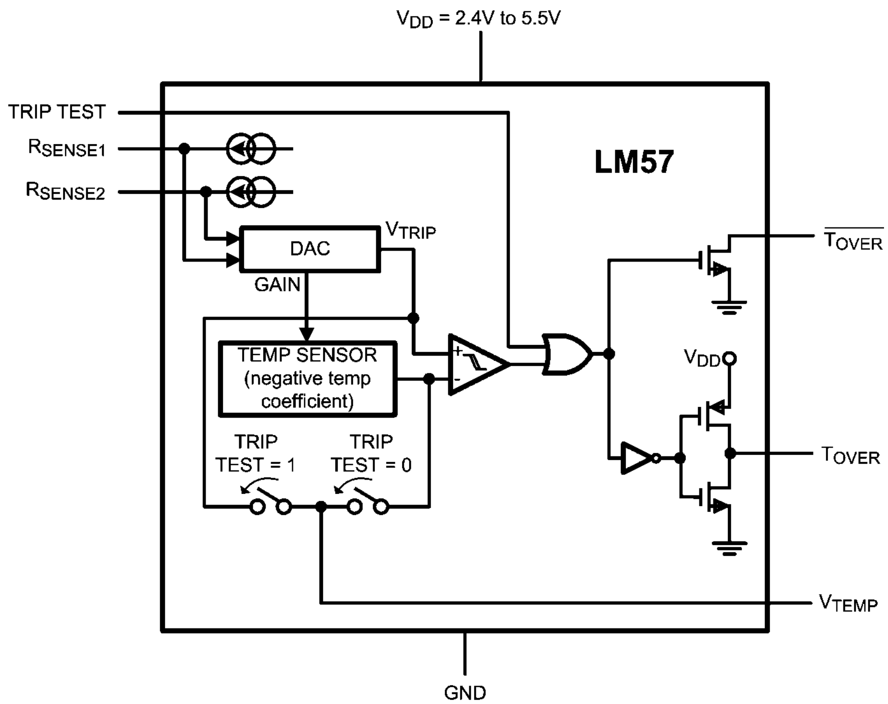


FIGURE 1. Over-Temperature Output to Microcontroller Digital Input

Block Diagram



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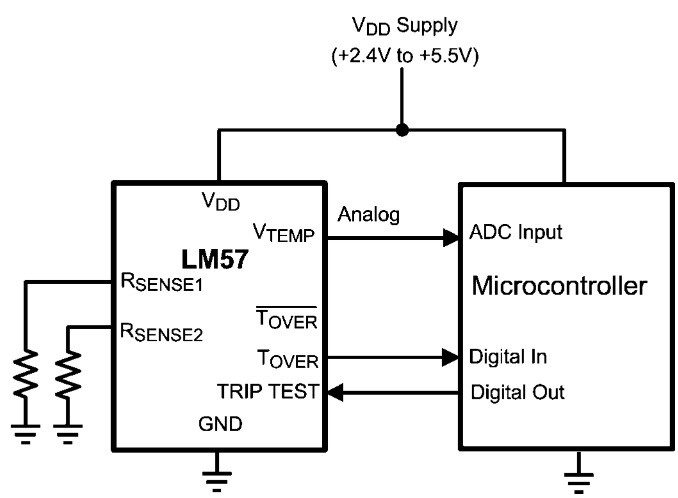
Typical Application



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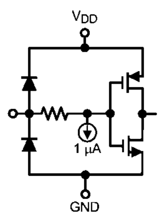
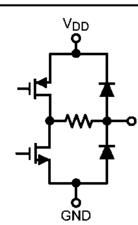
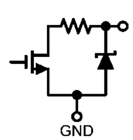
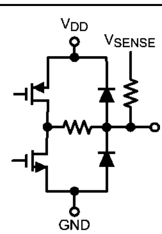
Pin Descriptions

Pin No.	Name	Type	Equivalent Circuit	Description
1	GND	Ground		Power Supply Ground
2	R_{SENSE1}			Trip-Point Resistor Sense. One of two sense pins which selects the temperature at which T_{OVER} and $\overline{T_{OVER}}$ will go active.
3	R_{SENSE2}			Trip-Point Resistor Sense. One of two sense pins which selects the temperature at which T_{OVER} and $\overline{T_{OVER}}$ will go active.
4	V_{DD}	Power		Supply Voltage
5	TRIP TEST	Digital Input		TRIP TEST pin. Active High input. If TRIP TEST = 0 (Default), then the V_{TEMP} output has the analog temperature sensor output voltage. If TRIP TEST = 1, then T_{OVER} and $\overline{T_{OVER}}$ outputs are asserted and V_{TEMP} = V_{TRIP}, the Temperature Trip Voltage. Tie this pin to ground if not used.
6	T_{OVER}	Digital Output		Over Temperature Switch output Active High, Push-Pull Asserted when the measured temperature exceeds the Trip Point Temperature or if TRIP TEST = 1 This pin may be left open if not used.
7	$\overline{T_{OVER}}$	Digital Output		Over Temperature Switch output Active Low, Open-drain (See Section 2.1 regarding required pull-up resistor.) Asserted when the measured temperature exceeds the Trip Point Temperature or if TRIP TEST = 1 This pin may be left open if not used.
8	V_{TEMP}	Analog Output		V_{TEMP} Analog Voltage Output If TRIP TEST = 0, then V_{TEMP} = V_{TS}, Temperature Sensor Output Voltage If TRIP TEST = 1, then V_{TEMP} = V_{TRIP}, Temperature Trip Voltage This pin may be left open if not used.

Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
8-Pin LLP	LM57BISD–5	57B5	1k Units Tape and Reel	SDA08B
	LM57BISDX–5	57B5	4.5k Units Tape and Reel	SDA08B
	LM57BISD–10	57B9	1k Units Tape and Reel	SDA08B
	LM57BISDX–10	57B9	4.5k Units Tape and Reel	SDA08B
	LM57CISD–5	57C5	1k Units Tape and Reel	SDA08B
	LM57CISDX–5	57C5	4.5k Units Tape and Reel	SDA08B
	LM57CISD–10	57C9	1k Units Tape and Reel	SDA08B
	LM57CISDX–10	57C9	4.5k Units Tape and Reel	SDA08B

Note:

The “-5” suffix is for 5°C hysteresis

The “-10” suffix is for 10°C hysteresis

Contact National Semiconductor Corporation for high temperature die (above 150°C).

Absolute Maximum Ratings (Note 1)

Supply Voltage	−0.3V to 6V
Voltage at $\overline{T_{OVER}}$	−0.3V to 6V
Voltage at T_{OVER} , V_{TEMP}, TRIP-TEST, R_{SENSE1}, and R_{SENSE2}	−0.3V to (V_{DD} + 0.3V)
Current at any pin	5 mA
Storage Temperature Range	−65°C to 150°C
ESD Susceptibility (Note 2)	
Human Body Model	5500V
Machine Model	450V
Charged Device Model	1250V

Soldering process must comply with National's Reflow Temperature Profile specifications. Refer to www.national.com/packaging. (Note 3)

Operating Ratings (Note 1)

Specified Temperature Range	−50°C to 150°C
Supply Voltage Range	+2.4 V to 5.5V

Accuracy Characteristics

There are four gains corresponding to each of the four Temperature Trip Point Ranges.

J2 is the sensor gain used for Temperature Trip Point −41°C to 51.8°C.

J3 is for Trip Points 52°C to 97°C.

J4 for 97°C to 119°C.

J5 for 119°C to 150°C.

Trip Point Accuracy

Parameter	Condition			LM57B	LM57C	Units (M ax)
Trip Point Accuracy (Includes 1% set-resistor tolerance) (Note 9)	J2	T_A = −41°C to 52°C	V_{DD} = 2.4V to 5.5V	±1.5	±2.3	°C
	J3	T_A = 52°C to 97°C	V_{DD} = 2.4V to 5.5V	±1.5	±2.3	°C
	J4	T_A = 97°C to 119°C	V_{DD} = 2.4V to 5.5V	±1.5	±2.3	°C
	J5	T_A = 119°C to 150°C	V_{DD} = 2.4V to 5.5V	±1.5	±2.3	°C

V_{TEMP} Analog Temperature Sensor Output Accuracy

These limits do not include DC load regulation. These stated accuracy limits are with reference to the values in the LM57 V_{TEMP} Temperature-to-Voltage Table.

Parameter	Condition			LM57B	LM57C	Units (Max)
V_{TEMP} Accuracy (These stated accuracy limits are with reference to the values in the LM57 Temperature-to-Voltage Table) (Note 9)	J2	T_A = −50°C to 150°C	V_{DD} = 2.4V to 5.5V	±0.95	±1.3	°C
	J3	T_A = −50°C to 150°C	V_{DD} = 2.4V to 5.5V	±0.8	±1.3	°C
	J4	T_A = 20°C to 50°C	V_{DD} = 2.4V to 5.5V	±0.7	±1.3	°C
		T_A = 0°C to 150°C	V_{DD} = 2.7V to 5.5V	±0.7	±1.3	
		T_A = −50°C to 0°C	V_{DD} = 3.1V to 5.5V	±0.8	±1.3	
	J5	T_A = 60°C to 150°C	V_{DD} = 2.4V to 5.5V	±0.7	±1.3	°C
		T_A = 20°C to 50°C	V_{DD} = 2.9V to 5.5V	±0.7	±1.3	
		T_A = 0°C to 150°C	V_{DD} = 3.2V to 5.5V	±0.7	±1.3	
		T_A = −50°C to 0°C	V_{DD} = 4.0V to 5.5V	±0.8	±1.3	

Electrical Characteristics

Unless otherwise noted, these specifications apply for V_{DD} = 2.4V to 5.5V. **Boldface** limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; All other limits apply to $T_A = T_J$ = +25°C , unless otherwise noted.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 4)	Max (Note 5)	Units
Temperature Sensor						
	V_{TEMP} Sensor Gain	J2 −41°C to 52°C		−5.166		mV/°C
		J3 52°C to 97°C		−7.752		
		J4 97°C to 119°C		−10.339		
		J5 119°C to 150°C		−12.924		
	Line Regulation DC: Supply-to-V_{TEMP} (Note 6)	V_{DD} = 2.4V to 5.5V, Gain = J4, Temp = 90°C		0.18		mV
				58		µV/V
				−84		dB
	Load Regulation: V_{TEMP} Output (Note 10)	Source ≤ 240 µA, (V_{DD} - V_{TEMP}) ≥ 200 mV			**−1**	mV
		Sink ≤ 300 µA, V_{TEMP} ≥ 360 mV			**1**	
		Source or Sink = 100 µA		1		Ω
	Load Capacitance: V_{TEMP} Output (Note 11)	No output series resistor required (See section 5.2)			**1100**	pF
I_S	Supply Current: Quiescent (Note 7)			24	**28**	µA
TRIP-TEST Input						
V_{IH}	Logic “1” Threshold Voltage		**V_{DD} - 0.5**			V
V_{IL}	Logic “0” Threshold Voltage				**0.5**	V
I_{IH}	Logic “1” Input Current			1.4	**3**	µA
I_{IL}	Logic “0” Input Leakage Current (Note 8)			0.001	**1**	µA
T_{OVER} (Push-Pull, Active-High) Output						
V_{OH}	Logic “1” Push-Pull Output Voltage	Source ≤ 600 µA	**V_{DD}- 0.2**			V
		Source ≤ 1.2 mA	**V_{DD} - 0.45**			
V_{OL}	Logic “0” Output Voltage	Sink ≤ 600 µA			**0.2**	V
		Sink ≤ 1.2 mA			**0.45**	
$\overline{T_{OVER}}$ (Open-Drain, Active-Low) Output						
V_{OL}	Logic “0” Output Voltage	Sink ≤ 600 µA			**0.2**	V
		Sink ≤1.2 mA			**0.45**	
I_{OH}	Logic “1” Output Leakage Current (Note 8)	Temperature = 30°C		0.001	**1**	µA
Hysteresis						
T_{HYST}	Hysteresis Temperature	5°C hysteresis option	**4.7**	5	**5.4**	°C
		10°C hysteresis option	**9.6**	10	**10.6**	°C
Timing						
t_{EN}	Time from power on to Digital Output Enabled (Note 11)			1.0	**2.9**	ms
t_{VTEMP}	Time from Power on to Analog Temperature (V_{TEMP}) valid (Note 11)			1.0	**2.9**	ms

Note 1: Absolute Maximum Ratings indicate limits beyond which damage may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: The Human Body Model (HBM) is a 100 pF capacitor charged to the specified voltage then discharged through a 1.5 kΩ resistor into each pin. The Machine Model (MM) is a 200 pF capacitor charged to the specified voltage then discharged directly into each pin. The Charged Device Model (CDM) is a specified circuit characterizing an ESD event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface.

Note 3: Reflow temperature profiles are different for lead-free and non-lead-free packages.

Note 4: Typicals are at $T_J = T_A = 25°C$ and represent most likely parametric norm.

Note 5: Limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 6: Line regulation (DC) is calculated by subtracting the output voltage at the highest supply voltage from the output voltage at the lowest supply voltage. The typical DC line regulation specification does not include the output voltage shift discussed in Section 5.3.

Note 7: Supply Current refers to the quiescent current of the LM57 only and does not include any load current

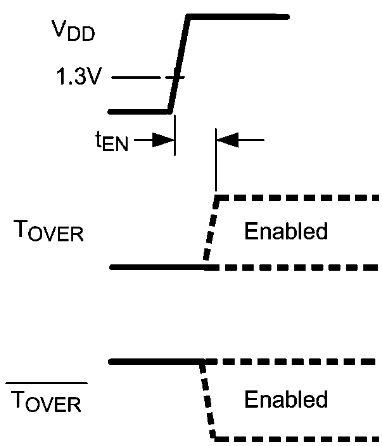
Note 8: This current is leakage current only and is therefore highest at high temperatures. Prototype test indicate that the leakage is well below 1 μA over the full temperature range. This 1 μA specification reflects the limitations of measuring leakage at room temperature. For this reason only, the leakage current is not guaranteed at a lower value.

Note 9: Accuracy is defined as the error between the measured and reference output voltages, tabulated in the Conversion Table at the specified conditions of supply gain setting, voltage, and temperature (expressed in °C). Accuracy limits include line regulation within the specified conditions. Accuracy limits do not include load regulation; they assume no DC load.

Note 10: Source currents are flowing out of the LM57. Sink currents are flowing into the LM57. Load Regulation is calculated by measuring Vtemp at 0 μA and subtracting the value with the conditions specified.

Note 11: Guaranteed by design and characterization.

Definitions of t_{EN} and $t_{V_{TEMP}}$



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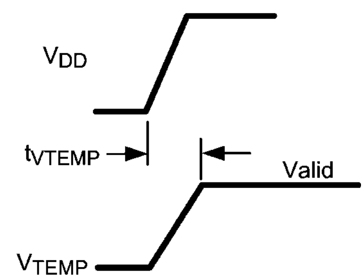

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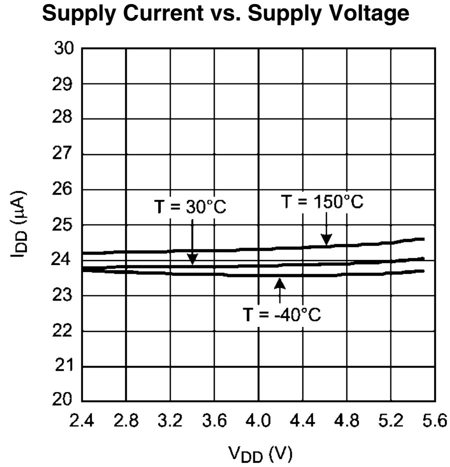
Typical Performance Characteristics

Supply Current vs. Supply Voltage



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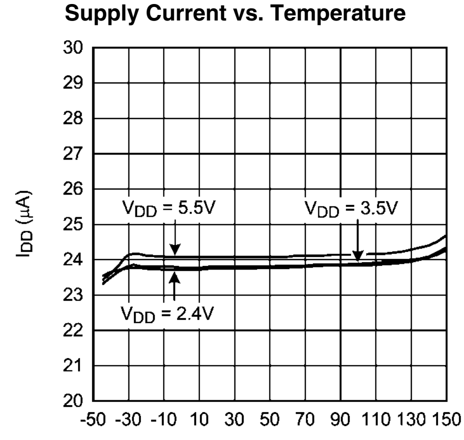
Supply Current vs. Temperature



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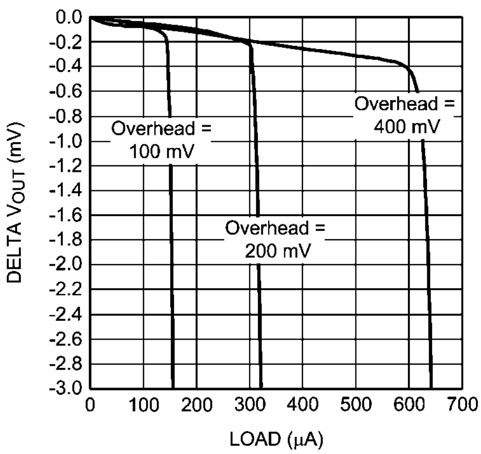
Load Regulation: Change in V_{TEMP} vs. Source Current Overhead is Vdd-Vtemp



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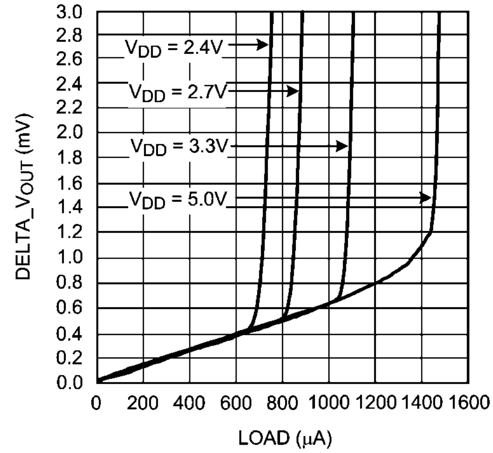
Load Regulation: Change in V_{TEMP} vs. Sink Current



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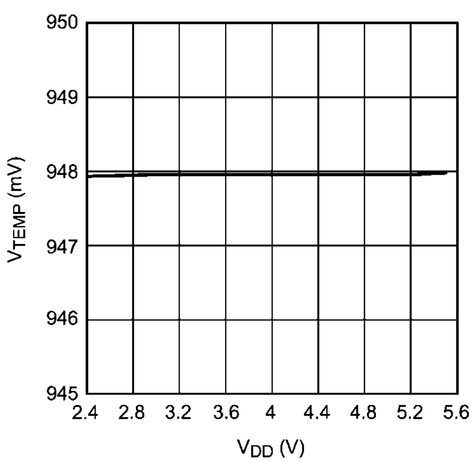
Line Regulation: V_{TEMP} vs. Supply Voltage



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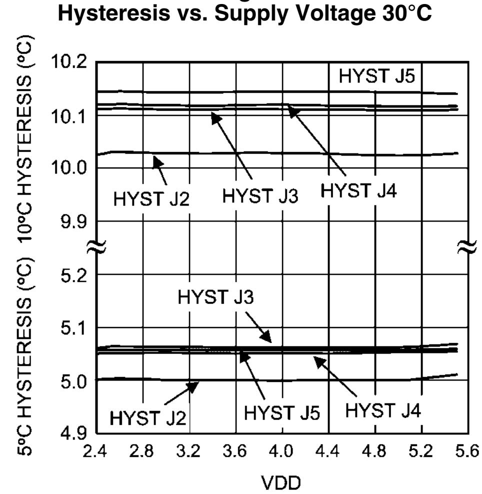
Line Regulation: Hysteresis vs. Supply Voltage 30°C



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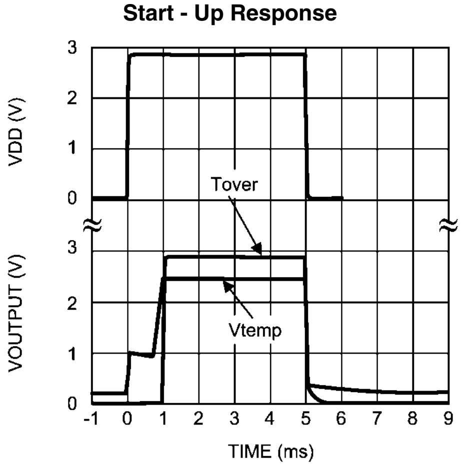
Start - Up Response



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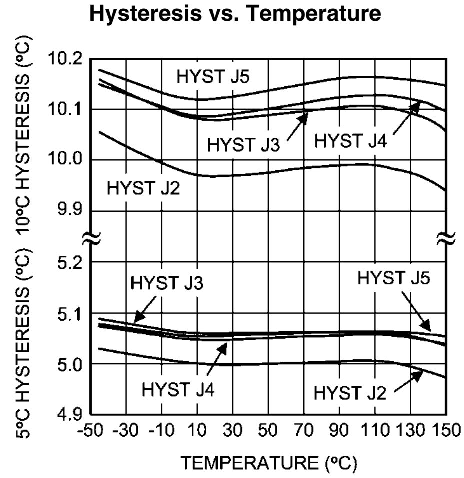
Hysteresis vs. Temperature



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Application Information

1.0 RESISTOR PROGRAMMING

Trip Point (°C) vs. Set-Resistor Values (Ω)

		R_{SENSE2}												
		J2				J3			J4		J5			
		976k	**825k**	**698k**	**590k**	**499k**	**412k**	**340k**	**280k**	**226k**	**178k**	**140k**	**105k**	**75k**
	976k	-40.7	-16.3	7.3	30.4	52.7	67.8	82.7	97.5	108.6	119.6	128.5	137.3	146.1
	825k	-39.1	-14.8	8.8	31.8	53.7	68.7	83.7	98.2	109.3	120.2	129.0	137.8	146.6
	698k	-37.6	-13.3	10.2	33.2	54.6	69.6	84.6	98.9	110.0	120.7	129.6	138.4	147.2
	590k	-36.0	-11.8	11.7	34.7	55.6	70.6	85.5	99.6	110.7	121.3	130.1	138.9	147.7
	499k	-34.5	-10.3	13.1	36.1	56.5	71.5	86.5	100.3	111.4	121.8	130.7	139.5	148.3
	412k	-32.9	-8.8	14.6	37.5	57.4	72.5	87.4	100.9	112.1	122.4	131.2	140.0	148.8
	340k	-31.4	-7.3	16.1	39.0	58.4	73.4	88.3	101.6	112.8	122.9	131.8	140.6	149.3
	280k	-29.9	-5.8	17.5	40.4	59.3	74.3	89.3	102.3	113.5	123.5	132.3	141.1	149.9
R_{SENSE1}	**226k**	-28.3	-4.3	18.9	41.8	60.3	75.3	90.2	103.0	114.2	124.0	132.9	141.7	
	178k	-26.8	-2.9	20.4	43.2	61.2	76.2	91.1	103.7	114.9	124.6	133.4	142.2	
	140k	-25.3	-1.4	21.8	44.7	62.1	77.1	92.1	104.4	115.6	125.2	134.0	142.8	
	105k	-23.8	0.0	23.2	46.1	63.1	78.1	93.0	105.1	116.3	125.7	134.5	143.3	
	75k	-22.3	1.5	24.7	47.5	64.0	79.0	93.9	105.8	117.0	126.3	135.1	143.9	
	46.4k	-20.8	3.0	26.1	48.9	65.0	79.9	94.8	106.5	117.6	126.8	135.6	144.4	
	22.6k	-19.3	4.4	27.5	50.3	65.9	80.9	95.8	107.2	118.3	127.4	136.2	145.0	
	0.01k	-17.8	5.9	28.9	51.8	66.8	81.8	96.7	107.9	119.0	127.9	136.7	145.5	

V_{TEMP} (mV) at the Trip Point vs. Set-Resistor Value (Ω)

		R_{SENSE2}												
		J2				J3			J4		J5			
		976k	**825k**	**698k**	**590k**	**499k**	**412k**	**340k**	**280k**	**226k**	**178k**	**140k**	**105k**	**75k**
	976k	1306.2	1183.8	1064.0	945.6	1243.7	1125.3	1006.8	1185.3	1066.0	1184.0	1064.6	944.8	825.0
	825k	1298.5	1176.2	1056.6	938.2	1236.3	1117.9	999.3	1177.8	1058.5	1176.6	1057.1	937.3	817.5
	698k	1290.7	1168.7	1049.1	930.8	1228.9	1110.5	991.9	1170.4	1051.0	1169.1	1049.6	929.8	810.1
	590k	1283.0	1161.2	1041.7	923.4	1221.5	1103.1	984.5	1163.0	1043.6	1161.6	1042.1	922.3	802.7
	499k	1275.3	1153.6	1034.3	916.0	1214.1	1095.7	977.1	1155.5	1036.1	1154.2	1034.6	914.8	795.2
	412k	1267.6	1146.1	1026.8	908.6	1206.7	1088.3	969.7	1148.1	1028.6	1146.7	1027.2	907.3	787.8
	340k	1259.9	1138.6	1019.4	901.2	1199.3	1080.9	962.2	1140.7	1021.1	1139.2	1019.7	899.8	780.3
	280k	1252.2	1131.0	1012.0	893.8	1191.9	1073.5	954.8	1133.2	1013.6	1131.7	1012.2	892.3	772.9
R_{SENSE1}	**226k**	1244.6	1123.5	1004.6	886.4	1184.5	1066.0	947.3	1125.8	1006.1	1124.3	1004.7	884.8	
	178k	1237.0	1116.0	997.3	879.0	1177.1	1058.6	939.9	1118.3	998.7	1116.8	997.2	877.3	
	140k	1229.4	1108.6	989.9	871.6	1169.7	1051.2	932.5	1110.9	991.2	1109.3	989.7	869.8	
	105k	1221.8	1101.2	982.5	864.2	1162.3	1043.8	925.0	1103.5	983.7	1101.8	982.2	862.3	
	75k	1214.1	1093.7	975.2	856.8	1154.9	1036.4	917.6	1096.0	976.2	1094.4	974.8	854.8	
	46.4k	1206.5	1086.3	967.8	849.4	1147.5	1029.0	910.2	1088.6	968.7	1086.9	967.3	847.3	
	22.6k	1198.9	1078.9	960.4	842.0	1140.1	1021.6	902.7	1081.2	961.2	1079.4	959.8	839.8	
	0.01k	1191.3	1071.4	953.1	834.6	1132.7	1014.2	895.3	1073.7	953.8	1072.0	952.3	832.3	

1.1 Selection of R_{SET} Resistors

To set the trip point:

(1) Locate the desired trip temperature on the Trip Point Table.

(2) Identify the corresponding R_{SENSE2} value by following the column up to the resistor value.

(3) Identify the corresponding R_{SENSE1} value by following the row leftwards to the resistor value.

(4) Use only the standard resistor values from the list.

(5) Use only the resistor with 1% tolerance and a temperature coefficient of 100ppm (or better). These restrictions are necessary to stay at the selected setting, and not to slip into an adjacent setting.

(6) This is consistent with using resistors from the Thick Film Chip Resistors CRCW0402 family. These are available with very small dimensions of L = 1.0mm, W = 0.5mm, H = 0.35mm.

(7) Note that the resistor tolerance does not diminish the accuracy of the trip point. See patent #6, 924, 758.

2.0 LM57 V_{TEMP} TEMPERATURE-TO-VOLTAGE TABLE

Temperature (°C)	V_{TEMP} (mV)			
	J2	J3	J4	J5
–50	1353	2029	2705	3381
–49	1348	2021	2695	3369
–48	1343	2014	2685	3357
–47	1338	2006	2675	3344
–46	1333	1999	2665	3332
–45	1328	1992	2655	3319
–44	1323	1984	2646	3307
–43	1318	1977	2636	3294
–42	1313	1969	2626	3282
–41	**1308**	1962	2616	3269
–40	**1303**	1954	2606	3257
–39	**1298**	1947	2596	3244
–38	**1293**	1939	2586	3232
–37	**1288**	1932	2576	3219
–36	**1283**	1924	2566	3207
–35	**1278**	1917	2556	3194
–34	**1273**	1909	2546	3182
–33	**1268**	1902	2536	3169
–32	**1263**	1894	2526	3157
–31	**1258**	1887	2516	3144
–30	**1253**	1879	2506	3132
–29	**1248**	1872	2495	3119
–28	**1243**	1864	2485	3107
–27	**1238**	1857	2475	3094
–26	**1233**	1849	2465	3082
–25	**1228**	1841	2455	3069
–24	**1223**	1834	2445	3056
–23	**1218**	1826	2435	3044
–22	**1213**	1819	2425	3031
–21	**1208**	1811	2415	3019
–20	**1203**	1804	2405	3006
–19	**1198**	1796	2395	2993
–18	**1193**	1789	2385	2981
–17	**1188**	1781	2375	2968
–16	**1182**	1773	2365	2956
–15	**1177**	1766	2354	2943
–14	**1172**	1758	2344	2930
–13	**1167**	1751	2334	2918

Temperature (°C)	V_{TEMP} (mV)			
	J2	J3	J4	J5
–12	**1162**	1743	2324	2905
–11	**1157**	1735	2314	2892
–10	**1152**	1728	2304	2880
–9	**1147**	1720	2294	2867
–8	**1142**	1713	2284	2854
–7	**1137**	1705	2273	2842
–6	**1132**	1697	2263	2829
–5	**1127**	1690	2253	2816
–4	**1122**	1682	2243	2803
–3	**1117**	1675	2233	2791
–2	**1112**	1667	2223	2778
–1	**1106**	1659	2212	2765
0	**1101**	1652	2202	2753
1	**1096**	1644	2192	2740
2	**1091**	1636	2182	2727
3	**1086**	1629	2172	2714
4	**1081**	1621	2161	2702
5	**1076**	1613	2151	2689
6	**1071**	1606	2141	2676
7	**1066**	1598	2131	2663
8	**1061**	1590	2121	2650
9	**1055**	1583	2110	2638
10	**1050**	1575	2100	2625
11	**1045**	1567	2090	2612
12	**1040**	1560	2080	2599
13	**1035**	1552	2069	2586
14	**1030**	1544	2059	2574
15	**1025**	1537	2049	2561
16	**1020**	1529	2039	2548
17	**1015**	1521	2028	2535
18	**1009**	1514	2018	2522
19	**1004**	1506	2008	2509
20	**999**	1498	1997	2497
21	**994**	1490	1987	2484
22	**989**	1483	1977	2471
23	**984**	1475	1967	2458
24	**979**	1467	1956	2445
25	**973**	1460	1946	2432

Temperature (°C)	V_{TEMP} (mV)			
	J2	J3	J4	J5
26	**968**	1452	1936	2419
27	**963**	1444	1925	2406
28	**958**	1436	1915	2394
29	**953**	1429	1905	2381
30	**948**	1421	1894	2368
31	**942**	1413	1884	2355
32	**937**	1405	1874	2342
33	**932**	1398	1863	2329
34	**927**	1390	1853	2316
35	**922**	1382	1843	2303.0
36	**917**	1374	1832	2290
37	**911**	1367	1822	2277
38	**906**	1359	1811	2264
39	**901**	1351	1801	2251
40	**896**	1343	1791	2238
41	**891**	1335	1780	2225
42	**885**	1328	1770	2212
43	**880**	1320	1759	2199
44	**875**	1312	1749	2186
45	**870**	1304	1739	2173
46	**865**	1296	1728	2160
47	**859**	1289	1718	2147
48	**854**	1281	1707	2134
49	**849**	1273	1697	2121
50	**844**	1265	1687	2108
51	**839**	1257	1676	2095
52	**833**	1249	1666	2082
53	828	**1242**	1655	2069
54	823	**1234**	1645	2056
55	818	**1226**	1634	2043
56	812	**1218**	1624	2030
57	807	**1210**	1613	2016
58	802	**1202**	1603	2003
59	797	**1194**	1592	1990
60	791	**1187**	1582	1977
61	786	**1179**	1571	1964
62	781	**1171**	1561	1951
63	776	**1163**	1550	1938
64	770	**1155**	1540	1925
65	765	**1147**	1529	1911
66	760	**1139**	1519	1898
67	755	**1131**	1508	1885
68	749	**1124**	1498	1872
69	744	**1116**	1487	1859
70	739	**1108**	1477	1846
71	734	**1100**	1466	1833
72	728	**1092**	1456	1819
73	723	**1084**	1445	1806

Temperature (°C)	V_{TEMP} (mV)			
	J2	J3	J4	J5
74	718	**1076**	1435	1793
75	713	**1068**	1424	1780
76	707	**1060**	1413	1767
77	702	**1052**	1403	1753
78	697	**1044**	1392	1740
79	691	**1036**	1382	1727
80	686	**1028**	1371	1714
81	681	**1021**	1360	1700
82	675	**1013**	1350	1687
83	670	**1005**	1339	1674
84	665	**997**	1329	1661
85	660	**989**	1318	1647
86	654	**981**	1307	1634
87	649	**973**	1297	1621
88	644	**965**	1286	1607
89	638	**957**	1276	1594
90	633	**949**	1265	1581
91	628	**941**	1254	1568
92	622	**933**	1244	1554
93	617	**925**	1233	1541
94	612	**917**	1222	1528
95	606	**909**	1212	1514
96	601	**901**	1201	1501
97	596	893	**1190**	1488
98	590	885	**1180**	1474
99	585	877	**1169**	1461
100	580	869	**1158**	1448
101	574	861	**1148**	1434
102	569	853	**1137**	1421
103	564	845	**1126**	1407
104	558	837	**1115**	1394
105	553	829	**1105**	1381
106	548	821	**1094**	1367
107	542	813	**1083**	1354
108	537	805	**1073**	1340
109	531	797	**1062**	1327
110	526	788	**1051**	1314
111	521	780	**1040**	1300
112	515	772	**1030**	1287
113	510	764	**1019**	1273
114	505	756	**1008**	1260
115	499	748	**997**	1246
116	494	740	**986**	1233
117	488	732	**976**	1219
118	483	724	**965**	1206
119	478	716	**954**	1192
120	472	708	943	**1179**
121	467	700	933	**1165**

Temperature (°C)	V_{TEMP} (mV) J2	J3	J4	J5
122	461	692	922	**1152**
123	456	683	911	**1138**
124	451	675	900	**1125**
125	445	667	889	**1111**
126	440	659	878	**1098**
127	434	651	868	**1084**
128	429	643	857	**1071**
129	424	635	846	**1057**
130	418	627	835	**1044**
131	413	618	824	**1030**
132	407	610	813	**1017**
133	402	602	803	**1003**
134	396	594	792	**989**
135	391	586	781	**976**
136	386	578	770	**962**
137	380	570	759	**949**

Temperature (°C)	V_{TEMP} (mV) J2	J3	J4	J5
138	375	561	748	**935**
139	369	553	737	**921**
140	364	545	726	**908**
141	358	537	716	**894**
142	353	529	705	**881**
143	347	520	694	**867**
144	342	512	683	**853**
145	336	504	672	**840**
146	331	496	661	**826**
147	326	488	650	**812**
148	320	480	639	**799**
149	315	471	628	**785**
150	309	463	617	**771**

Note: The Rset resistors select a trip point and a corresponding Vtemp gain (J2, J3, J4, or J5). The trip point range associated with a given gain is shown in bold on this table. The Vtemp gain is selected by the Rset resistors. Vtemp is valid over the entire temperature range.

2.1 LM57 V_{TEMP} Voltage -To-Temperature Equations

Trip-Point Region	LM57 Trip Point Range	V_{TEMP} (mV) Equations T(°C)
J2	–41°C to 52°C	$V_{TEMP} = 947.6 - 5.166(T-30) - 0.00129(T-30)^2$
J3	52°C to 97°C	$V_{TEMP} = 1420.9 - 7.752(T-30) - 0.00191(T-30)^2$
J4	97°C to 119°C	$V_{TEMP} = 1894.3 - 10.339(T-30) - 0.00253(T-30)^2$
J5	119°C to 150°C	$V_{TEMP} = 2367.7 - 12.924(T-30) - 0.00316(T-30)^2$

3.0 T_{OVER} AND $\overline{T_{OVER}}$ DIGITAL OUTPUTS

The T_{OVER} Active High, Push-Pull Output and the $\overline{T_{OVER}}$ Active Low, Open-Drain Output both assert at the same time whenever the Die Temperature reaches the Trip Point. They also assert simultaneously whenever the TRIP TEST pin is set high. Both outputs de-assert when the die temperature goes below the (Temperature Trip Point) - (Hysteresis). These two types of digital outputs enable the user the flexibility to choose the type of output that is most suitable for his design.

Either the T_{OVER} or the $\overline{T_{OVER}}$ Digital Output pins can be left open if not used.

The $\overline{T_{OVER}}$ Active Low, Open-Drain Digital Output, if used, requires a pull-up resistor between this pin and V_{DD}.

3.1 T_{OVER} and $\overline{T_{OVER}}$ Noise Immunity

The LM57 has some noise immunity to a premature trigger due to noise on the power supply. With the die temperature at 1°C below the trip point, there are no premature triggers for a square wave injected into the power supply with a magnitude of 100 mV_{PP} over a frequency range of 100 Hz to 2 MHz. Above the frequency a premature trigger may occur.

With the die temperature at 2°C below the trip point, and a magnitude of 200 mV_{PP}, there are no premature triggers from 100 Hz to 300 kHz. Above that frequency a premature trigger may occur.

Therefore if the supply line is noisy, it is recommended that a local supply decoupling cap be used to reduce that noise.

4.0 TRIP TEST DIGITAL INPUT

The TRIP TEST pin provides a means to test the digital outputs by causing them to assert, regardless of temperature.

In addition, when the TRIP TEST pin is pulled high the V_{TEMP} pin will be at the V_{TRIP} voltage.

5.0 V_{TEMP} ANALOG TEMPERATURE SENSOR OUTPUT

The V_{TEMP} push-pull output provides the ability to sink and source significant current. This is beneficial when, for example, driving dynamic loads like an input stage on an analog-to-digital converter (ADC). In these applications the source current is required to quickly charge the input capacitor of the ADC. See the Applications Circuits section for more discussion of this topic. The LM57 is ideal for this and other applications which require strong source or sink current.

5.1 V_{TEMP} Noise Considerations

A load capacitor on V_{TEMP} can help to filter noise.

For noisy environments, a 100nF supply decoupling cap placed closed across V_{DD} and GND pins of LM57 is recommended.

5.2 V_{TEMP} Capacitive Loads

The V_{TEMP} Output handles capacitive loading well. In an extremely noisy environment, or when driving a switched sampling input on an ADC, it may be necessary to add some filtering to minimize noise coupling. Without any precautions, the V_{TEMP} can drive a capacitive load less than or equal to 1100 pF as shown in *Figure 2*. For capacitive loads greater than 1100 pF, a series resistor is required on the output, as shown in *Figure 3*, to maintain stable conditions.

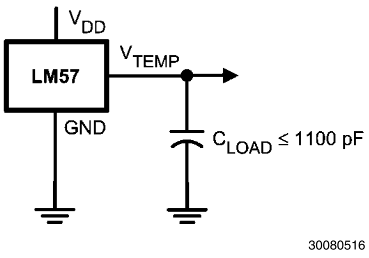
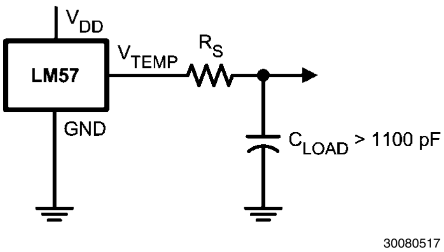


FIGURE 2. LM57 No Isolation Resistor Required



C_{LOAD}	Minimum R_S
1.1 nF to 99 nF	3 kΩ
100 nF to 999 nF	1.5 kΩ
1 µF	750 Ω

FIGURE 3. LM57 with Series Resistor for Capacitive Loading greater than 1100 pF.

5.3 V_{TEMP} Voltage Shift

The LM57 is very linear over temperature and supply voltage range. Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of V_{DD} and V_{TEMP}. The shift typically occurs when $V_{DD} - V_{TEMP} = 1.0V$.

This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in V_{DD} or V_{TEMP}. Since the shift takes place over a wide temperature change of 5°C to 20°C, V_{TEMP} is always monotonic. The accuracy specifications in the Electrical Characteristics table already includes this possible shift.

6.0 MOUNTING AND TEMPERATURE CONDUCTIVITY

The LM57 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface.

To ensure good temperature conductivity, the backside of the LM57 die is directly attached to the exposed pad. The temperatures of the lands and traces to the other leads of the LM57 will also affect the temperature reading.

Alternatively, the LM57 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM57 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. If moisture creates a short circuit from the

V_{TEMP} output to ground or V_{DD}, the V_{TEMP} output from the LM57 will not be correct. Printed-circuit coatings are often used to ensure that moisture cannot corrode the leads or circuit traces.

The LM57's junction temperature is the actual temperature being measured. The thermal resistance junction-to-ambient (θ_{JA}) is the parameter (from Figure 4) used to calculate the rise of a device junction temperature due to its power dissipation. The equation used to calculate the rise in the LM57's die temperature is

$$T_J = T_A + \theta_{JA} \left[(V_{DD} I_Q) + (V_{DD} - V_{TEMP})\ I_L \right]$$

where T_A is the ambient temperature, I_Q is the quiescent current, I_L is the load current on Vtemp.

For example, in an application where T_A = 30 °C, V_{DD} = 5.5 V, I_{DD} = 28 µA, J5 gain, V_{TEMP} = 2368 mV, and I_L = 0 µA, the total temperature rise would be [152°C/W*5.5V*28µA] = 0.023°C. To minimize self-heating, the load current on Vtemp should be minimized.

Device Number	Thermal Resistance (θ_{JA})	NS Package Number
LM57	152° C/W	SDA08B

FIGURE 4. LM57 Thermal Resistance

7.0 Rset TABLE

The LM57 uses the voltage at the two Rsense pins to set the trip point for the temperature switch. It is possible to drive the two Rsense pins with a voltage equal to the value generated by the resistor and the internal current-source and have the same switch point. Thus one can use an external DAC to drive each Rsense pin, allowing for the temperature trip point to be set dynamically by the system processor. The table shows the Rset value and its corresponding generated Rsense pin voltage (the “Center Value").

Rset Values (kΩ) vs Rsense Voltage (mV)

Rset (Ω)	Rsense Voltage (mV)
	Center Value
976k	1875
825k	1585
698k	1341
590k	1134
499k	959
412k	792
340k	653
280k	538
226k	434
178k	342
140k	269
105k	202
75k	146
46.4k	87
22.6k	43
0.01k	0

Applications Circuits

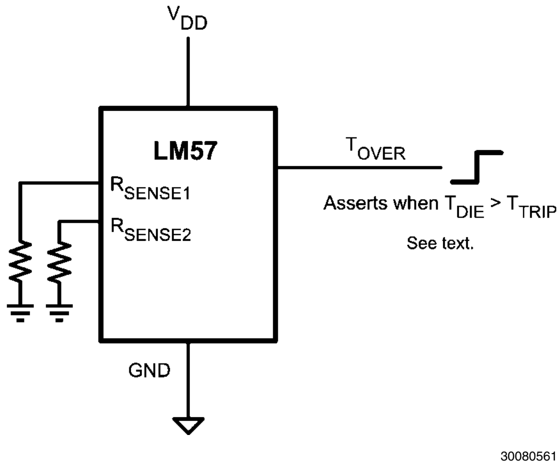


FIGURE 5. Temperature Switch Using Push-Pull Output

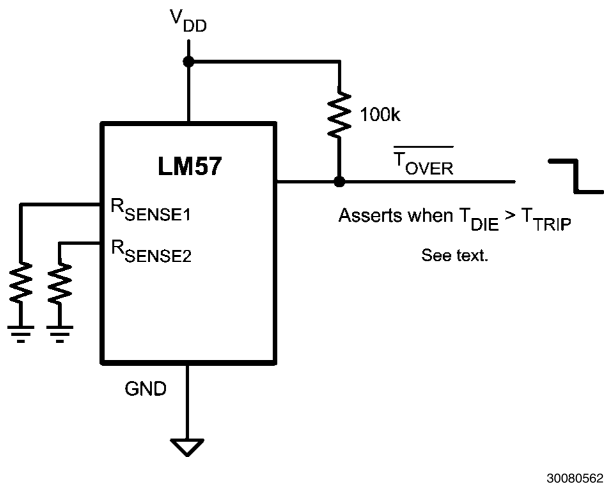
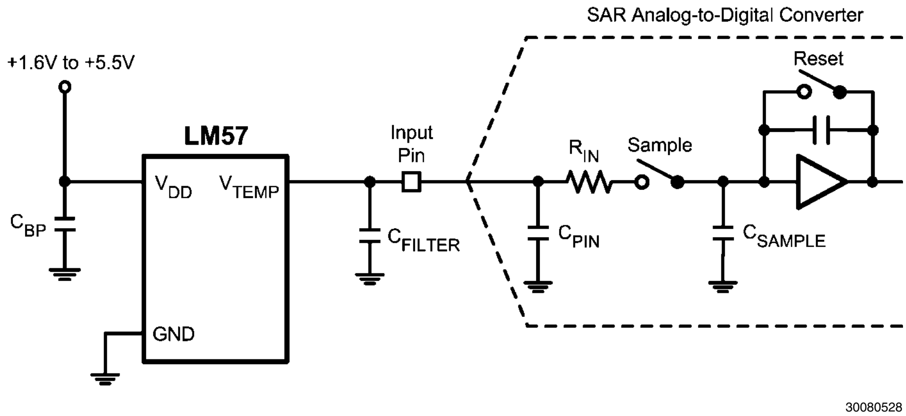


FIGURE 6. Temperature Switch Using Open-Drain Output



Most CMOS ADCs found in microcontrollers and ASICs have a sampled data comparator input structure. When the ADC charges the sampling cap, it requires instantaneous charge from the output of the analog source such as the LM57 temperature sensor and many op amps. This requirement is easily accommodated by the addition of a capacitor (C_{FILTER}). The size of C_{FILTER} depends on the size of the sampling capacitor and the sampling frequency. Since not all ADCs have identical input stages, the charge requirements will vary. This general ADC application is shown as an example only.

FIGURE 7. Suggested Connection to a Sampling Analog-to-Digital Converter Input Stage

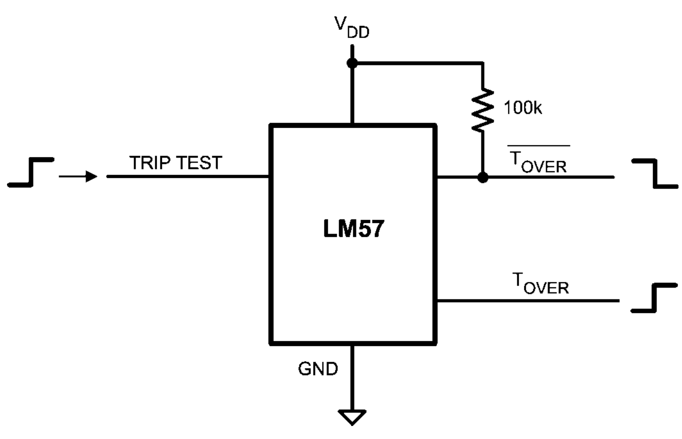
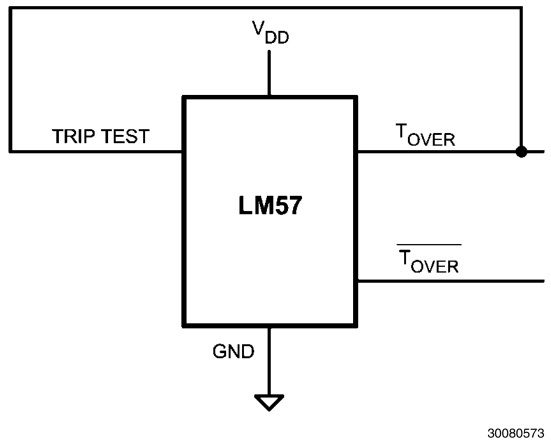
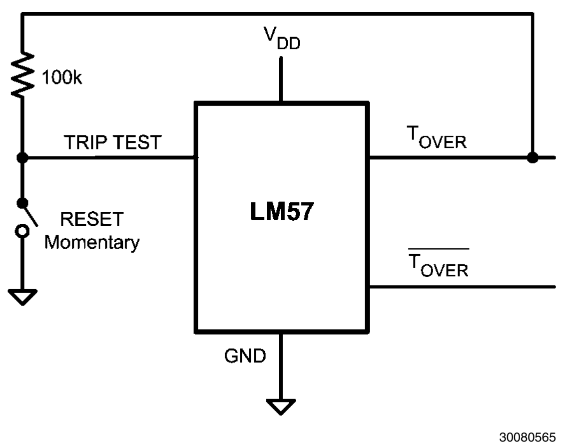


FIGURE 8. TRIP TEST Digital Output Test Circuit



When Tover goes active high, it drives Trip Test high. Trip Test high causes Tover to stay high. It is therefore latched. To release the latch: Power down then power up. The LM57 always comes up in a released condition.

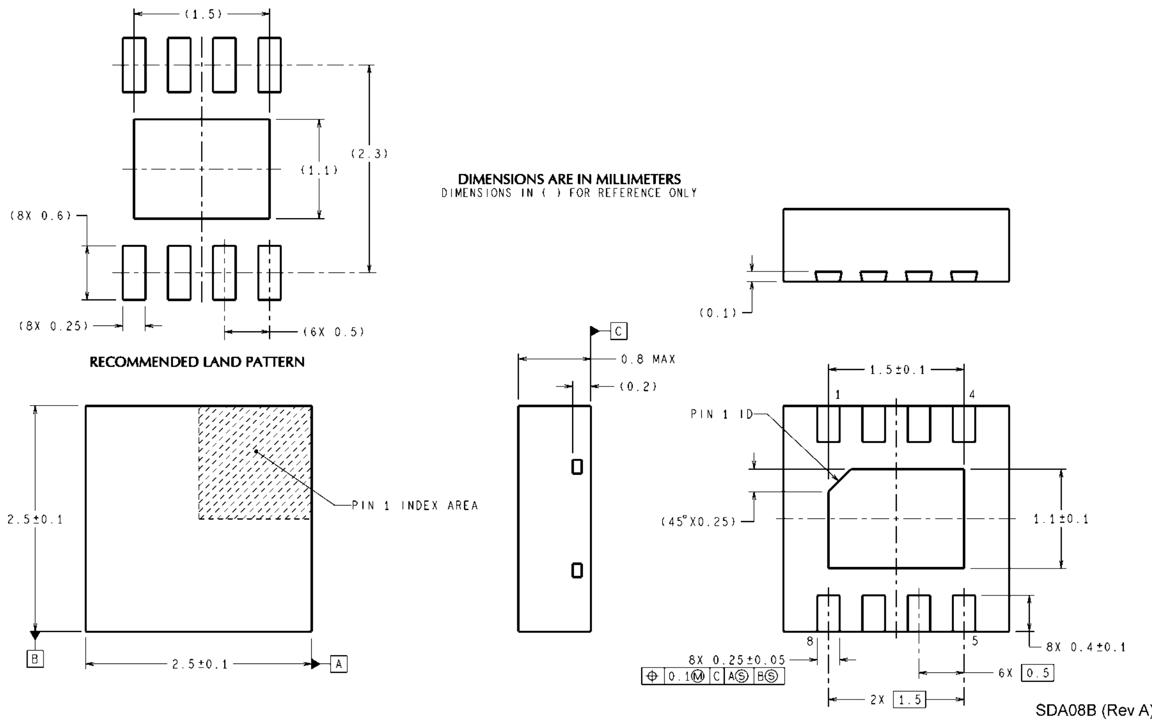
FIGURE 9. Simple Latch Circuit



The TRIP TEST pin, normally used to check the operation of the T_{OVER} and $\overline{T_{OVER}}$ pins, may be used to latch the outputs whenever the temperature exceeds the programmed limit and causes the digital outputs to assert. As shown in the figure, when T_{OVER} goes high the TRIP TEST input is also pulled high and causes T_{OVER} output to latch high and the $\overline{T_{OVER}}$ output to latch low. Momentarily switching the TRIP TEST input low will reset the LM57 to normal operation. The resistor limits the current out of the T_{OVER} output pin.

FIGURE 10. Latch Circuit using T_{OVER} Output

Physical Dimensions inches (millimeters) unless otherwise noted



8-Pin LLP
NS Package Number SDA08B

Notes

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Voltage Reference	www.national.com/vref	Design Made Easy	www.national.com/easy
PowerWise® Solutions	www.national.com/powerwise	Solutions	www.national.com/solutions
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