16-BIT COLOR LED DRIVER WITH PWM CONTROL

January 2012

GENERAL DESCRIPTION

The IS31FL3726 is comprised of constant-current drivers designed for color LEDs. The output current value can be set using an external resistor. The output current value can be adjusted from 5mA to 60mA through the external resistor.

As a result, all outputs will have virtually the same current levels.

This driver incorporates 16-bit constant t-current outputs, a 16-bit shift register, a 16-bit latch and a 16-bit AND-gate circuit.

These drivers have been designed using the CMOS process.

APPLICATIONAS

- Cellular phones
- MP3/MP4/CD/minidiskplayers
- Toys

FEATURES

- Output current capability and number of outputs: 60mA × 16 outputs
- Constant current range: 5mA to 60mA
- Application output voltage: ≥0.4V
- For anode-common LEDs
- Power supply voltage range, V_{DD} = 3.3V to 5.5V
- Serial and parallel data transfer rate: 20MHz (Max. cascade connection)
- Operating temperature range, T_A = −40°C ~ +85°C
- Package: QFN-24
- Current accuracy (All output on)

Output voltage	Current Accuracy		Output Current
	Between Bits	Between ICs	
≥0.4V	±4%	±12%	5 to 60 mA

BLOCK DIAGRAM

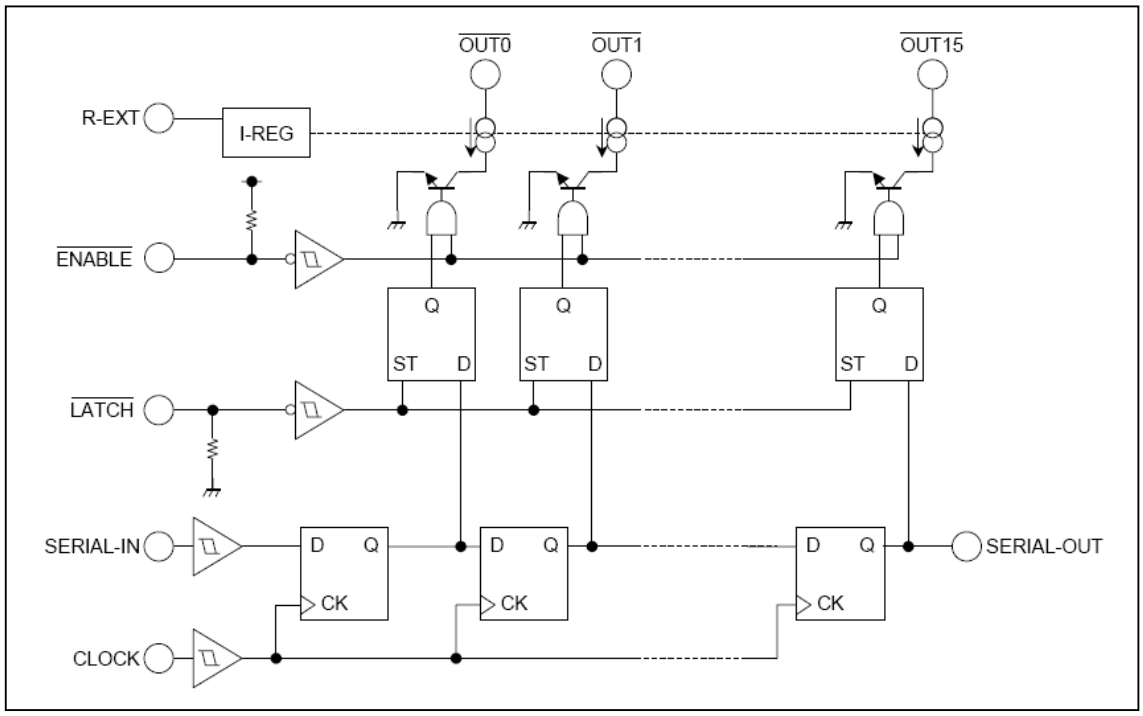


Figure 1 Block Diagram

TYPICAL APPLICATION CIRCUIT

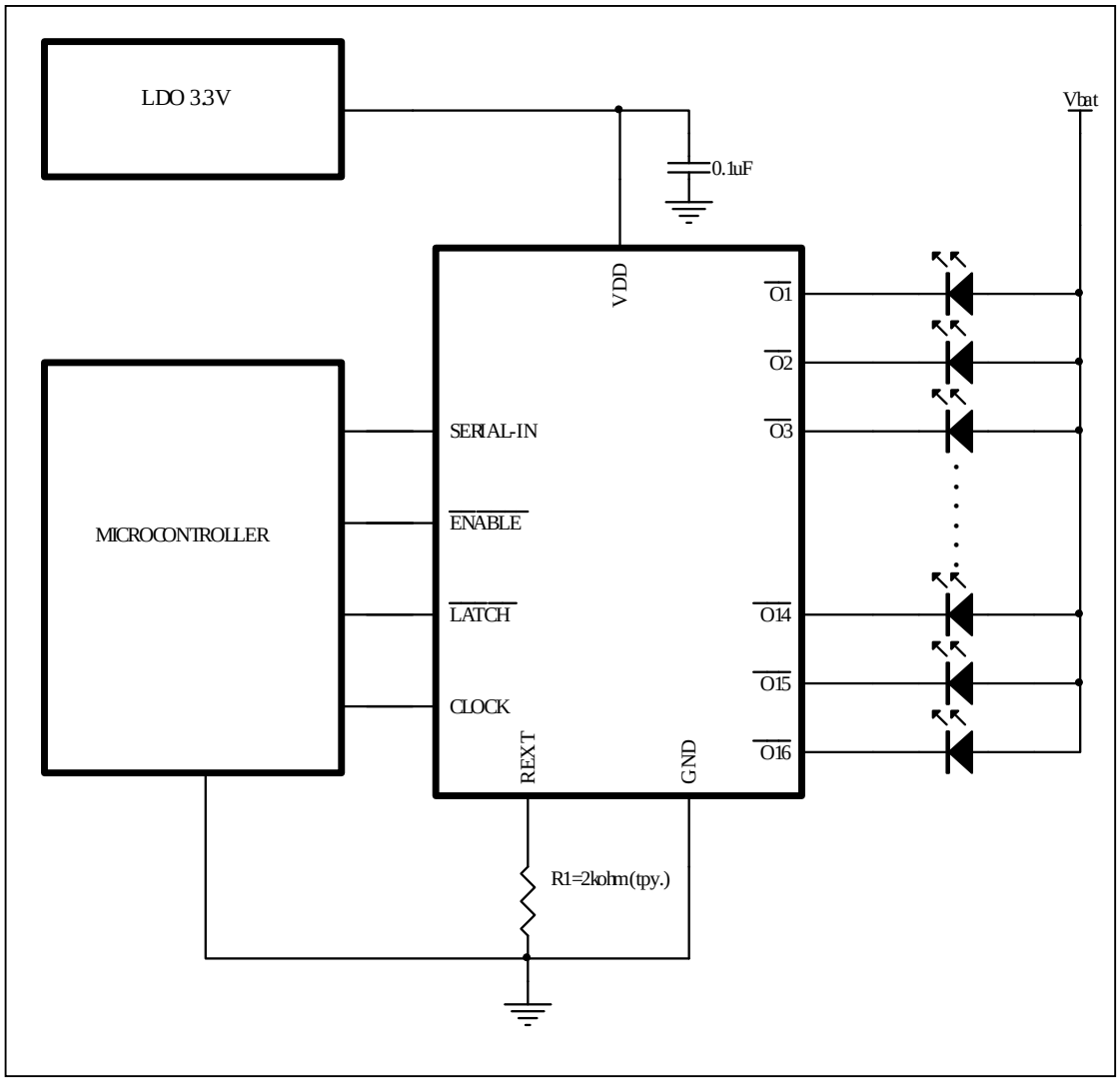
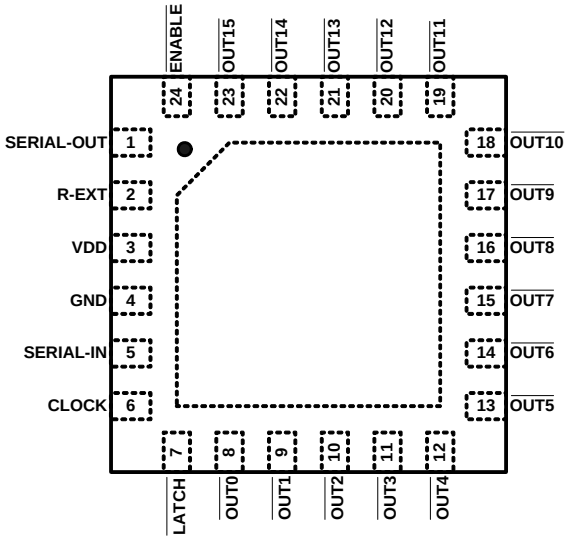


Figure 2 Typical Application Figure

PIN CONFIGURATION

Package	Pin Configuration (Top View)
QFN-24	

PIN DESCRIPTION

No	Pin	Description
1	SERIAL-OUT	Output terminal for serial data input on SERIAL-IN terminal.
2	R-EXT	Input terminal used to connect an external resistor. This regulated the output current.
3	VDD	Supply voltage terminal.
4	GND	GND terminal for control logic.
5	SERIAL-IN	Input terminal for serial data for data shift register.
6	CLOCK	Input terminal for clock for data shift on rising edge.
7	$\overline{\text{LATCH}}$	Input terminal for data strobe When the $\overline{\text{LATCH}}$ input is driven High, data is not latched. When it is pulled Low ，data is latched.
8 ~ 23	$\overline{\text{OUT0}}$~$\overline{\text{OUT15}}$	Constant-current output terminals.
24	$\overline{\text{ENABLE}}$	Input terminal for output enable. All outputs ($\overline{\text{OUT0}}$ to $\overline{\text{OUT15}}$) are turned off, when the $\overline{\text{ENABLE}}$ terminal is driven High .And are turned on, when the terminal is driven Low.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

Order Part No.	Package	QTY/Reel
IS31FL3726-QFLS2-TR	QFN-24, Lead-free	2500

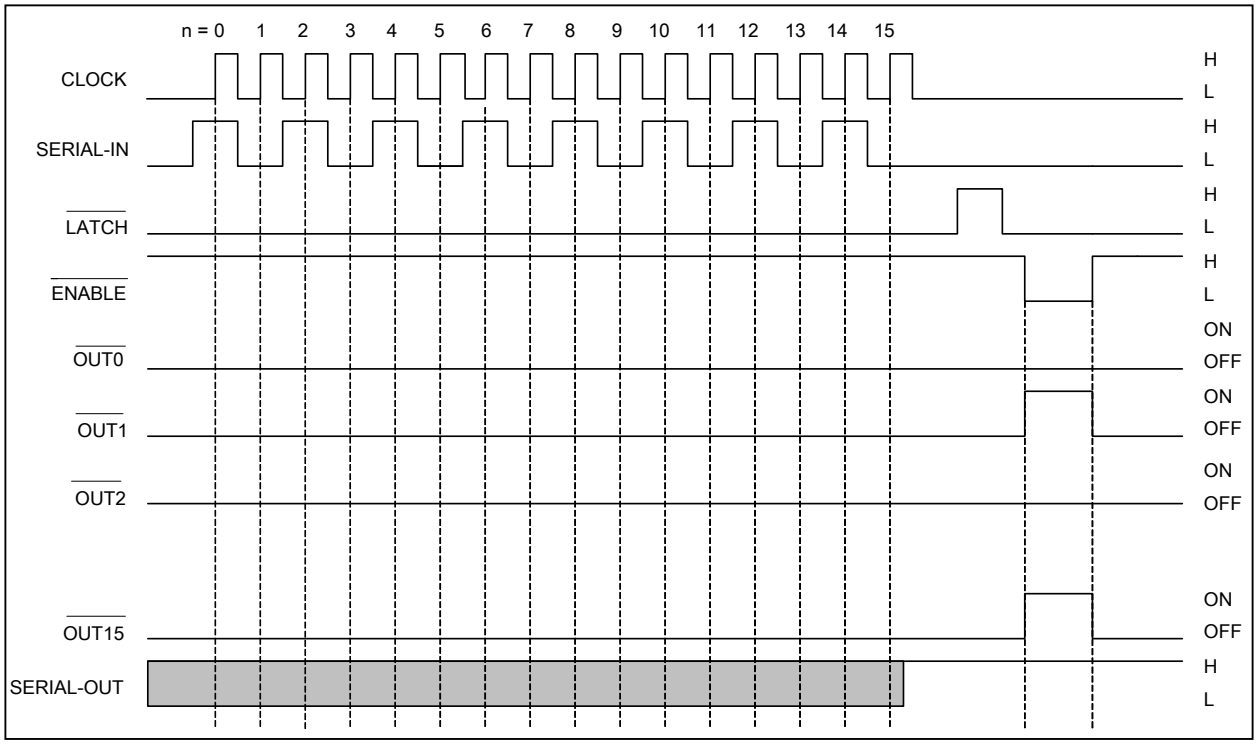


Figure 3 Timing Dagram

Warning: Latch circuit is leveled-latch circuit. Be careful because it is not triggered-latch circuit.

Note : The latches circuit holds data by pulling the LATCH terminal Low. And, when LATCH terminal is a High level, latch circuit doesn't hold data, and it passes from the input to the output. When ENABLE terminal is a Low level, output terminal OUT0 to OUT15 respond to the data, and on and off does. And, when ENABLE terminal is a High level, it offs with the output terminal regardless of the data.

Truth Table

CLOCK	LATCH	ENABLE	SERIAL-IN	OUT0 …OUT7 … OUT15	SERIAL-OUT
↑	H	L	Dn	Dn …Dn-7 …Dn-15	Dn-15
↑	L	L	Dn+1	No change	Dn-14
↑	H	L	Dn+2	Dn+2 …Dn-5 …Dn-13	Dn-13
↓	X	L	Dn+3	Dn+2 …Dn-5 …Dn-13	Dn-13
↓	X	H	Dn+3	OFF	Dn-13

Note : OUT0 to OUT15 =On when Dn = H; OUT0 to OUT15 =Off when Dn = L. In order to ensure that the level of the power supply voltage is correct, an external resistor must be connected between R-EXT and GND.

Warning: When V_{DD} < 2.5V or the start up time is less than 1ms, the following conditions, ENABLE=0, LATCH=1, SERIAL-IN=1, cannot be configured at the same time, or SN3726 will be abnormal.

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	−0.3V ~ +6.0V
Voltage at any input pin	−0.3V ~ V_{DD}+0.2V
Maximum junction temperature, T_{JMAX}	150°C
Storage temperature range, T_{STG}	−65°C ~ +150°C
Operating temperature range, T_A	−40°C ~ +85°C
ESD (HBM)	3kV

Note:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITION

T_A = 25°C, unless otherwise specified.

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}		3.3		5.5	V
Output voltage	V_{OUT}			0.7	4	V
Output current	I_{OUT}	Each DC 1 circuit	5		60	mA/ch
	I_{OH}	SERIAL-OUT			-1	mA
	I_{OL}	SERIAL-OUT			1	
Input voltage	V_{IH}		1.4			V
	V_{IL}				0.4	
Clock frequency	f_{CLK}	Cascade connected			20	MHz
$\overline{LATCH}$ pulse width	t_{wLAT}		50			ns
CLOCK pulse width	t_{wCLK}		25			ns
$\overline{ENABLE}$ pulse width (note)	t_{wENA}	Upper I_{OUT} = 20mA	2000			ns
		Lower I_{OUT} = 20mA	3000			
Set-up time for CLOCK terminal	t_{SETUP1}		10			ns
Hold time for CLOCK terminal	t_{HOLD}		10			ns
Set-up time for $\overline{LATCH}$ terminal	t_{SETUP2}		50			ns

Note : When the pulse of the Low level is input to the $\overline{ENABLE}$ terminal held in the High level.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{DD} = 3.3V ~ 5.5V, unless otherwise specified.

Characteristic	Symbol	Condition		Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	Normal operation		3.3		5.5	V
Output current	I_{OUT1}	V_{OUT} = 0.4V V_{DD} = 3.3V	R_{EXT} = 1kΩ	15	18.7	22	mA
	I_{OUT2}	V_{OUT} = 0.4V V_{DD} = 5V		15	18.9	22	
Output current error between bits	$\triangle I_{OUT1}$	V_{OUT}≥0.4V, All outputs on	R_{EXT} = 1kΩ		±3	±4	%
Output leakage current input voltage	I_{OZ}	V_{OUT} = 5.0V				1	uA
Input voltage	V_{IH}			1.4			V
	V_{IL}					0.4	
SOUT terminal voltage	V_{OL}	I_{OL} = 1.0mA, V_{DD} = 3.3V				0.3	V
		I_{OL} = 1.0mA, V_{DD} = 5V				0.3	
	V_{OH}	I_{OH} = -1.0mA, V_{DD} = 3.3V		3			
		I_{OH} = -1.0mA, V_{DD} = 5V		4.7			
Output current supply voltage regulation	%/V_{DD}	When V_{DD} is changed 3.3V to 5.5V			-1		%
Pull-up resistor	$R_{(Up)}$	$\overline{ENABLE}$ terminal		250	500	750	kΩ
Pull-down resistor	$R_{(Down)}$	$\overline{LATCH}$ terminal					
Supply current	$I_{DD(OFF)1}$	V_{OUT} = 5V	R_{EXT} = OPEN		1		mA
	$I_{DD(OFF)2}$	V_{OUT} = 5V All outputs off	R_{EXT} = 1kΩ		4.5		
	$I_{DD(ON)1}$	V_{OUT} = 0.7V All outputs on	R_{EXT} = 1kΩ		5		

SWITCHING CHARACTERISTICS

T_A = 25°C, unless otherwise specified.

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation delay	t_{pLH1}	CLK-$\overline{OUTn}$, $\overline{LATCH}$ = "H" $\overline{ENABLE}$ = "L"		80	200	ns
	t_{pLH2}	$\overline{LATCH}$–$\overline{OUTn}$, $\overline{ENABLE}$ = "L"		80	200	
	t_{pLH3}	$\overline{ENABLE}$-$\overline{OUTn}$, $\overline{LATCH}$ = "H"		130	250	
	t_{pLH}	CLK-SERIAL OUT	3	5		
	t_{pHL1}	CLK-$\overline{OUTn}$, $\overline{LATCH}$ = "H" $\overline{ENABLE}$ = "L"		160	250	
	t_{pHL2}	$\overline{LATCH}$-$\overline{OUTn}$, $\overline{ENABLE}$ = "L"		160	250	
	t_{pHL3}	$\overline{ENABLE}$-$\overline{OUTn}$, $\overline{LATCH}$ = "H"		200	350	
	t_{pLH}	CLK-SERIAL OUT	4	6		
Output rise time	t_{or}	10%~90% of voltage waveform	30	150	200	ns
Output fall time	t_{of}	90%~10% of voltage waveform	150	200	250	ns
Maximum CLOCK rise time	t_r	When not on PCB （Note ）			5	us
Maximum CLOCK fall time	t_f				5	us

Conditions: (Refer to test circuit.)

Topr = 25°C, V_{DD}=V_{IH} =3.3 V and 5 V, V_{OUT} = 0.7 V, V_{IL} =0 V, R_{EXT} =1000Ω,V_L =3.0 V, R_L=60Ω, C_L=10.5 pF

Note:

1. If the device is connected in a cascade and tr/tf for the waveform is large, it may not be possible to achieve the timing required for data transfer. Please consider the timings carefully.

2. Delay between outputs. The IS31FL3726 has graduated delay circuits between outputs. The fixed delay time is 5ns (typical), OUT1 has 5ns delay, OUT2 has 10 ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on. The delay works during switch on and switch off of each output channel. LEDs that have not turned on before $\overline{ENABLE}$ is low will still turn on and off at the determined delayed time regardless of the state of $\overline{ENABLE}$. Therefore, every LED will be illuminated for the amount of time $\overline{ENABLE}$ is pulled high.

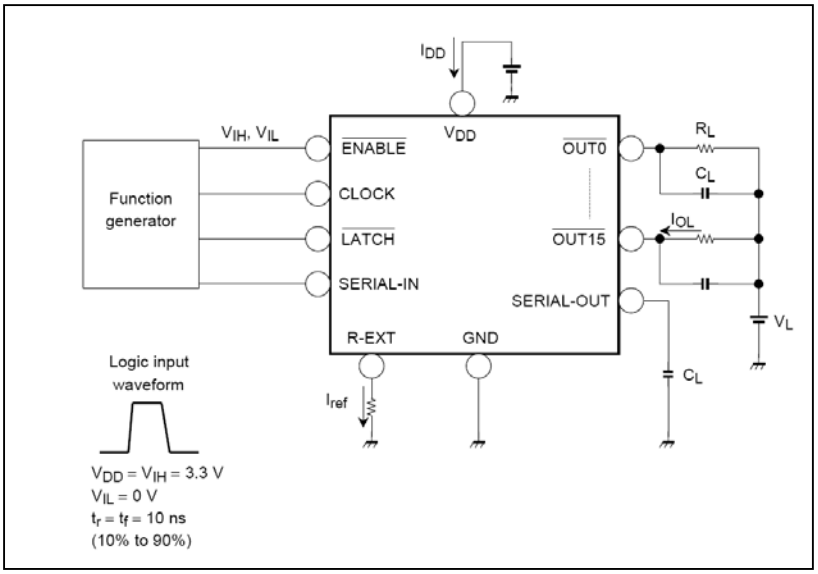
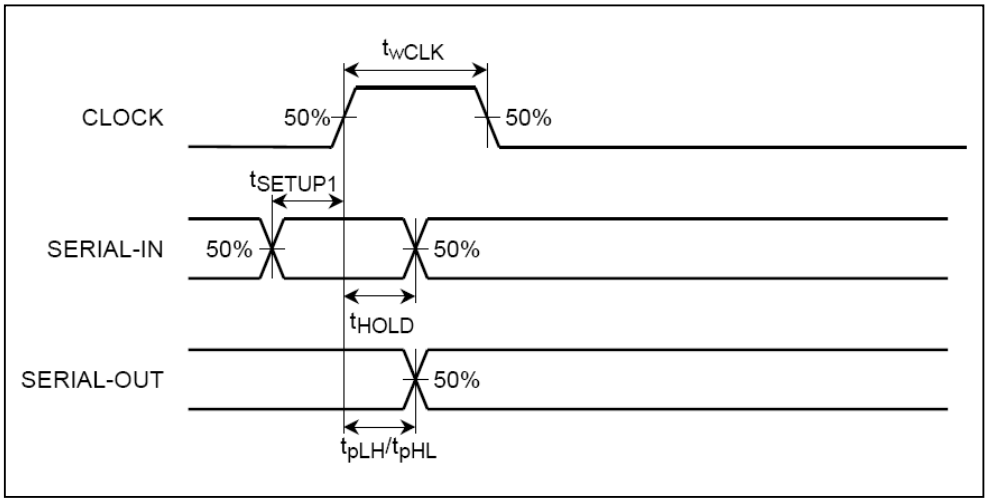


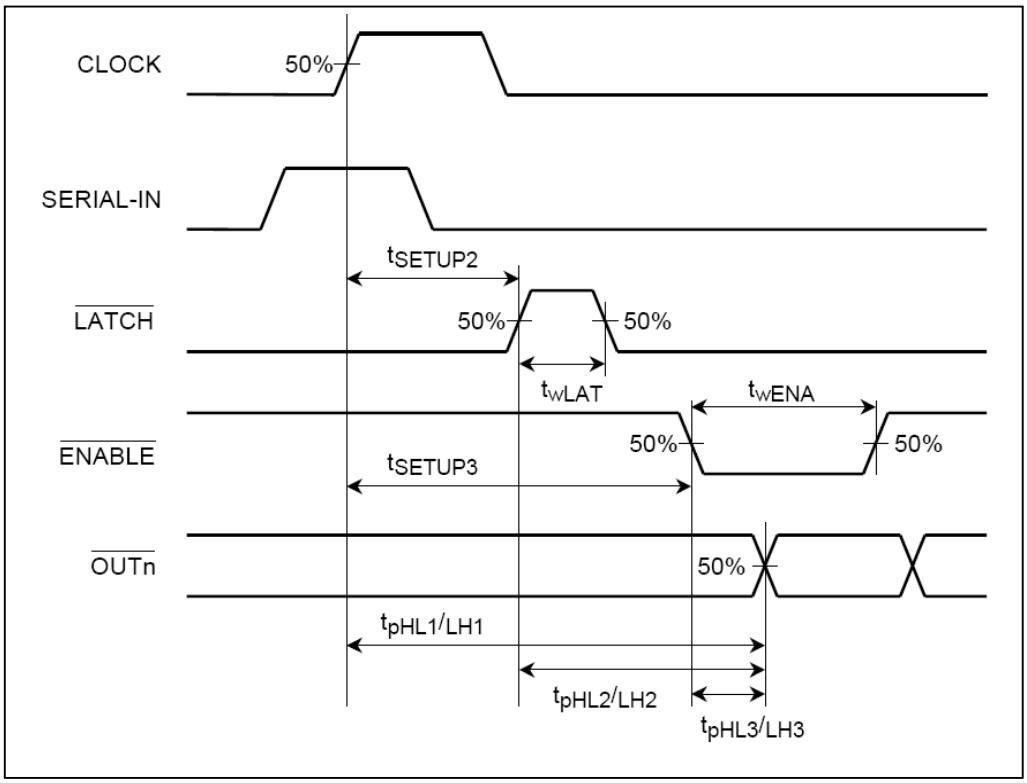
Figure 4 Test Diagram

TIMING WAVEFORM

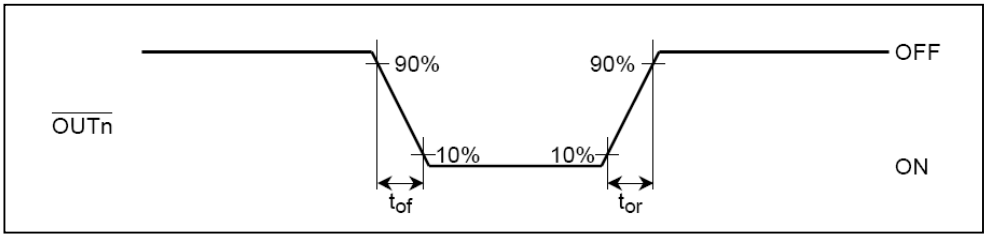
1. CLOCK, SERIAL-IN,SERIAL-OUT



2. CLOCK, SERIAL-IN, $\overline{\text{LATCH}}$, $\overline{\text{ENABLE}}$, $\overline{\text{OUTn}}$



3. $\overline{\text{OUTn}}$



TYPICAL OPERATING CHARACTERISTICS

ADJUSTING OUTPUT CURRENT

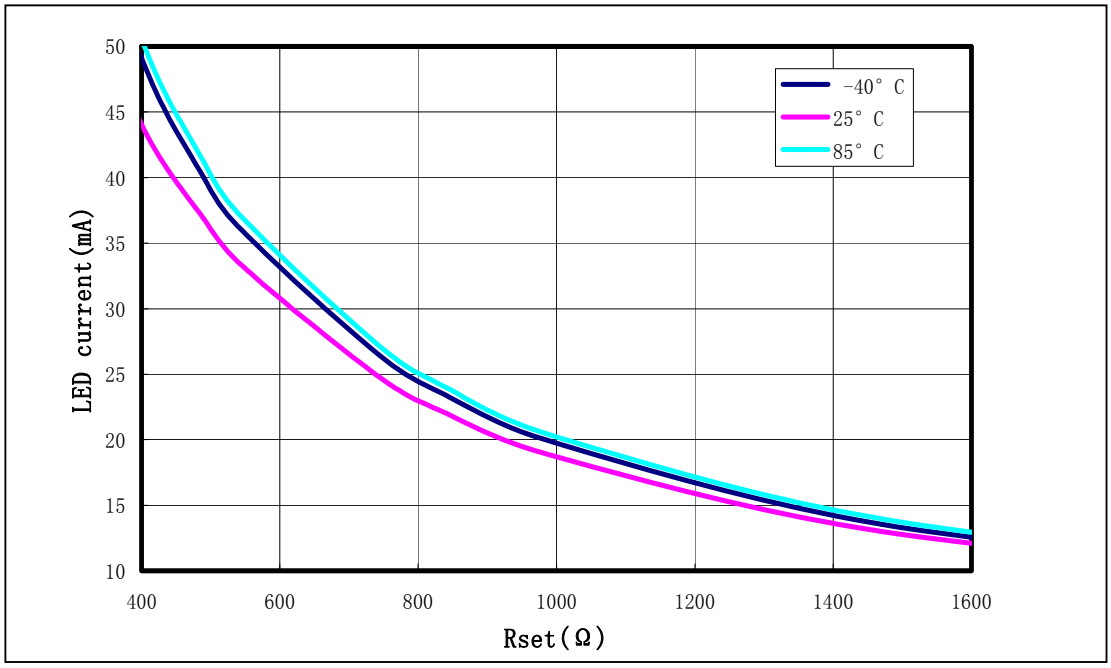
The output current of each channel is set by an external resistor R_{ext}, the relationship between I_{out} and R_{ext} is:

$$I_{out} = (V_{R\text{-}ext}/R_{ext})\times 52$$

the $V_{R\text{-}ext}$ is 0.36V in the IS31FL3726,so we can count the I_{out} as :

$$I_{out} = 0.36\times 52/R_{ext}.$$

As show in the figure below:



CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

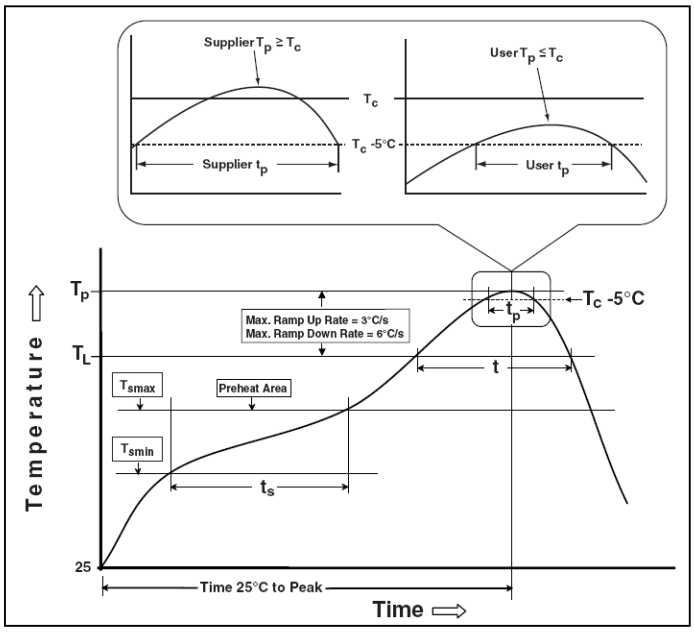
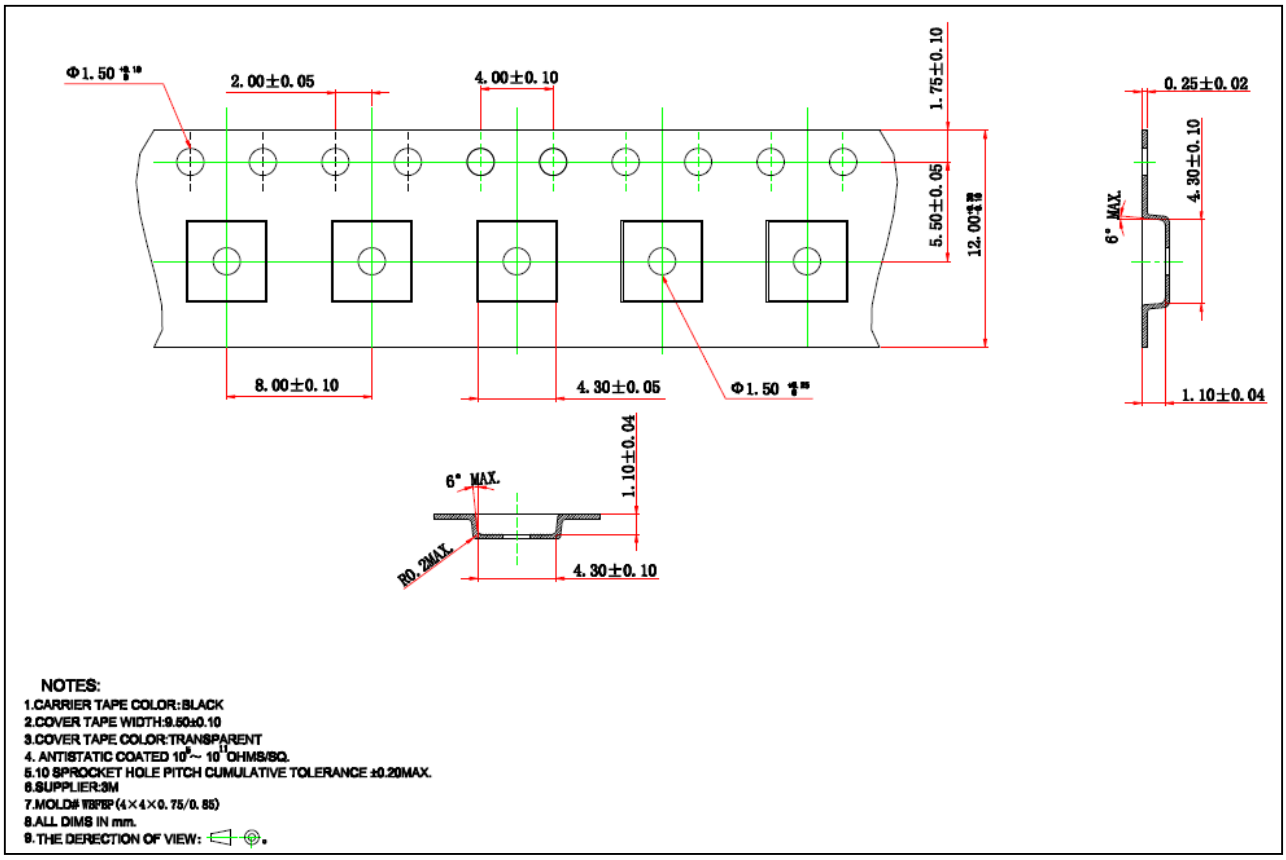


Figure 5 Classification Profile

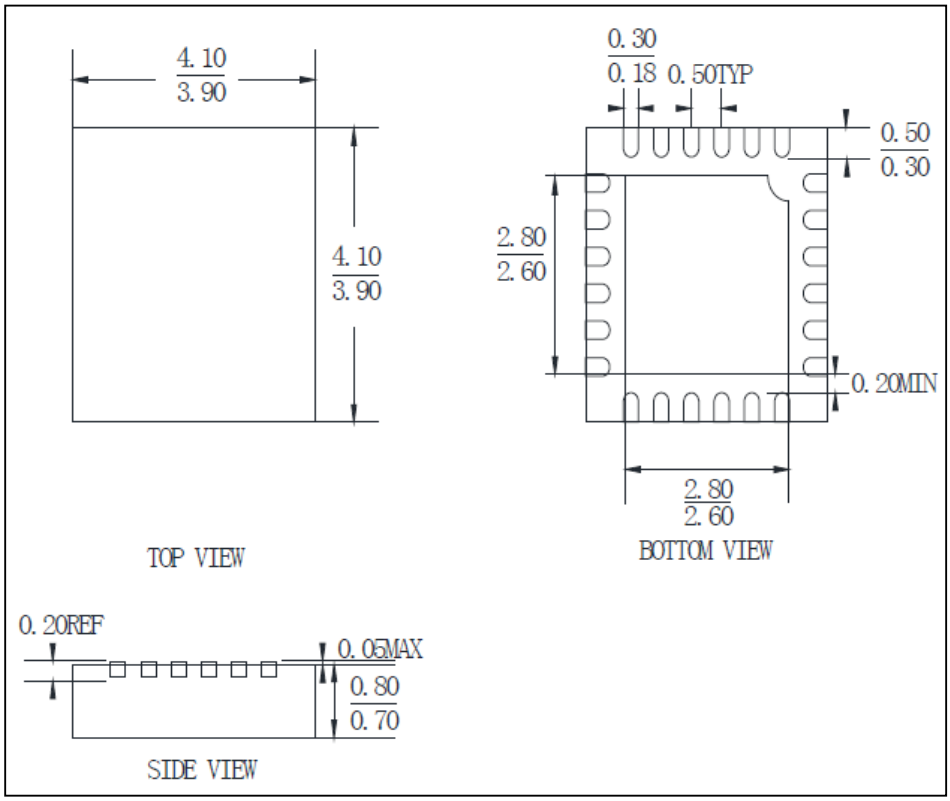
TAPE AND REEL INFORMATION



NOTES:
1.CARRIER TAPE COLOR:BLACK
2.COVER TAPE WIDTH:9.50±0.10
3.COVER TAPE COLOR:TRANSPARENT
4. ANTISTATIC COATED 10^{5}~ 10^{11} OHMS/SQ.
5.10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.20MAX.
6.SUPPLIER:3M
7.MOLD# [illegible] (4×4×0.75/0.85)
8.ALL DIMS IN mm.
9.THE DERECTION OF VIEW:

PACKAGE INFORMATION

QFN-24



Note: All dimensions in millimeters unless otherwise stated.